PCI-1553-DDC

MIL-STD-1553
PCI Module

REFERENCE MANUAL

Revision 1.2
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GENERAL DESCRIPTION

INTRODUCTION

The PCI-1553-DDC module provides Bus Controller (BC), Remote Terminal (RT) and Bus Monitor (BM) dual-redundant operations on the MIL-STD-1553 bus. The PCI form factor provide easy installation.

The ***PCI-1553-DDC-1*** is installed with the following resources:

- DDC ACE RISC based processor unit
- 64K x 16 bit dual ported SRAM
- Supports Bus Controller, Remote Terminal and Bus Monitor mode
- RT address and operational modes are program or jumper selectable
- 1553 bus long or short stub jumper option

The ***PCI-1553-DDC-2*** is installed with the following resources:

- 2 DDC ACE RISC based processor units
- 2 64K x 16 bit dual ported SRAMs
- Supports Bus Controller, Remote Terminal and Bus Monitor mode
- RT address and operational modes are program or jumper selectable
- 1553 bus long or short stub jumper option

FUNCTIONAL DESCRIPTION

A functional block diagram of the PCI module is depicted below in Figure 1. The PCI-1553-DDC is designed around the ACE that is used to manage the 1553 BUS.

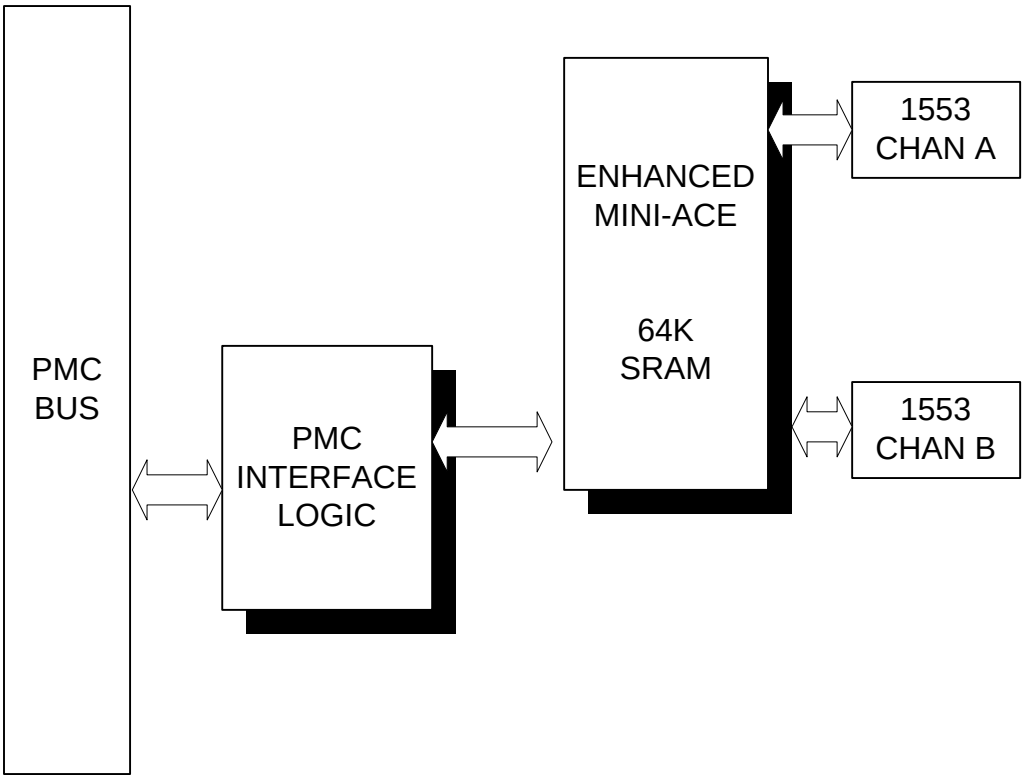
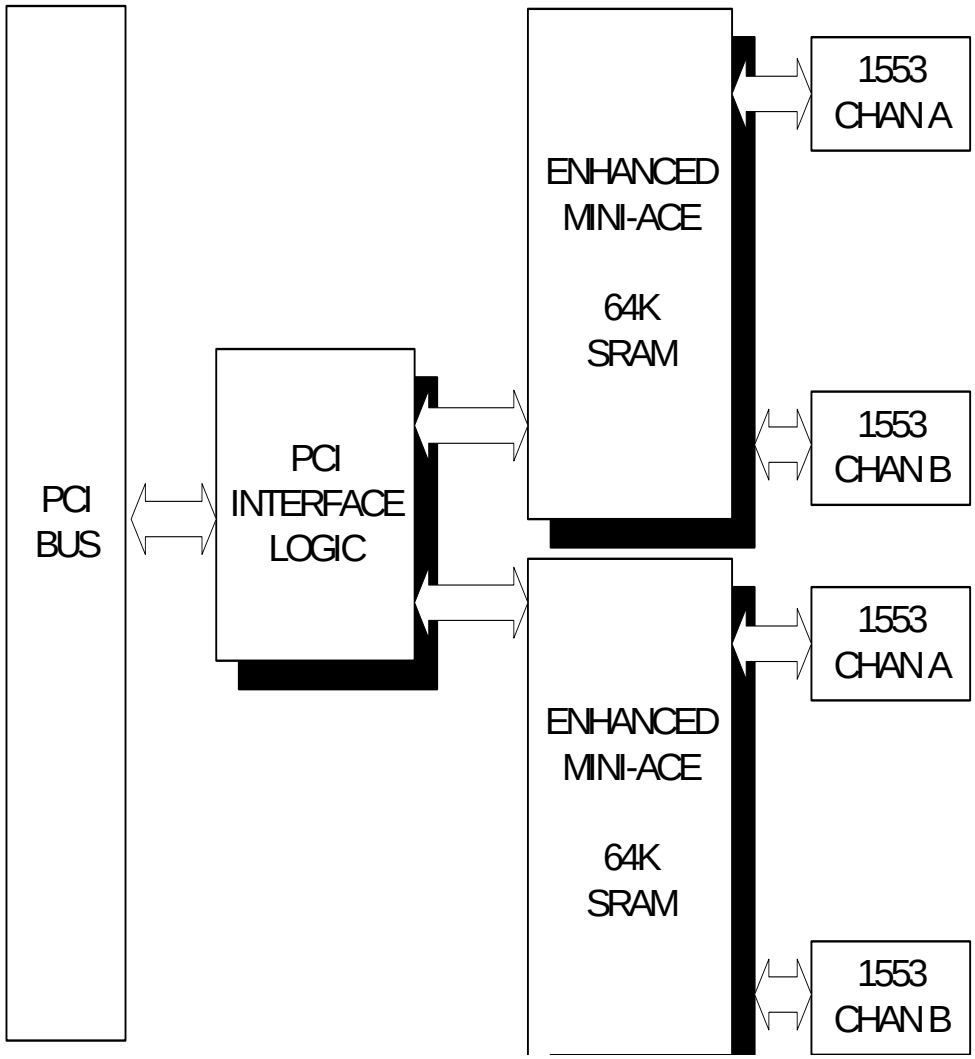


Figure 1 PCI-1553-DDC-1



REFERENCE MATERIALS LIST

The reader should refer to the “ACE USER’S GUIDE”, from DDC, that provides detailed descriptions about the ACE registers.

DDC
105 Wilbur Place
Bohemia, New York 11716-2482

Marketing Department :
Tel: (631) 567-5600 ext. 7257 or 7381,
Fax: (631) 567-7358

Technical Information :
1-800-DDC-5757 ext. 7257 or 7381
Literature Requests :
Headquarters - Tel: (631) 567-5600 ext. 7257 or 7381, Fax: (631) 567-7358
Southeast - Tel: (703) 450-7900, Fax: (703) 450-6610
West Coast - Tel: (714) 895-9777, Fax: (714) 895-4988
Europe - Tel: +44-(0)1635-811140, Fax: +44-(0)1635-32264
Asia/Pacific - Tel: +81-(0)3-3814-7688, Fax: +81-(0)3-3814-7689

WWW Home Page :
http://www.ddc-web.com

The reader should refer to the PCI Local Bus Specification for a detailed explanation of the PCI bus architecture and timing requirements. This specification is available from the following source:

PCI Special Interest Group
PO Box 14070
Portland, OR 97214
Tel: (800) 433-5177
Tel: (503) 797-4207
Fax: (503) 234-6762

The reader is also referred to the PLX-9080 PCI Controller data book:
PLX TECHNOLOGY
6195 Lusk Boulevard
San Diego, CA 92121-2793
Tel: (800) 755-2622

HOST (PCI) SIDE

1.0 Interface to HOST (PCI)

All PCI devices contain a set of registers in Configuration Space which allow for determining the manufacturer and model of the device, determining the resources necessary for the correct operation of the device, and other configuration information. Configuration space is decoded on a per slot / device basis via a mechanism described in the PCI specification.
All PCI devices can be relocated in physical memory by means of several Base Address Registers. These registers contain the high address bits, which must be matched for any access to the card to be successful. Part of the protocol of programming the Base Address Registers allows for the transfer of information regarding the size of the regions. The actual Base Address Registers are located in Configuration Space.
Normally, configuring the card is performed by the system controller and some form of firmware or BIOS. Unfortunately, determining Base Addresses and other configuration information in Configuration Space is operating system dependent. One of the primary functions of the device driver under Windows NT is to map these resources to the user application.
The card is actually accessed through the decoded base address registers.

PCI Configuration Space

PCI Address: *CONFIG:0x00 – 0x3C*
Mode of Access: *Read/Write*
Reset By *PCI Hardware Reset*

The card has the following registers available to PCI Configuration Space. They are implemented in the PLX chip. The registers are also accessible from the DSP Local bus.

Offset Into PCI CFG	31 – 24	23 – 16	15 – 8	7 – 0
0x00	Device ID		Vendor ID	
0x04	Status		Command	
0x08	Class Code			Revision ID
0x0C	BIST	Header Type	PCI Latency Timer	Cache Line Size
0x10	PCI Base Address 0 (Memory Access to PLX Registers)			
0x14	PCI Base Address 1 (I/O Access to PLX Registers)			
0x18	PCI Base Address 2 (Memory Access to DSP SRAM and card registers)			

0x1C	PCI Base Address 3 (Not Used for this card)			
0x20	Unused PCI Base Address 4			
0x24	Unused PCI Base Address 5			
0x28	Cardbus CIS Pointer (Not Supported)			
0x2C	Subsystem ID		Subsystem Vendor ID	
0x30	PCI Base Address for Expansion ROM			
0x34	Reserved			
0x38	Reserved			
0x3C	Max Latency	Min Grant	Interrupt Pin	Interrupt Line

Table 1.0 : PCI Configuration Space

The card presents the following initial configuration values to the PCI system, based on the values stored in the NVRAM device read by the PLX PCI9080 interface chip.

Register	Value (Meaning)
Vendor ID	0x13C5 (ALPHI Technology)
Device ID	0x0110 (PCI-1553-DDC-1) 0x111 (PCI-1553-DDC-2)
Revision ID	0x00
Class Code	0xff0000 (Device does not fit into defined class codes)
Interrupt Line	0xff
Interrupt Pin	A
Multifunction Device	No
Build In Self Test	No
Latency Timer	0x00
Minimum Grant	0x00
Maximum Latency	0x00
Base Address 0 Size	0x256 Bytes Allocated
Base Address 1 Size	0x256 Bytes Allocated
Base Address 2 Size	0x256 Bytes Allocated
Base Address 3 Size	0x256 KBytes Allocated
Expansion ROM Size	None

Table 1.1: PCI Configuration Register Default Values

PCI Base Address Regions

HOST Address	WIDTH USED	Description	TYPE
BAR0	64 BYTES 0X0h– 3Fh	PLX Operation Registers	MEM
BAR1	256 BYTES	NOT USED	I/O
BAR2	128 BYTES 0X0h– 7Fh	Ch 1 EN-MINI-ACE IO Space	MEM
BAR3	128 KBYTE 0X0h– 1FFFFh	Ch 1 EN-MINI-ACE DUAL PORTED SRAM	MEM

Table 2 PCI-1553-DDC-1

HOST Address	WIDTH	Description	TYPE
BAR0	64 BYTES 0X0h– 3Fh	PLX Operation Registers	MEM
BAR1	256 BYTES	NOT USED	I/O
BAR2	256 BYTES: 0X0h– 7Fh 0X80h– FFh	EN-MINI-ACE IO Space Ch 1 EN-MINI-ACE IO Space (128b) Ch 2 EN-MINI-ACE IO Space (128b)	 MEM MEM
BAR3	256 KBYTES 0X0h– 1FFFFh 0X20000h– 3FFFFh	EN-MINI-ACE DUAL PORT SRAM CH 1 DUAL PORT SRAM (128KB) CH 2 DUAL PORT SRAM (128KB)	 MEM MEM

Table 3 PCI-1553-DDC-2

JUMPER LOCATION DIAGRAM

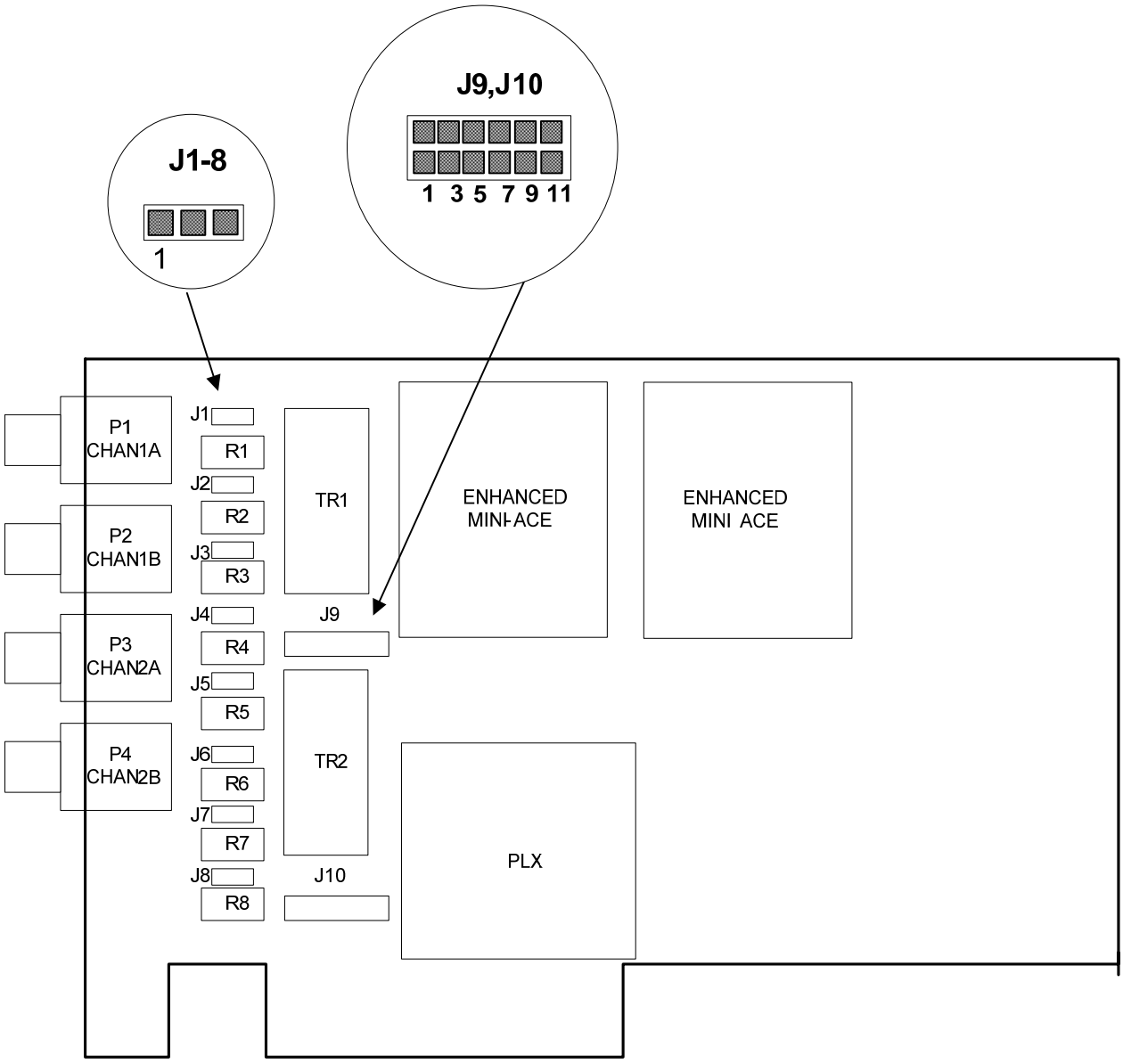


Figure 3

JUMPER	FACTORY SETTING	DESCRIPTION
J1	1-2	Long Stub/Short Stub Output channel 1A - (Short Stub)
J2	2-3	Long Stub/Short Stub Output channel 1A + (Short Stub)
J3	1-2	Long Stub/Short Stub Output channel 1B + (Short Stub)
J4	2-3	Long Stub/Short Stub Output channel 1B - (Short Stub)
J5	1-2	Long Stub/Short Stub Output channel 2A - (Short Stub)
J6	2-3	Long Stub/Short Stub Output channel 2A + (Short Stub)
J7	1-2	Long Stub/Short Stub Output channel 2B + (Short Stub)
J8	2-3	Long Stub/Short Stub Output channel 2B - (Short Stub)
J9	None	Remote terminal address and parity Summit 1
J10	None	Remote terminal address and parity Summit 2
P5	None	Altera programming plug

Table 4

J9,10 RT Address Selection

Signal	Jumper set	Description
RTPT	1-2	RT Address Parity
RTA4	3-4	RT Address Bit 4
RTA3	5-6	RT Address Bit 3
RTA2	7-8	RT Address Bit 2
RTA1	9-10	RT Address Bit 1
RTA0	11-12	RT Address Bit 0

Table 5

CONNECTION HARDWARE FOR 1553 BUS

The following hardware is available from:

Trompeter Electronics, Inc.
31186 La Baya Drive
P.O. Box 5069
Westlake Village, CA
91362-4047

Phone: (818) 707-2020
Fax : (818) 706-1040

PL155-29	Mating plug for P2 and P3 (1553 Channels A and B)
TWC-78-1	Cable meets 1553B requirements, 78 Ohm impedance
TNGM1-1-78	78 Ohm terminator
BN153	Tee connector

Contact the above manufacturer for other cabling options. They also can build complete cable assemblies to meet your requirements.

