

CPCI-SIP

**Slave Dual IndustryPack® Carrier
for 3U *CompactPCI™* systems**

REFERENCE MANUAL

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1. GENERAL DESCRIPTION

1.1 INTRODUCTION

The CPCI-SIP is a 3U format CompactPCI (CPCI) bus IP carrier. The **CPCI-SIP** provides mechanical support and the electrical interfaces for two single width IP modules, or a double width IP module. Multiple **CPCI-SIP** boards may be installed in a single system. The primary features of the **CPCI-SIP** are as follows:

- Support for up to two IP modules
- 8 MHz or 32 MHz IP operation via jumper selection
- Direct I/O or Memory mapped access from CPCI bus via AMCC 5933 PCI Chip
- Supports double-wide form factor IndustryPack®
- Full interrupt support of host
- Front panel I/O connectors for all IPs

1.2 FUNCTIONAL DESCRIPTION

A functional block diagram of the **CPCI-SIP** is presented below in Figure 1-1. The jumper placement and the connector placement is depicted in Figure 1-2. The **CPCI-SIP** operates as a slave that is managed by the host processor on the CPCI bus. Each pair of IP modules share a common clock that can be jumpered for 8 or 32 MHz operation.

The **CPCI-SIP** is supported by ALPHI Technology under *Windows NT* by a **Board Support Package** which is supplied with the card. Other documentation supplied with the card will describe this support in full detail.

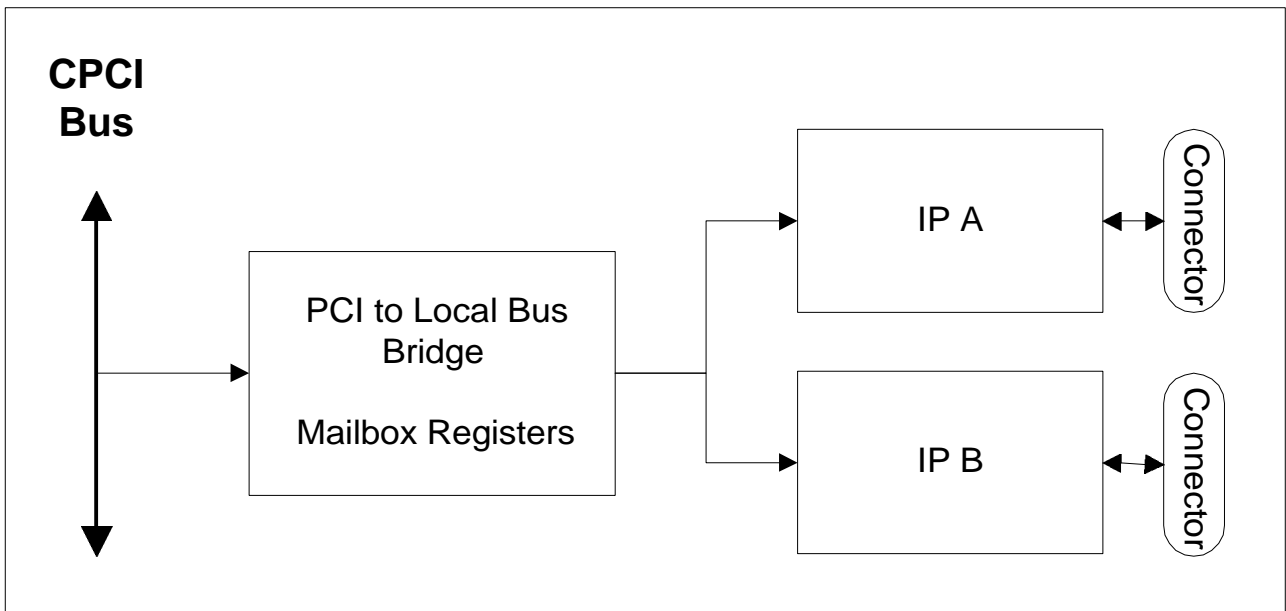


Figure 1.1: Block Diagram

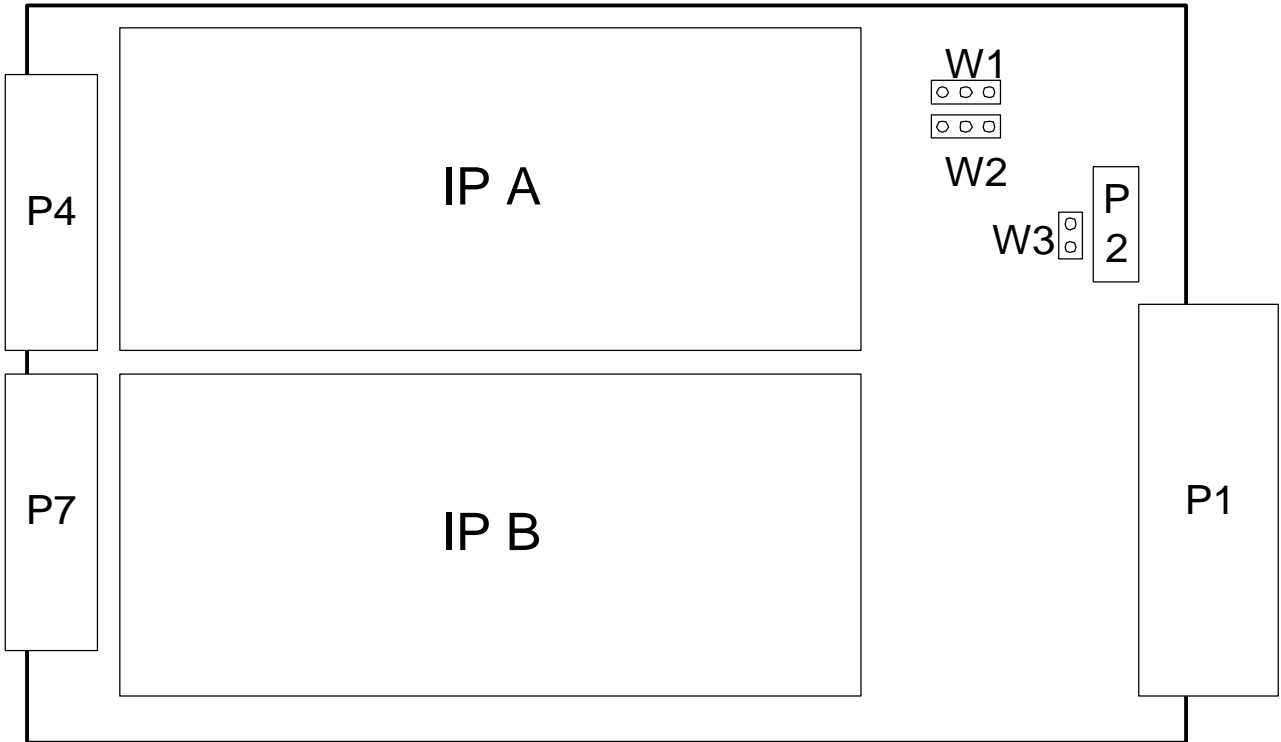


Figure 1.2: Jumper and Connector Locations

1.3 REFERENCE MATERIALS LIST

The reader should refer to the PCI Local Bus Specification for a detailed explanation of the PCI bus architecture and timing requirements. This specification is available from the following source:

PCI Special Interest Group

PO Box 14070

Portland, OR 97214

Tel: (800) 433-5177

Tel: (503) 797-4207

Fax: (503) 234-6762

The reader is also referred to the S5933 PCI Controller data book:

AMCC Applied Micro Circuits Corporation

6195 Lusk Boulevard

San Diego, CA 92121-2793

Tel: (800) 755-2622

<http://www.amcc.com>

WindowsNT and Windows95 Programming Tools:

BlueWater Systems

144 Railroad Ave. Suite #217

Edmonds, WA 98020

Tel: (206) 771-3610

Fax: (206) 771-2742

E-Mail: info@bluewatersystems.com

Web: <http://www.bluewatersystems.com>

2. HOST (CPCI) SIDE

2.1 PCI CONFIGURATION REGISTERS

The card presents the following configuration values to the CPCI system, based on the values stored in the NVRAM device read by the AMCC PCI interface chip.

Register	Value (Meaning)
Vendor ID	0x13c5 (ALPHI Technology)
Device ID	0x0102 (CPCI-SIP)
Revision ID	0x00
Class Code	0xff0000 (Device does not fit into defined class codes)
Interrupt Line	0xff
Interrupt Pin	A
Multifunction Device	No
Build In Self Test	No
Latency Timer	0x00
Minimum Grant	0x00
Maximum Latency	0x00
Expansion ROM Size	None

Table 2.1: CPCI Configuration Registers

2.2 PCI BASE ADDRESS REGISTERS

The card requests base address regions from the CPCI system after RESET, based on the values stored in the NVRAM device read by the AMCC PCI interface chip.

The decode addresses of these regions are assigned by the host processor. The **CPCI-SIP** uses 3 of the 5 AMCC mapped base address registers. The AMCC is normally programmed at the factory to request the following resource from the CPCI BIOS:

BAR	From	To	Description	Type
0	0x00000000	0x00000003F	AMCC PCI Operation Registers	MEM
1	0x00000000	0x000001FF	IP ID and IO Region	MEM
3	0x00000000	0x00FFFFFF	IP Memory Region	MEM

Table 2.2: Base Address and Use

NOTE: The AMCC has been programmed to request memory above 1 Mbytes.

2.3 CPCI OPERATION REGISTERS

The host processor communicates with the **CPCI-SIP** card via the AMCC pass-through interface. After the base address register has been programmed by the CPCI configurator, incoming CPCI I/O or Memory cycles are used to access the registers of the AMCC chip. The PCI Operation Registers of the AMCC 5933 chip are depicted below:

Offset	Register Name
0x00	OMB1 Outgoing Mailbox Register 1
0x04	OMB2 Outgoing Mailbox Register 2
0x08	OMB3 Outgoing Mailbox Register 3
0x0C	OMB4 Outgoing Mailbox Register 4
0x10	IMB1 Incoming Mailbox Register 1
0x14	IMB2 Incoming Mailbox Register 2
0x18	IMB3 Incoming Mailbox Register 3
0x1C	IMB4 Incoming Mailbox Register 4
0x20	FIFO Register Port (bi-directional)
0x24	MWAR Master Write Address Register
0x28	MWTC Master Write Transfer Counter
0x2C	MRAR Master Read Address Register
0x30	MRTC Master Read Transfer Counter
0x34	MBEF Mailbox Empty/Full Status
0x38	INTCSR Interrupt Control/Status Register
0x3C	MCSR Bus Master Control/Status Register

Table 2.3: AMCC Registers (HOST)

For more information about these registers refer to the AMCC PCI controller manual.

2.4 IP ID AND I/O REGION

16 bit accesses to the following offsets from BAR1 will allow for communication with the two IPs. Unspecified addresses are reserved. Note that the **CPCI-SIP** only supports 16 bit access to the I/O regions, but it does support 32 bit access to memory regions.

FROM	TO	R/W	REGION
0x00	0x3F	R/W	IP_A ID Space
0x40	0x41	R	IP_A Interrupt Vector 0
0x42	0x43	R	IP_A Interrupt Vector 1
0x80	0xFF	R/W	IP_A I/O Space
0x100	0x13F	R/W	IP_B ID Space
0x140	0x141	R	IP_B Interrupt Vector 0
0x142	0x143	R	IP_B Interrupt Vector 1
0x180	0x1FF	R/W	IP_B I/O Space

Table 2.4: IP ID and I/O Regions

2.5 IP MEMORY REGION

16 bit accesses to the following offsets from BAR3 will allow for communication with the two IPs. If the jumper is set for 32 bit access, then both IPs are strobed.

FROM	TO	R/W	REGION
0x000000	0x7FFFFFFF	R/W	IP_A Memory Space
0x800000	0xFFFFFFFF	R/W	IP_B Memory Space

Table 2.5: IP Memory Regions

3. IP DETAILS

Please consult the IP User's Manual for details about accessing the particular IP used.

3.1 IP MODULE ID SPACE

Each IP must support an identification PROM. The CPCI-SIP decodes 64 bytes of ID space for each IP module. The ID PROM contains information about each the IP, which is defined in the IndustryPack Specification. The two IP I/O spaces can be accessed at fixed offsets from Base Address 1, as indicated in Table 2.4. The information required for the most common IP PROM format is shown below:

OFFSET	DESCRIPTION	VALUE
0x00	ASCII "I"	0x49
0x02	ASCII "P"	0x50
0x04	ASCII "A"	0x41
0x06	ASCII "C"	0x43
0x08	Manufacturer ID	
0x0A	Model No	
0x0C	Revision	
0x0E	Reserved	0x00
0x10	Driver ID, Low Byte	
0x12	Driver ID, High Byte	
0x14	Number of bytes used	0x0C
0x16	CRC	
0x18-0x3F	User Space	

Table 3.1: Typical ID Space Layout

3.2 IP MODULE IO SPACE

The CPCI-SIP decodes 128 bytes of IO space for each IP module. The two IP I/O spaces can be accessed at fixed offsets from Base Address 1, as indicated in Table 2.4.

3.3 IP MODULE MEMORY SPACE

The CPCI-SIP decodes 8 Mbytes of MEM space for each IP module. The two IP MEM spaces can be accessed at fixed offsets from Base Address 3, indicated in Table 2.5.

3.4 IP MODULE INTERRUPT SPACE

The CPCI-SIP routes the interrupts from all IP modules to the INTA# signal on the CompactPCI bus. The CPCI-SIP decodes 2 16 bit words of INT space for each IP module to supply an optional interrupt vector. The two IP INT spaces can be accessed at fixed offsets from Base Address 1, as indicated in Table 2.4. IMB4 in the AMCC 5933 PCI Interface chip is written by the CPCI-SIP hardware when one or more IP modules are asserting an interrupt. If incoming Mailbox 4 Byte 3 interrupts have been enabled, then the CPCI-SIP will assert INTA#. Some IP modules may require that the host processor perform a read to INT space to clear pending interrupts. The PCI Operation Registers MBEF and INTCSR can be used to manage IP interrupts. See the Board Support Package for examples of how to support HOST interrupts.

4. RESET SIGNALS

The **CPCI-SIP** can be reset from two different sources:

- At power on or when the PCI RESET is asserted, the watchdog timer will hold the IP reset lines low for 200 ms.
- The AMCC has a bit called SYSRST which the HOST can toggle to reset the IPs. Software should hold the RESET asserted for 200 mS to meet the IP specifications.

5. JUMPER DESCRIPTIONS

JUMPER	FACTORY SETTING	DESCRIPTION
W1	2-3	IP A Clock Speed. 1-2 for 32 MHz, 2-3 for 8 MHz. 8 MHz is default.
W2	2-3	IP B Clock Speed. 1-2 for 32 MHz, 2-3 for 8 MHz. 8 MHz is default.
W3	1-2	When shorted, supports 16 bit IP memory access.

Table 5.1 Jumper Descriptions

6. LED INDICATORS

There are four LED indicators visible at the CPCI card bracket. They are marked with a legend on the bracket, and they are labeled on the PCB as L1 – L4 where L1 is at the top of the card.

The LEDs have the following meanings:

LED	LEGEND	Meaning
L1	WR	HOST is writing to IP.
L2	RD	HOST is reading from IP.
L3	IP B	DSP is accessing IP B.
L4	IP A	DSP is accessing IP A.

Table 6.1 LED Descriptions

7. CONNECTIONS

7.1 IP I/O CONNECTORS (P4, P7)

Connector	I/O for
P4	IP_A
P7	IP_B

50 pin high density flat cable connectors are used to route all the IP I/O signals off the card. ALPHI Technology can supply transition modules and cable assemblies to meet any special requirements. Contact the factory for additional information.

Connectors are manufactured by HIROSE.

Use	Model
On PC Board	HIF6A-50PA-1.27DS
Suggested Plug	H1F6-50D-1.27R

Table 7.1: I/O Connector Model Numbers

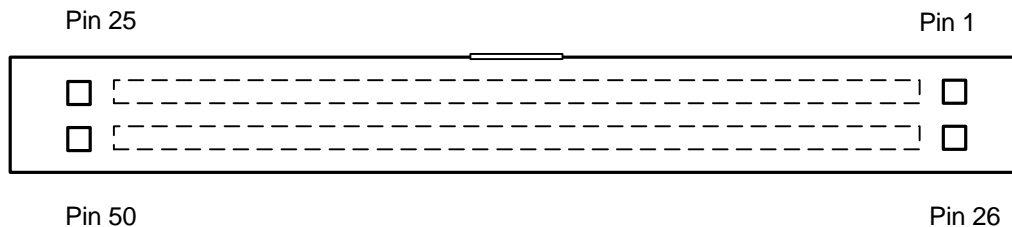


Figure 7.1: IP I/O CONNECTORS

The I/O signals for the two IPs are directly routed off the card through the front panel.

7.2 FACTORY USE (J2)

This connector is used at the factory for programming the FPGA.

7.3 32 BIT CPCI BUS (P1)

This connector plugs into the backplane and provides the standard CPCI signals for all CPCI systems.