CPCI-MFIO

Intelligent DSP Based
Multi-Function I/O Card
for 6U *CompactPCI*™ systems

REFERENCE MANUAL

761-10-000-4000
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Part Number : 761-10-000-4000

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1. GENERAL DESCRIPTION

1.1 INTRODUCTION

The **CPCI-MFIO** is an intelligent DSP based Multi-Function I/O card in a 6U CPCI form factor. The **CPCI-MFIO** provides up to 32 single ended or 16 differential inputs to a 16-bit A/D converter. The CPCI-MFIO supports 4 analog outputs and a general purpose digital I/O ports. The CPCI-MFIO also supports up to to PMC carrier slots. The DSP allows for the offloading from the HOST CPU any necessary I/O processing to monitor and service these channels. The primary features of the **CPCI-MFIO** are as follows:

- Integrated DSP (TI TMS320C31) at 60 MHz to offload I/O operation from host or for standalone applications
- 128K x 32 bit zero wait state SRAM for the DSP.
- 512K by 8 bit FLASH device for customer applications
- Up to 32 single ended or 16 differential analog inputs to a pair of 16 bit converters.
- Programmable PGA allow for gains of 1, 10, 100, or 1000.
- Programmable capture rates from 2 channels @ 100 KHz, to 32 channels @ 6250 Hz.
- Full support for automatic calibration of the inputs.
- 4 channels of 16 bit analog output
- Up to 16 bits of general purpose digital input or output.
- Bus Master DMA to offload HOST processor.
- Support two PMC Carrier Slots

1.2 FUNCTIONAL DESCRIPTION

A functional block diagram of the **CPCI-MFIO** is presented below in Figure 1-1. The jumper placement and the connector placement is depicted in Figure 1-2. The **CPCI-MFIO** can operate as a slave that is managed by the host processor on the CPCI bus or it can operate in a standalone mode of operation without a host.

The **CPCI-MFIO** is supported by ALPHI Technology under *Windows NT* by a **Board Support Package** that is supplied with the card. Other documentation supplied with the card will describe this support in full detail.

The card is also supported by a **DSP Support Library** providing the following features:

- Common access routines for communications with the HOST
- Identify the applicable card resources and parameters

All these are provided in a manner consistent across ALPHI Technology platforms. Other documentation supplied with the card will describe the support in full detail.

A bootloader provided on the card allows for control by the HOST and for independent operation in stand alone operation. User code can be downloaded to FLASH memory and booted automatically on reset. Access to the card can be made by the HOST CPCI bus.

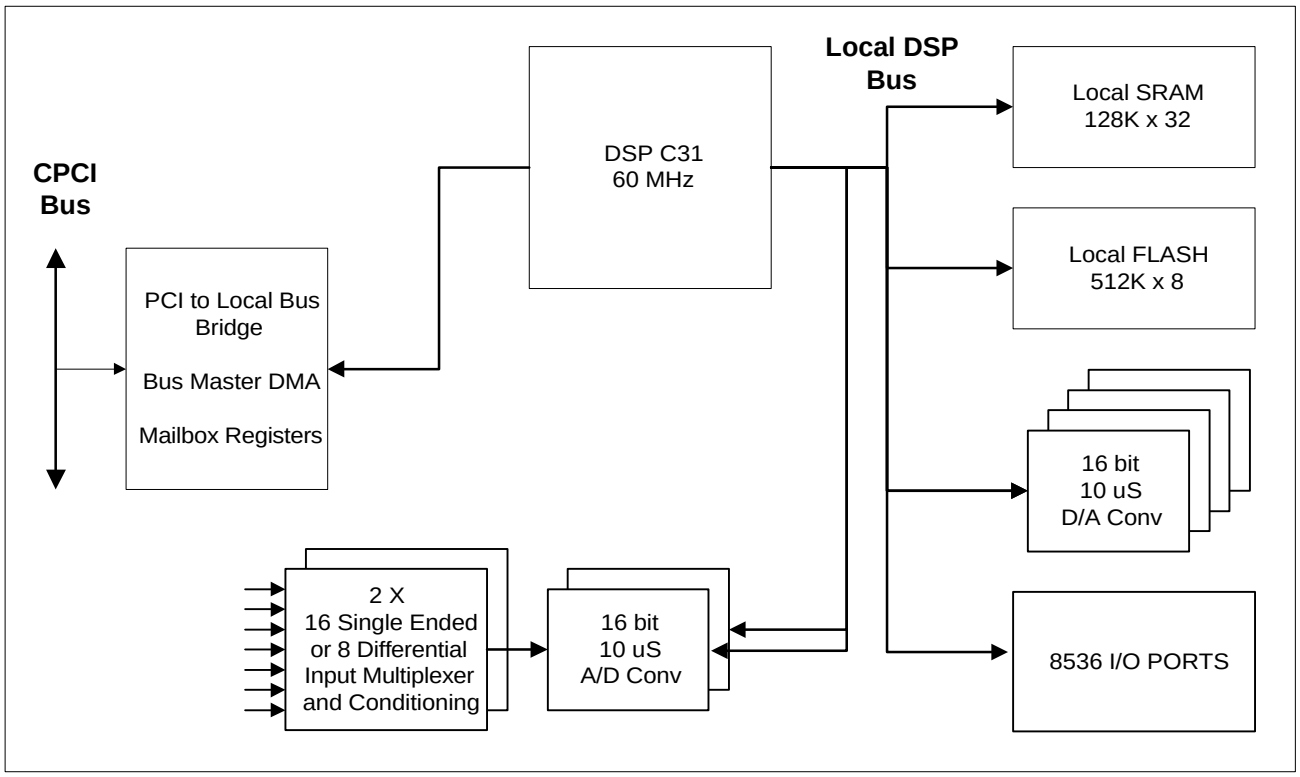

Figure 1.1: Block Diagram

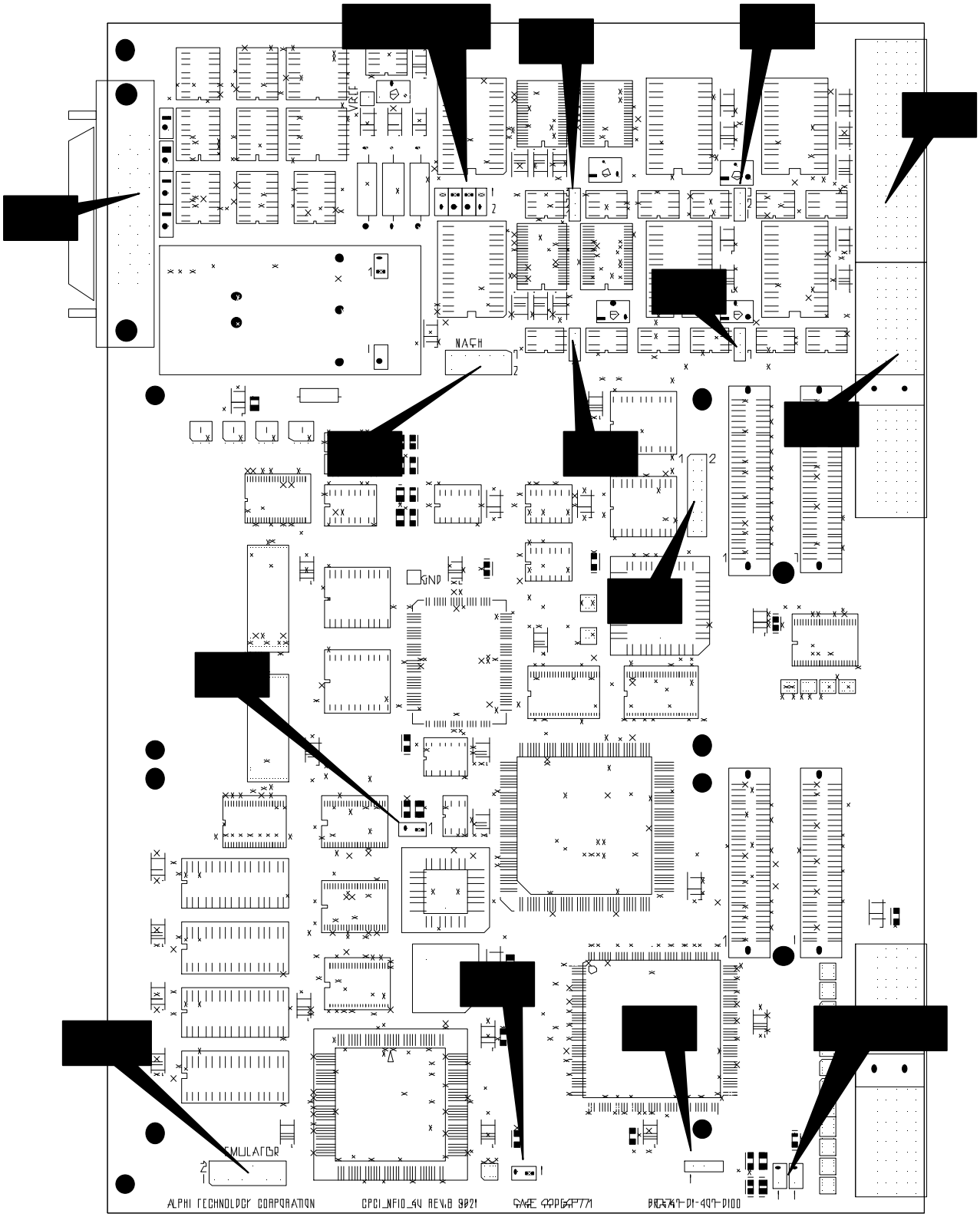

Figure 1.2: Jumper and Connector Locations

1.3 REFERENCE MATERIALS LIST

The reader should refer to the PCI Local Bus Specification for a detailed explanation of the PCI bus architecture and timing requirements. This specification is available from the following source:

PCI Special Interest Group
PO Box 14070
Portland, OR 97214
Tel: (800) 433-5177
Tel: (503) 797-4207
Fax: (503) 234-6762

The reader is also referred to the S5933 PCI Controller data book:

AMCC Applied Micro Circuits Corporation
6195 Lusk Boulevard
San Diego, CA 92121-2793
Tel: (800) 755-2622
http://www.amcc.com

WindowsNT and Windows95 Programming Tools:

BlueWater Systems
144 Railroad Ave. Suite #217
Edmonds, WA 98020
Tel: (206) 771-3610
Fax: (206) 771-2742
E-Mail: info@bluewatersystems.com
Web: http://www.bluewatersystems.com

2. HOST (CPCI) SIDE

2.1 PCI CONFIGURATION REGISTERS

The card presents the following configuration values to the CPCI system, based on the values stored in the NVRAM device read by the AMCC PCI interface chip.

Register	Value (Meaning)
Vendor ID	0x13c5 (ALPHI Technology)
Device ID	0x0204
Revision ID	0x00
Class Code	0xff0000 (Device does not fit into defined class codes)
Interrupt Line	0xff
Interrupt Pin	A
Multifunction Device	No
Build In Self Test	No
Latency Timer	0x00
Minimum Grant	0x00
Maximum Latency	0x00
Expansion ROM Size	None

Table 2.1: CPCI Configuration Registers

2.2 PCI BASE ADDRESS REGISTERS

The card requests base address regions from the CPCI system after RESET, based on the values stored in the NVRAM device read by the AMCC PCI interface chip.

The decode addresses of these regions are assigned by the host processor. The **CPCI-MFIO** uses 1 of the 5 AMCC mapped base address registers. The AMCC is normally programmed at the factory to request the following resource from the CPCI BIOS:

BAR	From	To	Description	Type
0	0x00000000	0x00000003F	AMCC PCI Operation Registers	MEM

Table 2.2: Base Address and Use

NOTE: The AMCC has been programmed to request memory above 1 Mbytes.

2.3 CPCI OPERATION REGISTERS

The host processor communicates with the **CPCI-MFIO** card via the AMCC pass-through interface. After the base address register has been programmed by the CPCI configurator, incoming CPCI I/O or Memory cycles are used to access the registers of the AMCC chip. The PCI Operation Registers of the AMCC 5933 chip are depicted below:

Offset	Register Name
0x00	OMB1 Outgoing Mailbox Register 1
0x04	OMB2 Outgoing Mailbox Register 2
0x08	OMB3 Outgoing Mailbox Register 3
0x0C	OMB4 Outgoing Mailbox Register 4
0x10	IMB1 Incoming Mailbox Register 1
0x14	IMB2 Incoming Mailbox Register 2
0x18	IMB3 Incoming Mailbox Register 3
0x1C	IMB4 Incoming Mailbox Register 4
0x20	FIFO Register Port (bi-directional)
0x24	MWAR Master Write Address Register
0x28	MWTC Master Write Transfer Counter
0x2C	MRAR Master Read Address Register
0x30	MRTC Master Read Transfer Counter
0x34	MBEF Mailbox Empty/Full Status
0x38	INTCSR Interrupt Control/Status Register
0x3C	MCSR Bus Master Control/Status Register

Table 2.3: AMCC Registers (HOST)

For more information about these registers refer to the AMCC PCI controller manual.

3. C31 SIDE

3.1 INTERNAL ORGANIZATION

The **CPCI-MFIO** card is divided into different sections. Each section and its relationship to other sections will be discussed. The **CPCI-MFIO** sections are:

- CPCI interface
- DSP Memory and Register Map
- Analog input interface
- Analog output interface
- Digital interface

3.2 CPCI INTERFACE

The local DSP processor communicates with the CPCI bus through the AMCCS9533 chip that provides bi-directional FIFO and Mailbox registers. The **CPCI-MFIO** can function as both a servant (CPCI target) or as a master (CPCI initiator) for DMA access. The following interface descriptions refer to the CPCI interface as seen by the local DSP. The AMCC registers are located at DSP address 0xf00080.

3.2.1 BI-DIRECTIONAL FIFO

Two separate FIFO data paths are implemented within the AMCCS9533, a read FIFO that allows data transfers from the module to the CPCI bus and a write FIFO that transfers data

from the CPCI to the module. Size of the FIFO is 32 bit X 8. Read and write DMA access to the host can occur via the FIFO registers if it is supported by the software on the HOST and is enabled. Alternatively, the FIFO registers can utilize a polled scheme on the HOST and DSP. Both FIFOs are accessed via access to the same location as seen by the DSP, offset 0x08.

3.2.2 MAILBOX REGISTERS

The Mailbox registers of the AMCCS9533 provide a bi-directional data path that can be used to send data or software control information between the HOST and DSP of that half of the **CPCI-MFIO** module. Interrupts can be enabled based on a specific mailbox event. There are 4 incoming mailboxes and 4 outgoing mailboxes. Each mailbox is 32 bits wide. The address offsets for the mailboxes are shown below in Table 3-1.

3.2.3 ADDITIONAL REGISTERS

The AMCC S5933 PCI controller has a set of additional registers to control and monitor the behavior of the CPCI interface.

The address offsets of these registers are shown below in Table 3-1.

Offset	Register Name
0x00	Incoming Mailbox Reg 1
0x01	Incoming Mailbox Reg 2
0x02	Incoming Mailbox Reg 3
0x03	Incoming Mailbox Reg 4
0x04	Outgoing Mailbox Reg 1
0x05	Outgoing Mailbox Reg 2
0x06	Outgoing Mailbox Reg 3
0x07	Outgoing Mailbox Reg 4
0x08	Add-on FIFO port
0x09	Bus master write Address Register
0x0A	Add-on Pass through Address
0x0B	Add-on Pass trough Data
0x0C	Bus master read Address Register
0x0D	Add-on Mailbox Empty/full Status
0x0E	Add-on Interrupt Control
0x0F	Add-on General Control/Status Register

Table 3.1: AMCC Registers (DSP)

For more information about these registers refer to the AMCC PCI controller manual.

3.3 DSP MEMORY AND REGISTER MAP SUMMARY

NAME	START	END	DATA	R/W	COMMENTS
SRAM	0x000000	0x01FFFF	D00-D31	R/W	Zero wait state static RAM
FLASH	0x400000	0x41FFFF	D00-D07	R/W	128K x 8 Protected
A/D RESULT	0xF00000	0xF00000	D00-D31	R	Both conversion results
CONTROL1	0xF00008	0xF00008	D00-D03	W	Controls internal settings
CONTROL2	0xF00010	0xF00010	D00-D07	W	Controls internal settings
CONTROL3	0xF00018	0xF00018	D00-D00	W	Controls internal settings
STROBE	0xF00020	0xF00020	N/A	WS	Start conversion
DACOUT1	0xF00028	0xF00028	D00-D31	W	DAC Outputs 1 and 2
DACOUT2	0xF00030	0xF00030	D00-D31	W	DAC Outputs 3 and 4
Z8536	0xF00038	0xF00038	D00-D07	R/W	Z8536 digital I/O ports
LAST CHAN	0xF00040	0xF00040	D00-D03	W	Ending channel register
MODE/GAIN	0xF00060	0xF0006F	D00-D07	R/W	Mode and gain per channel
AMCC	0xF00080	0xF000FF	D00-D31	R/W	AMCC Registers

Table 3.2: DSP Memory Map

3.3.1 A/D RESULT (Read Only)

BITS 31 - 16	BITS 15 - 00
Channel 17 – 32 Result	Channel 1 – 16 Result

This 32 bit register contains the conversion results from the two A/D converters. This result must be read during the INT2 interrupt handler, or it will be overwritten with the next conversion result. There is no status bit to indicate completion of a conversion.

3.3.2 CONTROL1 (Write Only)

BIT 03	BIT 02	BIT 01	BIT 00
CAL_MODE	EX_SCAN_EN	TCLK0_EN	EX_GATE_EN

EX_GATE_EN ***External gate enable***

If this bit is set to 1, then **EXGATE** must be low for A/D conversions. If this bit is cleared to 0, then **EXGATE** has no effect.

TCLK0_EN, EX_SCAN_EN ***A/D***

These bits determine what will trigger an A/D conversion.

EX_SCAN_EN	TCLK0_EN	DOUT Selection
0	0	Writes to ***STROBE*** will trigger conversion.
0	1	**TCLK0** from DSP will trigger conversion.
1	0	**EXTRIG** will trigger conversion.
1	1	Both **TCLK0** and **EXTRIG** will trigger conversion.

Table 3.4: Signal routing to STRB_OUT

CAL_MODE ***CALIBRATE MODE***

If this bit is set to 1, then the input multiplexers are switched to one of the calibration sources. These include ground, a +5V reference, and each of the two analog outputs.

If this bit is cleared, then the input multiplexers are connected to the analog inputs.

See the section describing the **MODE / GAIN** registers for more details.

3.3.3 CONTROL2 (Write Only)

BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 00
D/A GND	OUT4_RNG	OUT3_RNG	OUT2_RNG	OUT1_RNG	B_DIR	A_DIR	POE

POE ***Z8536 Port Output Enable***

If this bit is set to 1, then the isolation buffers for the Z8536 ports A and B are enabled. If this bit is cleared to 0, then the Z8536 is effectively isolated from the external digital signals.

A_DIR ***PIA Port A as input or output***

When this bit is set to 1, then port A will drive external circuitry. If this bit is cleared to 0, then port A will function as an input.

B_DIR ***PIA Port B as input or output***

When this bit is set to 1, then port B will drive external circuitry. If this bit is cleared to 0, then port B will function as an input.

OUT1_RNG ***Output Range for D/A 1***

If this bit is set to 1, the output range for D/A 1 is set to +/- 10 volts. If this bit is cleared, the output range for D/A 1 is set to 0 – 10 volts.

OUT2_RNG ***Output Range for D/A 2***

If this bit is set to 1, the output range for D/A 2 is set to +/- 10 volts. If this bit is cleared, the output range for D/A 2 is set to 0 – 10 volts.

OUT3_RNG ***Output Range for D/A 3***

If this bit is set to 1, the output range for D/A 3 is set to +/- 10 volts. If this bit is cleared, the output range for D/A 3 is set to 0 – 10 volts.

OUT4_RNG ***Output Range for D/A 4***

If this bit is set to 1, the output range for D/A 4 is set to +/- 10 volts. If this bit is cleared, the output range for D/A 4 is set to 0 – 10 volts.

D/A GND ***Disconnect the DAC outputs from the DACs and ground them***

When this bit is cleared to a 0, the output jacks and the signals fed back to the A/D converters for calibration are grounded. When this bit is set to a 1, the DAC outputs function normally.

3.3.4 CONTROL3 (Write Only)

BIT 01	BIT 00
ONE_CH	EXT_INT_EN

EXT_INT_EN Enable external interrupt generation on INT3

When this bit is set to 1, then a rising edge on EX_DA will trigger a DSP interrupt. If this bit is cleared to 0, then no interrupt is generated.

ONE_CH Single Channel Acquisition mode

When this bit is set to 1, then the input multiplexers are forced to the channel specified in the **LAST CHAN** register. Only a single conversion will be triggered for each trigger signal. If this bit is cleared to 0, then the state machine functions normally, scanning channels from 1 to the channel specified in the **LAST CHAN** register. Channels are acquired one at a time with 10 uS of separation between them.

3.3.5 STROBE (Write Strobe)

If enabled by the bits in **CONTROL1**, a DSP write to this location will start a conversion cycle.

3.3.6 D/A OUTPUT (Write Only)

BITS 31 - 16	BITS 15 - 00
Channel 2 Output	Channel 1 Output

A write to this 32 bit register will update both DAC outputs. The update will occur immediately and is not synced to any clocks.

3.3.7 Z8536 DIGITAL I/O PORTS

Z8536 Register	BITS 07 - 00
Port C Data Register	0xF00038
Port B Data Register	0xF00039
Port A Data Register	0xF0003A
Control Register	0xF0003B

Only the lower data bits D0-D07 are connected to the Z8536. Any read operation should mask off the upper data bits D08-D31 as they are not valid.

3.3.8 LAST CHAN (Write only)

BITS 03 - 00
Last Channel Scanned

This register is intended to serve two purposes. In state machine mode, this register sets the last valid channel for A/D acquisition. In single channel mode, this register allows the selection of a single pair of channels to acquire at high speed.

3.3.9 MODE/GAIN (Read / Write)

These 16 registers allow for gain selection and differential / single ended mode selection on a per channel basis.

BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 00
CAL1	DIFF2	G2_01	G2_00	CAL0	DIFF1	G1_01	G1_00

CAL1, CAL0 Calibration source

When calibrate mode is selected, these bits switch the calibration MUX to one of the four calibration sources.

CAL1	CAL0	Source
0	0	GND
0	1	VREF (+5 V)
1	0	DAC1 Output
1	1	DAC2 Output

Table 3.X: Calibration Sources

DIFF2, DIFF1 Differential mode selection

When normal input mode is selected, these bits select whether the channel is in differential mode or single ended. If the bit is set to 1, then the channel is in differential mode. Note that a channel may be scanned twice in differential mode if the conditions are right. See the following table for details. Note that the last channel register will terminate the table at that channel.

Channel	DIFF2 = 0	DIFF2 = 1	DIFF1 = 0	DIFF1 = 1
1	CH 17 SE	CH 09 DE	CH 01 SE	CH 01 DE
2	CH 18 SE	CH 10 DE	CH 02 SE	CH 02 DE
3	CH 19 SE	CH 11 DE	CH 03 SE	CH 03 DE
4	CH 20 SE	CH 12 DE	CH 04 SE	CH 04 DE
5	CH 21 SE	CH 13 DE	CH 05 SE	CH 05 DE
6	CH 22 SE	CH 14 DE	CH 06 SE	CH 06 DE
7	CH 23 SE	CH 15 DE	CH 07 SE	CH 07 DE
8	CH 24 SE	CH 16 DE	CH 08 SE	CH 08 DE
9	CH 25 SE	CH 09 DE	CH 09 SE	CH 01 DE
10	CH 26 SE	CH 10 DE	CH 10 SE	CH 02 DE
11	CH 27 SE	CH 11 DE	CH 11 SE	CH 03 DE
12	CH 28 SE	CH 12 DE	CH 12 SE	CH 04 DE
13	CH 29 SE	CH 13 DE	CH 13 SE	CH 05 DE
14	CH 30 SE	CH 14 DE	CH 14 SE	CH 06 DE
15	CH 31 SE	CH 15 DE	CH 15 SE	CH 07 DE
16	CH 32 SE	CH 16 DE	CH 16 SE	CH 08 DE

Table 3.x: Input channel selections.

G2_01, G2_00, G1_01, G1_00 Gain Selection

Input gains are selected on a per channel basis according to the following table.

Gx_01	Gx_00	Gain Selected
0	0	1
0	1	10
1	0	100
1	1	1000

Table 3.X: Gain Selection

3.4 RESET SIGNALS

The **CPCI-MFIO** can be reset from two different sources:

- At power on or when the PCI RESET is asserted, the watchdog timer will hold the C31 RESET line low for 200 mS.
- The AMCC has a bit called SYSRST which the HOST can toggle to reset the DSP and internal logic. Software should hold the RESET asserted for 200 mS to ensure a proper reset.

3.5 LOCAL DSP INTERRUPT SOURCES

The local DSP has four interrupt lines. The source of each interrupt is listed in the table below. Additionally, at reset, the INT1 line is pulsed to tell the C31 to find the FLASH image at 0x400000 (if boot mode is MC).

SOURCE	ENABLE SIGNAL	INTERRUPT LEVEL
External Gate	None	INT0
AMCC	Inside 5933	INT1
AMCC FIFO: WR not Full RD not Empty	None	INT1
A/D Data Ready	None	INT2
Ext Interrupt	**CONTROL** register	INT3

Table 3.5: Interrupt Sources

4. JUMPER DESCRIPTIONS

JUMPER	FACTORY SETTING	DESCRIPTION
W1	None	D/A 1 Reference Select
W2	None	D/A 3 Reference Select
W3	None	Factory use.
W4	None	Factory use.
W5	None	D/A 2 Reference Select
W6	None	D/A 4 Reference Select
W7	None	Z8536 Port C I/O Routing
W8	None	When shorted, provides DSP and board reset.
W9	None	DSP Boot Mode: MC/~MP. The DSP's boot mechanism is designed to operate in MC mode, booting from the FLASH.
W10	None	Factory use only
W11	None	If installed, connects 30 MHz clock to PCI clock for stand alone operation and access to AMCC. Hosted operation is default.
W12	None	If installed, forces PCI reset high for stand alone operation. Hosted operation is default.

Table 4.1 Jumper Descriptions

5. CONNECTIONS

5.1 EXTERNAL ANALOG INPUT CONNECTOR (P1)

A 50 pin D shelled connector is used to route the analog inputs to the card. ALPHI Technology can supply transition modules and cable assemblies to meet any special requirements. Contact the factory for additional information.

Connectors are manufactured by AMP.

On PC Board	787190-8
Suggested Plug	749111-7

Table 5.1: I/O Connector Model Numbers

Figure 5.1: Analog Input Connector

Pin	Connection	Pin	Connection
1	A_GND	26	A_GND
2	IN24/IN16+	27	IN32/IN16-
3	A_GND	28	A_GND
4	IN23/IN15+	29	IN31/IN15-
5	IN22/IN14+	30	IN30/IN14-
6	A_GND	31	A_GND
7	IN21/IN13+	32	IN29/IN13-
8	IN20/IN12+	33	IN28/IN12-
9	A_GND	34	A_GND
10	IN19/IN11+	35	IN27/IN11-
11	IN18/IN10+	36	IN26/IN10-
12	A_GND	37	A_GND
13	IN17/IN09+	38	IN25/IN09-
14	IN08/IN08+	39	IN16/IN08-
15	A_GND	40	A_GND
16	IN07/IN07+	41	IN15/IN07-
17	IN06/IN06+	42	IN14/IN06-
18	A_GND	43	A_GND
19	IN05/IN05+	44	IN13/IN05-
20	IN04/IN04+	45	IN12/IN04-
21	A_GND	46	A_GND
22	IN03/IN03+	47	IN11/IN03-
23	IN02/IN02+	48	IN10/IN02-
24	A_GND	49	A_GND
25	IN01/IN01+	50	IN09/IN01-

Anlog Input Connector P1

5.2 J4 CPCI BACKPLANE I/O CONNECTOR

Pin	Connection	Pin	Connection
1	3.3V	26	
2	IO_01	27	
3		28	
4	IO_14	29	IO_16
5	IO_08	30	
6	CS_DAB*	31	IO_02
7	EXGATE	32	EXTRIG
8	EX_DA	33	OUT_SCAN
9	IO_13	34	IO_15
10	IO_07	35	
11		36	
12		37	
13		38	
14		39	
15		40	3.3V
16		41	
17		42	
18		43	
19	3.3V	44	
20		45	
21		46	
22		47	
23	OUT4B	48	GNDA
24	GNDA	49	
25		50	

J4 CPCI Rear I/O Connector

Pin	Connection	Pin	Connection
51		76	+5
52		77	FP_PC1
53		78	
54		79	
55	IO_10	80	IO_12
56	IO_04	81	
57		82	
58		83	
59	IO_09	84	FP_PC0
60	IO_03	85	IO_11
61		86	
62		87	
63		88	
64		89	
65	3.3V	90	+5
66		91	
67		92	
68		93	
69		94	
70		95	
71		96	
72		97	
73		98	
74		99	OUT3B
75	OUT1B	100	GNDA

J4 CPCI Rear I/O Connector

Pin	Connection	Pin	Connection
101	+5	126	GND
102		127	GND
103		128	GND
104	FP_PC3	129	GND
105		130	GND
106	IO_06	131	GND
107		132	GND
108		133	GND
109	FP_PC2	134	GND
110		135	GND
111	IO_05	136	GND
112		137	GND
113		138	GND
114		139	GND
115	3.3V	140	GND
116		141	GND
117		142	GND
118		143	GND
119		144	GND
120		145	GND
121		146	GND
122		147	GND
123		148	GND
124	GNDA	149	GND
125	OUT2B	150	GND

J4 CPCI Rear I/O Connector

5.3 J5 CPCI BACKPLANE I/O CONNECTOR

Pin	Connection	Pin	Connection
1	3.3V	23	3.3V
2		24	
3		25	
4		26	
5		27	
6		28	
7	IN31/IN15-	29	IN23/IN15+
8	IN21/IN13+	30	IN30/IN14-
9	IN28/IN12-	31	IN20/IN12+
10	IN18/IN10+	32	
11		33	
12	3.3V	34	3.3V
13		35	
14		36	
15		37	
16		38	
17		39	
18	IN15/IN07-	40	IN07/IN07+
19	IN05/IN05+	41	IN14/IN06-
20	IN12/IN04-	42	IN04/IN04+
21	IN02/IN02+	43	
22		44	

J5 CPCI Rear I/O Connector

Pin	Connection	Pin	Connection
45	3.3V	67	+5
46		68	
47		69	
48		70	
49		71	
50		72	
51	IN32/IN16-	73	IN24/IN16+
52	IN22/IN14+	74	
53		75	
54		76	IN27/IN11-
55	IN25/IN09-	77	IN17/IN09+
56	3.3V	78	+5
57		79	
58		80	
59		81	
60		82	
61		83	
62	IN16/IN08-	84	IN08/IN08+
63	IN06/IN06+	85	
64		86	
65		87	IN11/IN03-
66	IN09/IN01-	88	IN01/IN01+

J5 CPCI Rear I/O Connector

Pin	Connection	Pin	Connection
89	+5	111	GND
90		112	GND
91		113	GND
92		114	GND
93		115	GND
94		116	GND
95		117	GND
96		118	GND
97	IN29/IN13-	119	GND
98	IN19/IN11+	120	GND
99	IN26/IN10-	121	GND
100	+5	122	GND
101		123	GND
102		124	GND
103		125	GND
104		126	GND
105		127	GND
106		128	GND
107		129	GND
108	IN13/IN05-	130	GND
109	IN03/IN03+	131	GND
110	IN10/IN02-	132	GND

J5 CPCI Rear I/O Connector

5.4 DAC OUTPUTS P2, P2, P3 and P4

IDC Header pins route the outputs of the DAC channels off the board.

5.5 EMULATOR CONNECTION (P11)

This connector is used to connect the emulator to the C31 DSP.

5.6 FACTORY USE (P10)

This connector is used at the factory for programming the FPGA.

5.7 RESERVED (P4, P5)

These connectors allow for a possible optional sample and hold board or filter board.

5.8 32 BIT CPCI BUS (J1)

This connector plugs into the backplane and provides the standard CPCI signals for all CPCI systems.

6. STANDALONE OPERATION

When the board is operated without a CPCI HOST, two signals must be driven in order to assure correct operation. These signals are provided by placing the correct jumpers on the board when in stand alone operation. If the board is returned to a PCI hosted environment, these jumpers must be removed, or they will interfere with the correct operation of the PCI host.

When the board is operated in stand alone mode, the board can by operated under an emulator. Changing the downloaded code in the FLASH will require returning to a hosted environment.

6.1 CPCI RESET

This signal must be pulled high by inserting a jumper in location W8 for stand alone operation. In a hosted environment, it must be removed.

6.2 CPCI BUS CLOCK

The AMCC requires that a CPCI BUS clock be present for its internal operation. This signal must be driven by the internal clock oscillator when operated in stand alone operation. This is accomplished by inserting a jumper in location W9 for stand alone operation. In a hosted environment, it must be removed.