# CPCI-Dual_IPC

**Intelligent IP CARRIER for *CPCI*™ systems**
**with Two TMS 320C31 DSPs**
**Up to Four IndustryPack® Modules**

## REFERENCE MANUAL

740-11-000-4000
Version 1.1
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Part Number : 740-11-000-4000 

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# 1. GENERAL DESCRIPTION

## 1.1 INTRODUCTION

The **CPCI-Dual_IPC** is a CPCI expansion card in a 6U form factor. The card is logically equivalent to two of ALPHI Technology's CPCI-IPC cards on a larger size card, with a DEC bridge chip to split the PCI bus. The **CPCI-Dual_IPC** provides mechanical support and the electrical interfaces for two single width IP modules, or a double width IP module for each logical CPCI-IPC. Multiple **CPCI-Dual_IPC** boards may be installed in a single system. The primary features of the **CPCI-Dual_IPC** are as follows:

- Logically and software equivalent to two CPCI-IPCs.
- Support for up to four IP modules (two per CPCI-IPC)
- 8 MHz or 32 MHz IP operation via jumper selection
- Dual on board DSP C31s at 32 MHz (one per CPCI-IPC) to offload I/O operation from host or for standalone applications
- Direct memory mapped access to the C31s from CPCI bus via AMCC 5933 PCI Chip
- Full interrupt support of host and DSP C31s
- Supports double-wide form factor IndustryPack®
- Front panel I/O connectors for all IPs

## 1.2 FUNCTIONAL DESCRIPTION

A functional block diagram of the **CPCI-Dual_IPC** is presented below in Figure 1-1. The jumper placement is depicted in Figure 1-2 and the connector placement in Figure 1-3. The **CPCI-Dual_IPC** can operate as a slave that is managed by the host processor on the CPCI bus or it can operate in a standalone mode of operation without a host. Each pair of IP modules share a common clock that can be jumpered for 8 or 32 MHz operation.

The **CPCI-Dual_IPC** is supported by ALPHI Technology under *Windows NT* by a **Board Support Package** which is supplied with the card. Other documentation supplied with the card will describe this support in full detail.

The card is also supported by a **DSP Support Library** providing the following features:

- Common access routines for communications with the HOST
- Mapping C language standard input and output by each of the DSPs to the onboard 8530 serial chips
- Identify the applicable card resources and parameters

All these are provided in a manner consistent across ALPHI Technology platforms. Other documentation supplied with the card will describe the support in full detail.

A bootloader provided on the card allows for control by the HOST and for independent operation in stand alone operation. User code can be downloaded to FLASH memory and booted automatically on reset. Access to the card can be made both by the HOST CPCI bus and serially through the 8530.

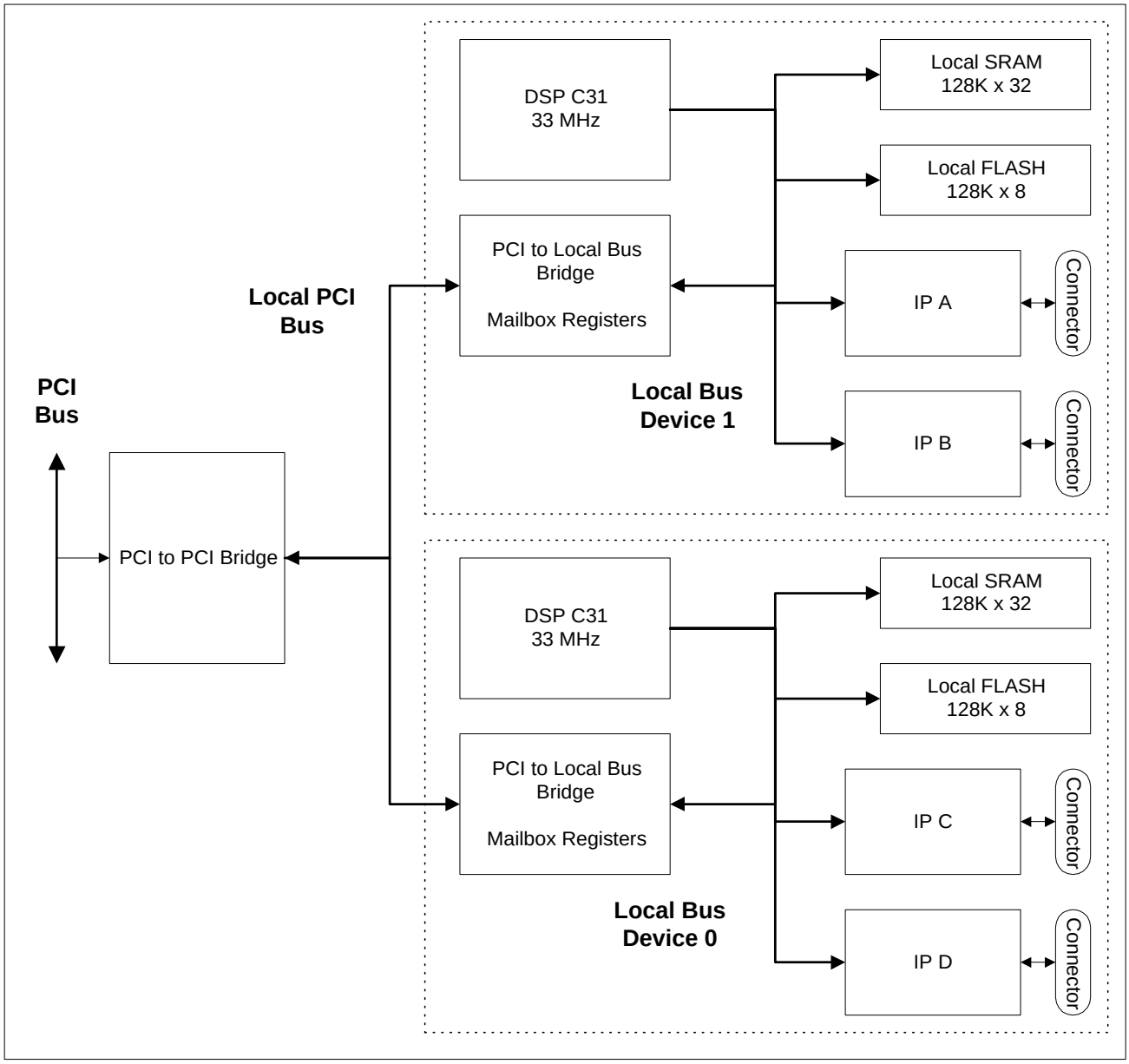


***Figure 1.1: Block Diagram***

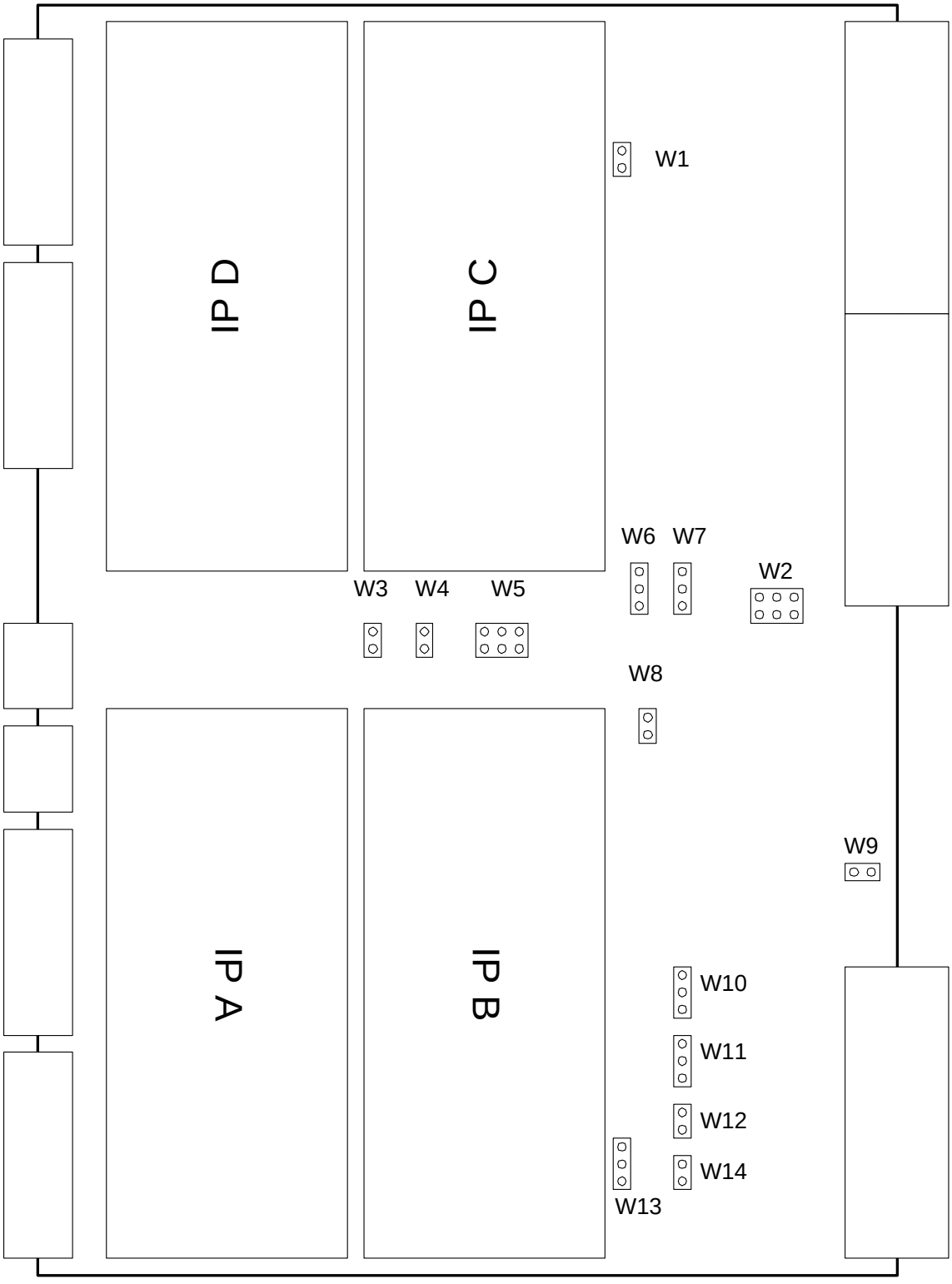


***Figure 1.2: Jumper Locations***

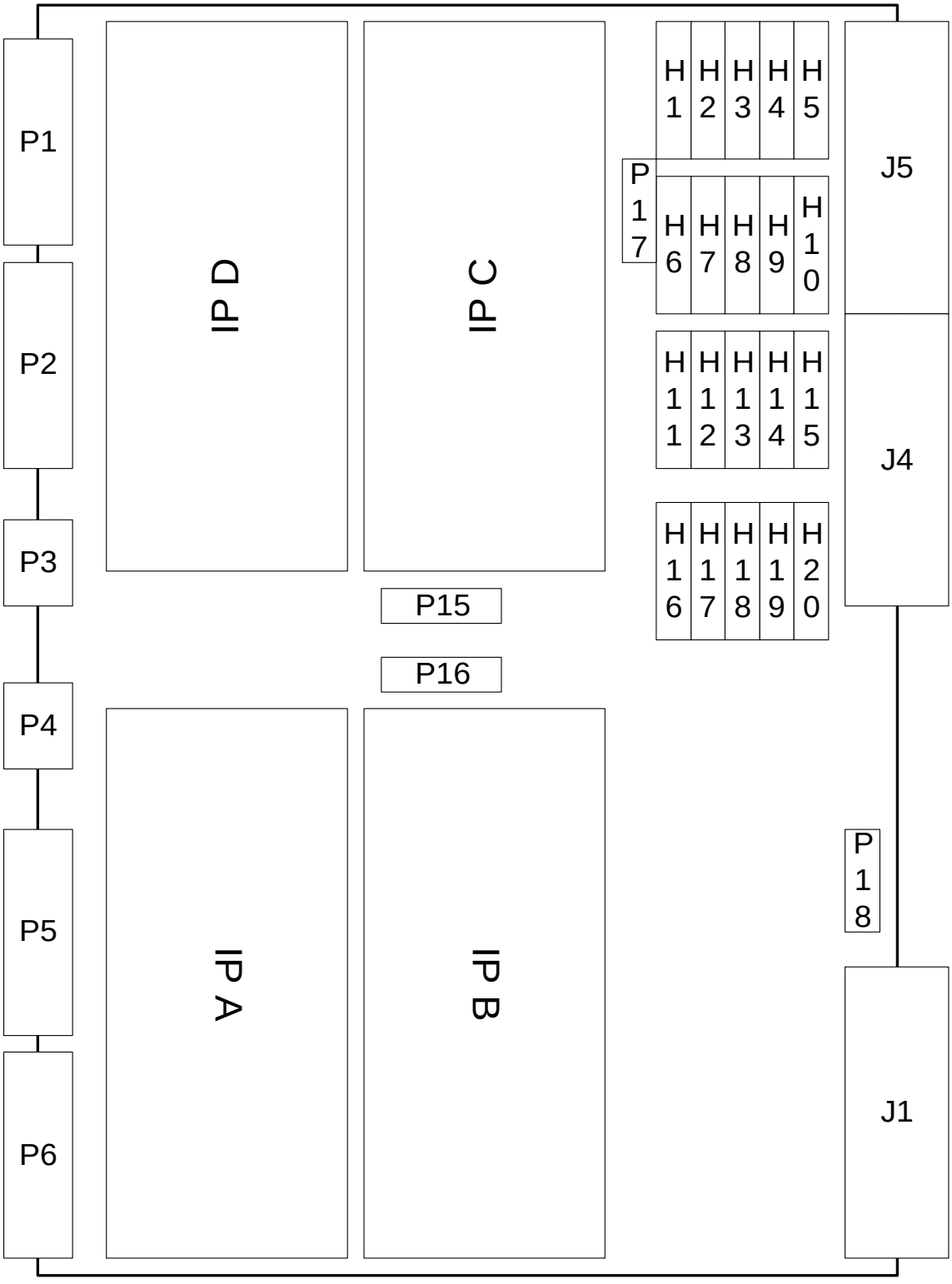


***Figure 1.3: Connector Locations***

## 1.3 REFERENCE MATERIALS LIST

The reader should refer to the PCI Local Bus Specification for a detailed explanation of the PCI bus architecture and timing requirements. This specification is available from the following source:

**PCI Special Interest Group**
**PO Box 14070**
**Portland, OR 97214**
**Tel: (800) 433-5177**
**Tel: (503) 797-4207**
**Fax: (503) 234-6762**

The reader is also referred to the S5933 PCI Controller data book:

**AMCC Applied Micro Circuits Corporation**
**6195 Lusk Boulevard**
**San Diego, CA 92121-2793**
**Tel: (800) 755-2622**
**http://www.amcc.com**

WindowsNT and Windows95 Programming Tools:

**BlueWater Systems**
**144 Railroad Ave. Suite #217**
**Edmonds, WA 98020**
**Tel: (206) 771-3610**
**Fax: (206) 771-2742**
**E-Mail: info@bluewatersystems.com**
**Web: http://www.bluewatersystems.com**

# 2. DUAL NATURE OF THE CPCI-Dual_IPC

This CPCI card consists of two completely separate logical CPCI-IPC units with separate PCI bridge chips. Because of this dual nature of the card, it is more logical to talk about one half at a time, and the remainder of this manual is written to reflect this nature.

# 3. HOST (CPCI) SIDE

## 3.1 CPCI CONFIGURATION REGISTERS

Each half of the card presents the following configuration values to the CPCI system, based on the values stored in the NVRAM device read by the AMCC PCI interface chip.

| Register | Value (Meaning) |
|---|---|
| Vendor ID | 0x13c5 (ALPHI Technology) |
| Device ID | 0x0203 (CPCI-Dual_IPC) |
| Revision ID | 0x00 |
| Class Code | 0xff0000 (Device does not fit into defined class codes) |
| Interrupt Line | 0xff |
| Interrupt Pin | A |
| Multifunction Device | No |
| Build In Self Test | No |
| Latency Timer | 0x00 |
| Minimum Grant | 0x00 |
| Maximum Latency | 0x00 |
| Expansion ROM Size | None |

***Table 3.1: PCI Configuration Registers***

## 3.2 CPCI BASE ADDRESS REGISTERS

Each half of the card requests base address regions from the CPCI system after RESET, based on the values stored in the NVRAM device read by the AMCC PCI interface chip.

The decode addresses of these regions are assigned by the host processor. Each half of the **CPCI-Dual_IPC** uses 1 of the 5 AMCC mapped base address registers. The AMCC is normally programmed at the factory to request the following resources from the CPCI BIOS:

| BAR | From | To | Description | Type |
|---|---|---|---|---|
| 0 | 0x00000000 | 0x00000003F | AMCC PCI Operation Registers | MEM |

***Table 3.2: Base Address and Use***

***NOTE: The AMCC has been programmed to request memory above 1 Mbytes.***

## 3.3 CPCI OPERATION REGISTERS

The host processor communicates with each half of the **CPCI-Dual_IPC** card via the AMCC pass-through interface. After the base address register has been programmed by the CPCI

configurator, incoming CPCI I/O or Memory cycles are used to access the registers of each AMCC chip. The PCI Operation Registers of the AMCC 5933 chip are depicted below:

| Offset | Register Name |
|---|---|
| 0x00 | OMB1 Outgoing Mailbox Register 1 |
| 0x04 | OMB2 Outgoing Mailbox Register 2 |
| 0x08 | OMB3 Outgoing Mailbox Register 3 |
| 0x0C | OMB4 Outgoing Mailbox Register 4 |
| 0x10 | IMB1 Incoming Mailbox Register 1 |
| 0x14 | IMB2 Incoming Mailbox Register 2 |
| 0x18 | IMB3 Incoming Mailbox Register 3 |
| 0x1C | IMB4 Incoming Mailbox Register 4 |
| 0x20 | FIFO Register Port (bi-directional) |
| 0x24 | MWAR Master Write Address Register |
| 0x28 | MWTC Master Write Transfer Counter |
| 0x2C | MRAR Master Read Address Register |
| 0x30 | MRTC Master Read Transfer Counter |
| 0x34 | MBEF Mailbox Empty/Full Status |
| 0x38 | INTCSR Interrupt Control/Status Register |
| 0x3C | MCSR Bus Master Control/Status Register |

***Table 3.2: AMCC Registers (HOST)***

For more information about these registers refer to the AMCC PCI controller manual.

# 4. C31 SIDE

## 4.1 INTERNAL ORGANIZATION

Each half of the **CPCI-Dual_IPC** card is divided into different sections. Each section and its relationship to other sections will be discussed. The **CPCI-Dual_IPC** sections are:

- CPCI interface
- IP interface

## 4.2 CPCI INTERFACE

The local DSP processor communicates with the CPCI bus through the AMCCS9533 chip that provides bi-directional FIFO and Mailbox registers. Each half of the **CPCI-Dual_IPC** can function as both a servant (CPCI target) or as a master (CPCI initiator) for DMA access. The following interface descriptions refer to the CPCI interface as seen by the local DSP. The AMCC registers are located at DSP address 0xf00080.

### 4.2.1 BI-DIRECTIONAL FIFO

Two separate FIFO data paths are implemented within the AMCCS9533, a read FIFO that allows data transfers from the module to the CPCI bus and a write FIFO that transfers data from the CPCI to the module. Size of the FIFO is 32 bit X 8. Read and write DMA access to the host can occur via the FIFO registers if it is supported by the software on the HOST and

is enabled. Alternatively, the FIFO registers can utilize a polled scheme on the HOST and DSP. Both FIFOs are accessed via access to the same location as seen by the DSP, offset 0x08.

### 4.2.2 MAILBOX REGISTERS

The Mailbox registers of the AMCCS9533 provide a bi-directional data path that can be used to send data or software control information between the HOST and DSP of that half of the **CPCI-Dual_IPC** module. Interrupts can be enabled based on a specific mailbox event. There are 4 incoming mailboxes and 4 outgoing mailboxes. Each mailbox is 32 bits wide. The address offsets for the mailboxes are shown below in Table 3-1.

### 4.2.3 ADDITIONAL REGISTERS

The AMCC S5933 PCI controller has a set of additional registers to control and monitor the behavior of the CPCI interface.

The address offsets of these registers are shown below in Table 3-1.

| Offset | Register Name |
|---|---|
| 0x00 | Incoming Mailbox Reg 1 |
| 0x01 | Incoming Mailbox Reg 2 |
| 0x02 | Incoming Mailbox Reg 3 |
| 0x03 | Incoming Mailbox Reg 4 |
| 0x04 | Outgoing Mailbox Reg 1 |
| 0x05 | Outgoing Mailbox Reg 2 |
| 0x06 | Outgoing Mailbox Reg 3 |
| 0x07 | Outgoing Mailbox Reg 4 |
| 0x08 | Add-on FIFO port |
| 0x09 | Bus master write Address Register |
| 0x0A | Add-on Pass through Address |
| 0x0B | Add-on Pass trough Data |
| 0x0C | Bus master read Address Register |
| 0x0D | Add-on Mailbox Empty/full Status |
| 0x0E | Add-on Interrupt Control |
| 0x0F | Add-on General Control/Status Register |

***Table 4.1: AMCC Registers (DSP)***

For more information about these registers refer to the AMCC PCI controller manual.

## 4.3 IP INTERFACE and PAGED MEMORY

The ID and IO space for the IPs are directly accessed based on the memory map below. IP memory space is overlaid with the FLASH space, and is controlled via the register CTRL.

Recall that there are only two IPs accessible by each DSP in that half of the card.

## 4.4 DSP MEMORY AND REGISTER MAP SUMMARY

| NAME | START | END | DATA | R/W | COMMENTS |
|---|---|---|---|---|---|
| SRAM | 0x000000 | 0x01FFFF | D00-D31 | R/W | Zero wait state static RAM |
| FLASH | 0x400000 | 0x47FFFF | D00-D07 | R/W | 512K x 8 |
| IPMEMSL_A | 0x400000 | 0x7FFFFF | D00-D15 | R/W | IP_A memory ( 8 Mbytes ) |
| IPMEMSL_B | 0x400000 | 0x7FFFFF | D00-D15 | R/W | IP_B memory ( 8 Mbytes ) |
| CTR | 0xF00010 | 0xF00010 | D00-D03 | W | Controls internal settings |
| INTGNT_A | 0xF00020 | 0xF00021 | D00-D15 | R | Interrupt vectors from IP_A |
| INTGNT_B | 0xF00022 | 0xF00023 | D00-D15 | R | Interrupt vector from IP_B |
| C31_STAT | 0xF00028 | 0xF00028 | D00-D04 | R | IP interrupt; Bus Error |
| BERR_RST | 0xF00030 | 0xF00030 | N/A | W | Reset Bus Error Status |
| IPSTROBE | 0xF00038 | 0xF00038 | N/A | W | Assert *IPSTROBE |
| SCC8530 | 0xF00048 | 0xF0004C | D00-D07 | R/W | Serial communication port |
| AMCC | 0xF00080 | 0xF000FF | D00-D31 | R/W | AMCC REGISTERS |
| IOSEL_A | 0xF00200 | 0xF0023F | D00-D15 | R/W | IP_A I/O Space |
| IOSEL_B | 0xF00240 | 0xF0027F | D00-D15 | R/W | IP_B I/O Space |
| IDSEL_A | 0xF00280 | 0xF002BF | D00-D15 | R/W | IP_A ID Space |
| IDSEL_B | 0xF002C0 | 0xF002FF | D00-D15 | R/W | IP_B ID Space |

***Table 4.2: DSP Memory Map***

### 4.4.1 CTRL (Write Only)

| BIT 07 | BIT 06 | BIT 05 | BIT 04 | BIT 03 | BIT 02 | BIT 01 | BIT 00 |
|---|---|---|---|---|---|---|---|
| | | | | TCLK1_EN | BANKSEL | 32BIT_AB | FLASH |

***TCLK1_EN Signal routing to IPSTROBE***

See the following table for routing signals to *IPSTROBE.

| TCLK1_EN, | Result |
|---|---|
| 0 | Connect DSP Timer 1 output to *IPSTROBE |
| 1 | Software writes to register IPSTROBE (0xF00038) output to *IPSTROBE |

***IPMEM, BANKSEL Memory Page Selection***

The FLASH and the two IP memory spaces are all paged into a common DSP address range starting at 0x400000. Selection of the appropriate page is accomplished by programming the FLASH and BANKSEL bits.

| BANKSEL | FLASH | Page Selection |
|---|---|---|
| X | 0 | FLASH (default) |
| 0 | 1 | IP_A Memory Space |
| 1 | 1 | IP_B Memory Space |

**Table 4-3: Memory Page Selection**

***32BIT_AB 32-bit Width Enable***

Setting this bit to a one enables the IP interface A and B for 32-bit transfers. Setting this bit to a zero disables the 32-bit transfers (default setting). This bit must be set to a one when using a double width IP. Note that the DSP always reads or writes in 32-bits, however only the lower 16 bits are valid when 32BIT_AB = 0.

### 4.4.2 C31_STAT INTERRUPT STATUS REGISTER (Read Only)

| BIT 07 | BIT 06 | BIT 05 | BIT 04 | BIT 03 | BIT 02 | BIT 01 | BIT 00 |
|---|---|---|---|---|---|---|---|
| | | | CBERR | IP_B IREQ1 | IP_B IREQ0 | IP_A IREQ1 | IP_A IREQ0 |

Each IP module can generate two different interrupts. When any Industry Pack generates an interrupt, the corresponding interrupt is ORed with other pending interrupts. The DSP can read this register to determine which interrupts are pending.

***CBERR Bus Error Status***

Any access to a non-existent IP will never complete since no device will assert *IPACK.

To prevent this from happening, and hanging the DSP, any access to an IP also starts a timer to ensure that the cycle completes. The fact that a cycle has timed out has occurred is reported in **C31_STAT**, and can be cleared by writing to **BERR_RST**.

The DSP C31 can read this bit to know that a access to an IP has not responded by asserting *IPACK. This status is reset with a write to **BERR_RST**.

This event will also cause a DSP interrupt, so any DSP interrupt routine which hooks the 8530 interrupt should be prepared to handle it (by at least writing to **BERR_RST**).

### 4.4.3 BERR_RST (Write Strobe Only)

A write to this location will reset the CBERR bit in the **C31_STAT** register.

### 4.4.4 IPSTROBE (Write Strobe Only)

If the **CTRL** Register is configured to allow it, a write to this location will trigger a pulse on the *IPSTROBE line to all the IPs.

### 4.4.5 SERIAL PORT (Read / Write)

The DSP processor on each half of the **CPCI-Dual_IPC** has access to its own SCC85C30 serial communication controller. The 8530 provides an RS232C asynchronous serial communication port. Port B of the 8530 is not connected.

The bootloader and hardware support libraries supplied with the **CPCI-Dual_IPC** utilizes the RS232C port for a console for standard input and output by the DSP. The customer may alternatively wish to write his own software to use this port. Examples are provided in the **Board Support Package**.

## 4.5 RESET SIGNALS

Each half of the **CPCI-Dual_IPC** can be reset from two different sources:

- At power on or when the PCI RESET is asserted, the watchdog timer will hold the C31 RESET line and the IP reset lines low for 200 ms.
- Each AMCC has a bit called SYSRST which the HOST can toggle to reset that DSP and IP resets. Software should hold the RESET asserted for 200 mS to meet the IP specifications

## 4.6 LOCAL DSP INTERRUPT SOURCES

Each of the local DSPs has four interrupt lines. The source of each interrupt is listed in the table below. Additionally, at reset, the INT1 line is pulsed to tell the C31 to find the FLASH image at 0x400000 (if boot mode is MC).

| SOURCE | ENABLE SIGNAL | INTERRUPT LEVEL |
|---|---|---|
| SCC8530 | Inside SCC8530 | INT0 |
| Bus Error | None | INT0 |
| AMCC | Inside 5933 | INT1 |
| AMCC FIFO:<br>WR not Full<br>RD not Empty | None | INT2 |
| IP interrupt | None | INT3 |

***Table 4-4: Interrupt Sources***

## 5. LED INDICATORS

There are eight LED indicators visible at the CPCI card bracket. They are marked with a legend on the bracket. Four LEDs apply to each half of the board.

The LEDs have the following meanings:

| LEGEND | Meaning | LEGEND | Meaning |
|---|---|---|---|
| B2 | DSP is accessing IP B. | A2 | DSP is accessing IP A. |
| R2 | DSP is reading a register in the AMCC. | W2 | DSP is writing a register in the AMCC. |
| R1 | DSP is reading a register in the AMCC. | W1 | DSP is writing a register in the AMCC. |
| B1 | DSP is accessing IP B. | A1 | DSP is accessing IP A. |

***Table 5.1 LED Descriptions***

## 6. JUMPER DESCRIPTIONS

### 6.1 FIRST HALF (Device 0)

| JUMPER | FACTORY SETTING | DESCRIPTION |
|---|---|---|
| W3 | None | DSP Boot Mode: MC/~MP. The DSP's boot mechanism is designed to operate in MC mode, booting from the FLASH. |
| W5 | None | Available to user for software configuration. The state is available in C31_STAT. |
| W7 | 2-3 | IP A, B Clock Speed. 1-2 for 32 MHz, 2-3 for 8 MHz. 8 MHz is default. |
| W9 | None | When shorted, provides DSP and IP reset. |

***Table 6.1 Jumper Descriptions for Device 0***

### 6.2 SECOND HALF (Device 1)

| JUMPER | FACTORY SETTING | DESCRIPTION |
|---|---|---|
| W1 | None | When shorted, provides DSP and IP reset. |
| W2 | None | Available to user for software configuration. The state is available in C31_STAT. |
| W4 | None | DSP Boot Mode: MC/~MP. The DSP's boot mechanism is designed to operate in MC mode, booting from the FLASH. |
| W6 | 2-3 | IP A, B Clock Speed. 1-2 for 32 MHz, 2-3 for 8 MHz. 8 MHz is default. |

***Table 6.2 Jumper Descriptions for Device 1***

### 6.3 GLOBAL

| JUMPER | FACTORY SETTING | DESCRIPTION |
|---|---|---|
| W8 | 1-2 | Shorted when DSP operates at 32 MHz and U43 not installed; not when U43 installed for custom DSP frequency. |
| W10 | 2-3 | Must be connected for correct operation. |
| W11 | 2-3 | Must be connected for correct operation. |
| W12 | None | If installed, connects 32 MHz clock to PCI clock for stand alone operation and access to AMCC. Hosted operation is default. |
| W13 | None | Must not be connected for correct operation. |
| W14 | None | If installed, forces PCI reset high for stand alone operation. Hosted operation is default. |

***Table 6.2 Jumper Descriptions***

## 7. CONNECTIONS

### 7.1 IP I/O CONNECTORS (P1, P2, P5, P6)

| Connector | Label on PCB | Device | Software |
|---|---|---|---|
| P6 | IP_A | Device 0 | IP_A |
| P5 | IP_B | Device 0 | IP_B |
| P2 | IP_C | Device 1 | IP_A |
| P1 | IP_D | Device 1 | IP_B |

50 pin subminiature D shelled connectors are used to route all the IP I/O signals off the card. ALPHI Technology can supply transition modules and cable assemblies to meet any special requirements. Contact the factory for additional information.

Connectors are manufactured by AMP and the style is CHAMP.

| Use | Model |
|---|---|
| On PC Board | 787096-1 |
| Suggested Plug | 787131-1 |
| Suggested Shell | 787133-2 |

***Table 7.1: I/O Connector Model Numbers***

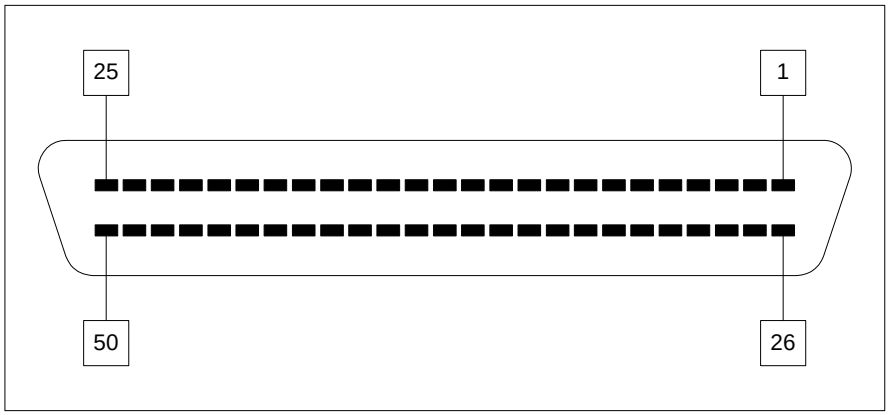


***Figure 7.1: IP I/O CONNECTORS***

The I/O signals for all four IPs are directly routed off the card through the front panel.

## 7.2 SERIAL RS232 PORT (P3, P4)

| Connector | Device |
|---|---|
| P4 | Device 0 |
| P3 | Device 1 |

A 9 pin subminiature D shelled connector is used to route both RS232 signals off the card. Port A of both 8530s are configured as RS232 ports, and they serve as the console output for the bootloader and any DSP programs linked with the ALPHI_IO.LIB library discussed in the **DSP Support Library**.

Connectors are manufactured by ITT Cannon.

| Use | Model |
|---|---|
| On PC Board | MDSM-9PE-C10 |
| Suggested Plug | MDSM-9SC-Z11 |

***Table 7.2: Serial Connector Model Numbers***

The pinout is described in the table below.

| Pin | Description | Pin | Description |
|---|---|---|---|
| 1 | No Connection | 2 | Transmit Data |
| 3 | Receive Data | 4 | Clear To Send |
| 5 | Ground | 6 | Request To Send |
| 7 | Ground | 8 | No Connection |
| 9 | No Connection | | |

***Table 7.3: Serial RS232 Port (P4)***

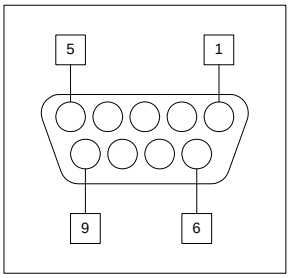


***Figure 7.2: Serial RS232 Port (P4)***

## 7.3 EMULATOR CONNECTION (P15, P16)

| Connector | Device |
|---|---|
| P16 | Device 0 |
| P15 | Device 1 |

This connector is used to connect the emulator to the C31 DSP. It follows the standard form as described by TI in their processor manual.

## 7.4 FACTORY USE (P17, P18)

This connector is used at the factory for programming the FPGA.

## 7.5 32 BIT CPCI BUS (J1)

This connector plugs into the backplane and provides the standard CPCI signals for all CPCI systems.

## 7.6 Backplane I/O Connections (J4 and J5)

The board is designed to optionally output the I/O lines from the IPs out the back panel if desired by the customer. By installing jumper blocks on the 20 headers H1 – H20, the IP I/O lines are connected to J4 and J5. Alternatively, the customer can wirewrap a custom pinout if desired.

| IP I/O Line | Header and Pin | Header and Pin | Backplane and Pin |
|---|---|---|---|
| IP_A:1 | H20:19 | H20:20 | J4:11 |
| IP_A:2 | H19:19 | H19:20 | J4:36 |
| IP_A:3 | H18:19 | H18:20 | J4:61 |
| IP_A:4 | H17:19 | H17:20 | J4:86 |
| IP_A:5 | H16:19 | H16:20 | J4:111 |
| IP_A:6 | H20:17 | H20:18 | J4:10 |
| IP_A:7 | H19:17 | H19:18 | J4:35 |
| IP_A:8 | H18:17 | H18:18 | J4:60 |
| IP_A:9 | H17:17 | H17:18 | J4:85 |
| IP_A:10 | H16:17 | H16:18 | J4:110 |
| IP_A:11 | H20:15 | H20:16 | J4:9 |
| IP_A:12 | H19:15 | H19:16 | J4:34 |
| IP_A:13 | H18:15 | H18:16 | J4:59 |
| IP_A:14 | H17:15 | H17:16 | J4:84 |
| IP_A:15 | H16:15 | H16:16 | J4:109 |
| IP_A:16 | H20:13 | H20:14 | J4:8 |
| IP_A:17 | H19:13 | H19:14 | J4:33 |
| IP_A:18 | H18:13 | H18:14 | J4:58 |
| IP_A:19 | H17:13 | H17:14 | J4:83 |
| IP_A:20 | H16:13 | H16:14 | J4:108 |
| IP_A:21 | H20:11 | H20:12 | J4:7 |
| IP_A:22 | H19:11 | H19:12 | J4:32 |
| IP_A:23 | H18:11 | H18:12 | J4:57 |
| IP_A:24 | H17:11 | H17:12 | J4:82 |
| IP_A:25 | H16:11 | H16:12 | J4:107 |
| IP_A:26 | H20:9 | H20:10 | J4:6 |
| IP_A:27 | H19:9 | H19:10 | J4:31 |
| IP_A:28 | H18:9 | H18:10 | J4:56 |
| IP_A:29 | H17:9 | H17:10 | J4:81 |
| IP_A:30 | H16:9 | H16:10 | J4:106 |
| IP_A:31 | H20:7 | H20:8 | J4:5 |
| IP_A:32 | H19:7 | H19:8 | J4:30 |
| IP_A:33 | H18:7 | H18:8 | J4:55 |
| IP_A:34 | H17:7 | H17:8 | J4:80 |
| IP_A:35 | H16:7 | H16:8 | J4:105 |
| IP_A:36 | H20:5 | H20:6 | J4:4 |
| IP_A:37 | H19:5 | H19:6 | J4:29 |
| IP_A:38 | H18:5 | H18:6 | J4:54 |
| IP_A:39 | H17:5 | H17:6 | J4:79 |
| IP_A:40 | H16:5 | H16:6 | J4:104 |
| IP_A:41 | H20:3 | H20:4 | J4:3 |
| IP_A:42 | H19:3 | H19:4 | J4:28 |
| IP_A:43 | H18:3 | H18:4 | J4:53 |
| IP_A:44 | H17:3 | H17:4 | J4:78 |
| IP_A:45 | H16:3 | H16:4 | J4:103 |
| IP_A:46 | H20:1 | H20:2 | J4:2 |
| IP_A:47 | H19:1 | H19:2 | J4:27 |
| IP_A:48 | H18:1 | H18:2 | J4:52 |
| IP_A:49 | H17:1 | H17:2 | J4:77 |
| IP_A:50 | H16:1 | H16:2 | J4:102 |

| IP I/O Line | Header and Pin | Header and Pin | Backplane and Pin |
|---|---|---|---|
| IP_B:1 | H15:19 | H15:20 | J4:25 |
| IP_B:2 | H14:19 | H14:20 | J4:50 |
| IP_B:3 | H13:19 | H13:20 | J4:75 |
| IP_B:4 | H12:19 | H12:20 | J4:100 |
| IP_B:5 | H11:19 | H11:20 | J4:125 |
| IP_B:6 | H15:17 | H15:18 | J4:24 |
| IP_B:7 | H14:17 | H14:18 | J4:49 |
| IP_B:8 | H13:17 | H13:18 | J4:74 |
| IP_B:9 | H12:17 | H12:18 | J4:99 |
| IP_B:10 | H11:17 | H11:18 | J4:124 |
| IP_B:11 | H15:15 | H15:16 | J4:23 |
| IP_B:12 | H14:15 | H14:16 | J4:48 |
| IP_B:13 | H13:15 | H13:16 | J4:73 |
| IP_B:14 | H12:15 | H12:16 | J4:98 |
| IP_B:15 | H11:15 | H11:16 | J4:123 |
| IP_B:16 | H15:13 | H15:14 | J4:22 |
| IP_B:17 | H14:13 | H14:14 | J4:47 |
| IP_B:18 | H13:13 | H13:14 | J4:72 |
| IP_B:19 | H12:13 | H12:14 | J4:97 |
| IP_B:20 | H11:13 | H11:14 | J4:122 |
| IP_B:21 | H15:11 | H15:12 | J4:21 |
| IP_B:22 | H14:11 | H14:12 | J4:46 |
| IP_B:23 | H13:11 | H13:12 | J4:71 |
| IP_B:24 | H12:11 | H12:12 | J4:96 |
| IP_B:25 | H11:11 | H11:12 | J4:121 |
| IP_B:26 | H15:9 | H15:10 | J4:20 |
| IP_B:27 | H14:9 | H14:10 | J4:45 |
| IP_B:28 | H13:9 | H13:10 | J4:70 |
| IP_B:29 | H12:9 | H12:10 | J4:95 |
| IP_B:30 | H11:9 | H11:10 | J4:120 |
| IP_B:31 | H15:7 | H15:8 | J4:19 |
| IP_B:32 | H14:7 | H14:8 | J4:44 |
| IP_B:33 | H13:7 | H13:8 | J4:69 |
| IP_B:34 | H12:7 | H12:8 | J4:94 |
| IP_B:35 | H11:7 | H11:8 | J4:119 |
| IP_B:36 | H15:5 | H15:6 | J4:18 |
| IP_B:37 | H14:5 | H14:6 | J4:43 |
| IP_B:38 | H13:5 | H13:6 | J4:68 |
| IP_B:39 | H12:5 | H12:6 | J4:93 |
| IP_B:40 | H11:5 | H11:6 | J4:118 |
| IP_B:41 | H15:3 | H15:4 | J4:17 |
| IP_B:42 | H14:3 | H14:4 | J4:42 |
| IP_B:43 | H13:3 | H13:4 | J4:67 |
| IP_B:44 | H12:3 | H12:4 | J4:92 |
| IP_B:45 | H11:3 | H11:4 | J4:117 |
| IP_B:46 | H15:1 | H15:2 | J4:16 |
| IP_B:47 | H14:1 | H14:2 | J4:41 |
| IP_B:48 | H13:1 | H13:2 | J4:66 |
| IP_B:49 | H12:1 | H12:2 | J4:91 |
| IP_B:50 | H11:1 | H11:2 | J4:116 |

| IP I/O Line | Header and Pin | Header and Pin | Backplane and Pin |
|---|---|---|---|
| IP_C:1 | H10:19 | H10:20 | J5:11 |
| IP_C:2 | H9:19 | H9:20 | J5:33 |
| IP_C:3 | H8:19 | H8:20 | J5:55 |
| IP_C:4 | H7:19 | H7:20 | J5:77 |
| IP_C:5 | H6:19 | H6:20 | J5:99 |
| IP_C:6 | H10:17 | H10:18 | J5:10 |
| IP_C:7 | H9:17 | H9:18 | J5:32 |
| IP_C:8 | H8:17 | H8:18 | J5:54 |
| IP_C:9 | H7:17 | H7:18 | J5:76 |
| IP_C:10 | H6:17 | H6:18 | J5:98 |
| IP_C:11 | H10:15 | H10:16 | J5:9 |
| IP_C:12 | H9:15 | H9:16 | J5:31 |
| IP_C:13 | H8:15 | H8:16 | J5:53 |
| IP_C:14 | H7:15 | H7:16 | J5:75 |
| IP_C:15 | H6:15 | H6:16 | J5:97 |
| IP_C:16 | H10:13 | H10:14 | J5:8 |
| IP_C:17 | H9:13 | H9:14 | J5:30 |
| IP_C:18 | H8:13 | H8:14 | J5:52 |
| IP_C:19 | H7:13 | H7:14 | J5:74 |
| IP_C:20 | H6:13 | H6:14 | J5:96 |
| IP_C:21 | H10:11 | H10:12 | J5:7 |
| IP_C:22 | H9:11 | H9:12 | J5:29 |
| IP_C:23 | H8:11 | H8:12 | J5:51 |
| IP_C:24 | H7:11 | H7:12 | J5:73 |
| IP_C:25 | H6:11 | H6:12 | J5:95 |
| IP_C:26 | H10:9 | H10:10 | J5:6 |
| IP_C:27 | H9:9 | H9:10 | J5:28 |
| IP_C:28 | H8:9 | H8:10 | J5:50 |
| IP_C:29 | H7:9 | H7:10 | J5:72 |
| IP_C:30 | H6:9 | H6:10 | J5:94 |
| IP_C:31 | H10:7 | H10:8 | J5:5 |
| IP_C:32 | H9:7 | H9:8 | J5:27 |
| IP_C:33 | H8:7 | H8:8 | J5:49 |
| IP_C:34 | H7:7 | H7:8 | J5:71 |
| IP_C:35 | H6:7 | H6:8 | J5:93 |
| IP_C:36 | H10:5 | H10:6 | J5:4 |
| IP_C:37 | H9:5 | H9:6 | J5:26 |
| IP_C:38 | H8:5 | H8:6 | J5:48 |
| IP_C:39 | H7:5 | H7:6 | J5:70 |
| IP_C:40 | H6:5 | H6:6 | J5:92 |
| IP_C:41 | H10:3 | H10:4 | J5:3 |
| IP_C:42 | H9:3 | H9:4 | J5:25 |
| IP_C:43 | H8:3 | H8:4 | J5:47 |
| IP_C:44 | H7:3 | H7:4 | J5:69 |
| IP_C:45 | H6:3 | H6:4 | J5:91 |
| IP_C:46 | H10:1 | H10:2 | J5:2 |
| IP_C:47 | H9:1 | H9:2 | J5:24 |
| IP_C:48 | H8:1 | H8:2 | J5:46 |
| IP_C:49 | H7:1 | H7:2 | J5:68 |
| IP_C:50 | H6:1 | H6:2 | J5:90 |

| IP I/O Line | Header and Pin | Header and Pin | Backplane and Pin |
|---|---|---|---|
| IP_D:1 | H5:19 | H5:20 | J5:22 |
| IP_D:2 | H4:19 | H4:20 | J5:44 |
| IP_D:3 | H3:19 | H3:20 | J5:66 |
| IP_D:4 | H2:19 | H2:20 | J5:88 |
| IP_D:5 | H1:19 | H1:20 | J5:110 |
| IP_D:6 | H5:17 | H5:18 | J5:21 |
| IP_D:7 | H4:17 | H4:18 | J5:43 |
| IP_D:8 | H3:17 | H3:18 | J5:65 |
| IP_D:9 | H2:17 | H2:18 | J5:87 |
| IP_D:10 | H1:17 | H1:18 | J5:109 |
| IP_D:11 | H5:15 | H5:16 | J5:20 |
| IP_D:12 | H4:15 | H4:16 | J5:42 |
| IP_D:13 | H3:15 | H3:16 | J5:64 |
| IP_D:14 | H2:15 | H2:16 | J5:86 |
| IP_D:15 | H1:15 | H1:16 | J5:108 |
| IP_D:16 | H5:13 | H5:14 | J5:19 |
| IP_D:17 | H4:13 | H4:14 | J5:41 |
| IP_D:18 | H3:13 | H3:14 | J5:63 |
| IP_D:19 | H2:13 | H2:14 | J5:85 |
| IP_D:20 | H1:13 | H1:14 | J5:107 |
| IP_D:21 | H5:11 | H5:12 | J5:18 |
| IP_D:22 | H4:11 | H4:12 | J5:40 |
| IP_D:23 | H3:11 | H3:12 | J5:62 |
| IP_D:24 | H2:11 | H2:12 | J5:84 |
| IP_D:25 | H1:11 | H1:12 | J5:106 |
| IP_D:26 | H5:9 | H5:10 | J5:17 |
| IP_D:27 | H4:9 | H4:10 | J5:39 |
| IP_D:28 | H3:9 | H3:10 | J5:61 |
| IP_D:29 | H2:9 | H2:10 | J5:83 |
| IP_D:30 | H1:9 | H1:10 | J5:105 |
| IP_D:31 | H5:7 | H5:8 | J5:16 |
| IP_D:32 | H4:7 | H4:8 | J5:38 |
| IP_D:33 | H3:7 | H3:8 | J5:60 |
| IP_D:34 | H2:7 | H2:8 | J5:82 |
| IP_D:35 | H1:7 | H1:8 | J5:104 |
| IP_D:36 | H5:5 | H5:6 | J5:15 |
| IP_D:37 | H4:5 | H4:6 | J5:37 |
| IP_D:38 | H3:5 | H3:6 | J5:59 |
| IP_D:39 | H2:5 | H2:6 | J5:81 |
| IP_D:40 | H1:5 | H1:6 | J5:103 |
| IP_D:41 | H5:3 | H5:4 | J5:14 |
| IP_D:42 | H4:3 | H4:4 | J5:36 |
| IP_D:43 | H3:3 | H3:4 | J5:58 |
| IP_D:44 | H2:3 | H2:4 | J5:80 |
| IP_D:45 | H1:3 | H1:4 | J5:102 |
| IP_D:46 | H5:1 | H5:2 | J5:13 |
| IP_D:47 | H4:1 | H4:2 | J5:35 |
| IP_D:48 | H3:1 | H3:2 | J5:57 |
| IP_D:49 | H2:1 | H2:2 | J5:79 |
| IP_D:50 | H1:1 | H1:2 | J5:101 |

## 8. STANDALONE OPERATION

When the board is operated without a CPCI HOST, two signals must be driven in order to assure correct operation. These signals are provided by placing the correct jumpers on the board when in stand alone operation. If the board is returned to a PCI hosted environment, these jumpers must be removed, or they will interfere with the correct operation of the PCI host.

When the board is operated in stand alone mode, the board can by operated under an emulator and by downloading and executing programs via the serial port under control of the bootloader.

### 8.1 CPCI RESET

This signal must be pulled high by inserting a jumper in location W14 for stand alone operation. In a hosted environment, it must be removed.

### 8.2 CPCI BUS CLOCK

The AMCC requires that a CPCI BUS clock be present for its internal operation. This signal must be driven by the internal clock oscillator when operated in stand alone operation. This is accomplished by inserting a jumper in location W12 for stand alone operation. In a hosted environment, it must be removed.