CPCI-AD16

Intelligent DSP Based
16 Channel 16 Bit A/D Converter Board
for 3U *CompactPCI*™ systems

REFERENCE MANUAL

717-20-000-4000
Version 2.0
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Part Number : 717-20-000-4000

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1. GENERAL DESCRIPTION

1.1 INTRODUCTION

The **CPCI-AD16** is an intelligent DSP based high performance analog data acquisition system for 3U CompactPCI applications. The **CPCI-AD16** acquires 16 single-ended or differential channels with 16 bits of resolution at a sampling rate of 12.5 kHz per channel, or fewer channels at up to a maximum of 100 kHz. The local DSP processor can acquire and store data samples, and optionally perform any preprocessing necessary for customer applications. An optional low-pass filter module can simplify the design of any system that requires Nyquist filtering or sample and hold before the A/D converters. Multiple **CPCI-AD16** boards may be installed in a single system. The primary features of the **CPCI-AD16** are as follows:

- 16 analog input channels configurable for single ended or differential mode.
- Individual instrumentation amplifiers for each input, with digitally programmable gain.
- Two 16 bit 10 μS A/D converters, each multiplexed to 8 inputs.
- Integrated DSP (TI TMS320C31) at 32 MHz to offload I/O operation from host.
- 128K x 32-bit zero wait state static RAM.
- 128K x 8 bit FLASH ROM for storing DSP program.
- Direct memory mapped control of DSP from CPCI bus via AMCC 5933 PCI Chip.
- Full interrupt support of host and DSP.
- Front panel I/O connectors for all signals.
- External or internal sampling clock.
- External or internal power supply.

1.2 FUNCTIONAL DESCRIPTION

A functional block diagram of the **CPCI-AD16** is presented below in Figure 1-1. The jumper placement and the connector placement is depicted in Figure 1-2. The **CPCI-AD16** operates as a slave that is managed by the host processor on the CPCI bus.

The **CPCI-AD16** is supported by ALPHI Technology under *Windows NT* by a **Board Support Package** which is supplied with the card. Other documentation supplied with the card will describe this support in full detail.

The card is also supported by a **DSP Support Library** providing the following features:

- Common access routines for communications with the HOST
- Identify the applicable card resources and parameters

These are provided in a manner consistent across ALPHI Technology platforms. Other documentation supplied with the card will describe the support in full detail.

A bootloader provided on the card allows for control by the HOST and for automatically loading custom application code. User code can be downloaded to FLASH memory and booted automatically on reset. Access to the card can be made by the HOST CPCI bus.

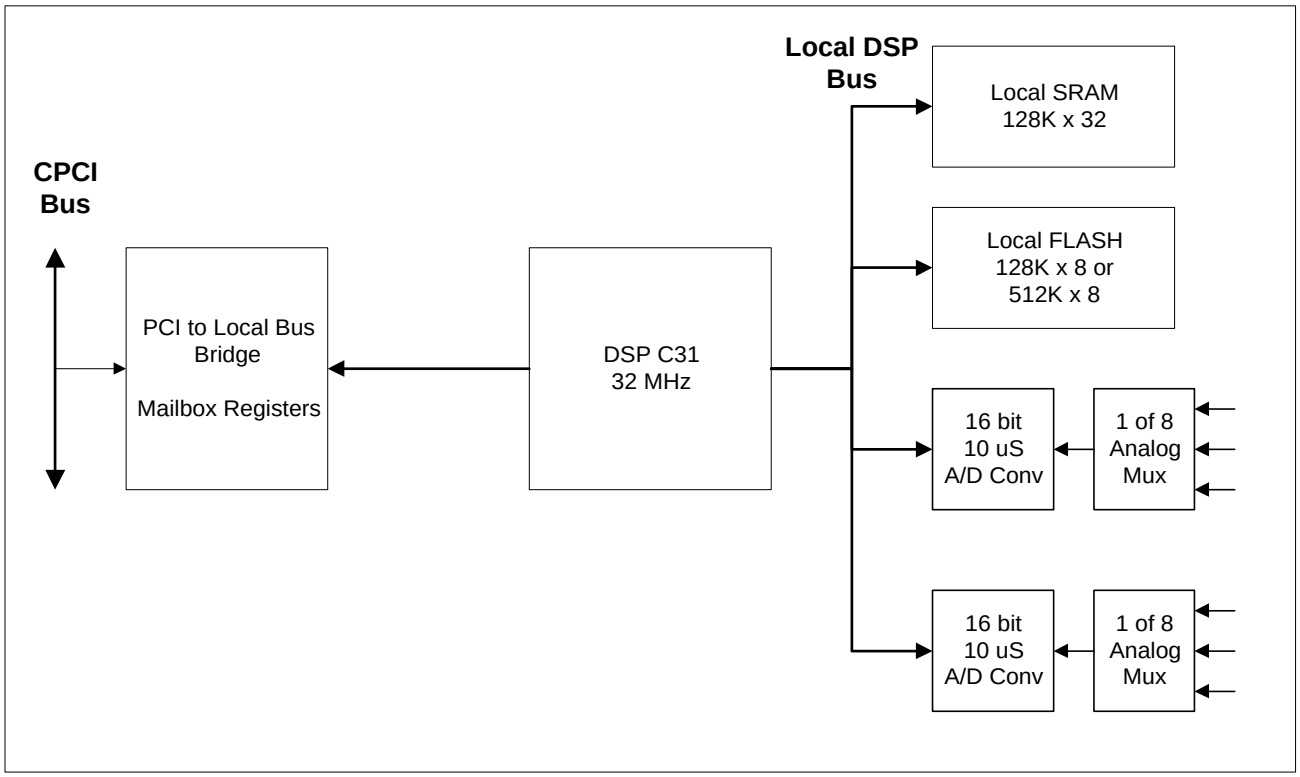

Figure 1.1: Block Diagram

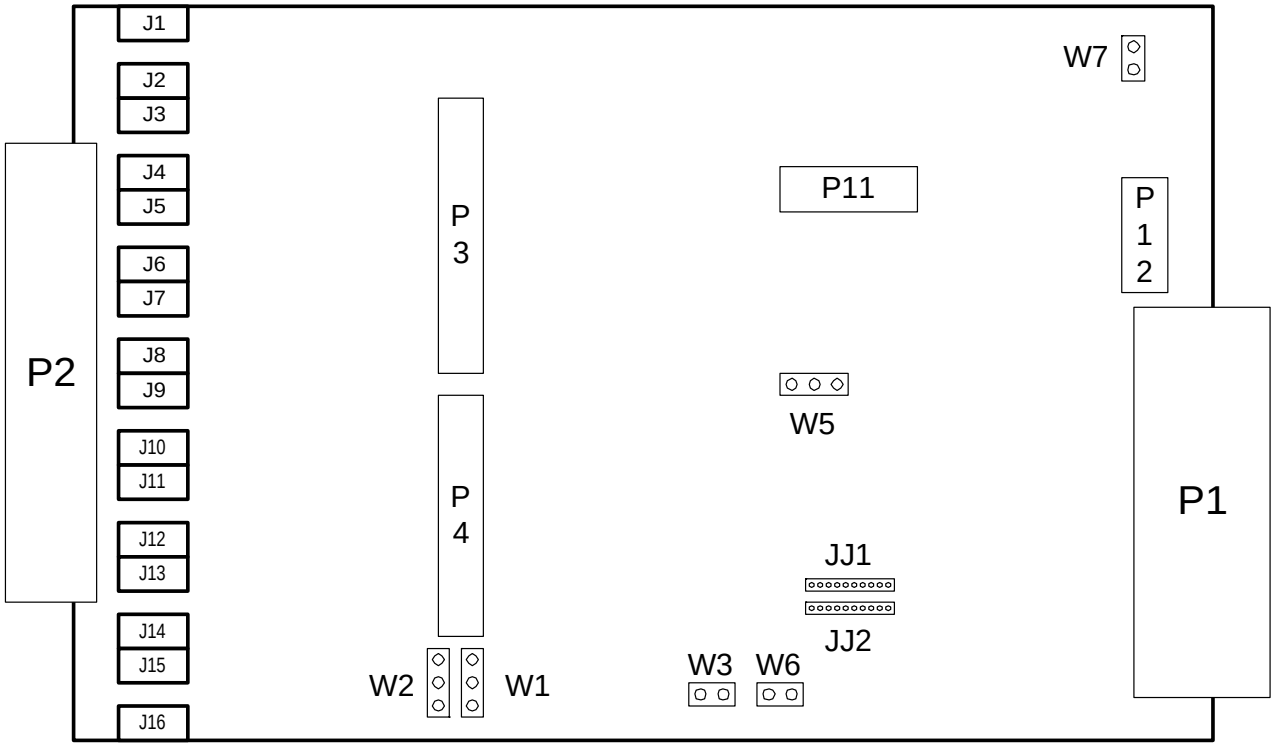

Figure 1.2: Jumper and Connector Locations

1.3 REFERENCE MATERIALS LIST

The reader should refer to the PCI Local Bus Specification for a detailed explanation of the PCI bus architecture and timing requirements. This specification is available from the following source:

PCI Special Interest Group
PO Box 14070
Portland, OR 97214
Tel: (800) 433-5177
Tel: (503) 797-4207
Fax: (503) 234-6762

The reader is also referred to the S5933 PCI Controller data book:

AMCC Applied Micro Circuits Corporation
6195 Lusk Boulevard
San Diego, CA 92121-2793
Tel: (800) 755-2622
http://www.amcc.com

WindowsNT and Windows95 Programming Tools:

BlueWater Systems
144 Railroad Ave. Suite #217
Edmonds, WA 98020
Tel: (206) 771-3610
Fax: (206) 771-2742
E-Mail: info@bluewatersystems.com
Web: http://www.bluewatersystems.com

2. HOST (CPCI) SIDE

2.1 PCI CONFIGURATION REGISTERS

The card presents the following configuration values to the CPCI system, based on the values stored in the NVRAM device read by the AMCC PCI interface chip.

Register	Value (Meaning)
Vendor ID	0x13c5 (ALPHI Technology)
Device ID	0x0104 (CPCI-AD16)
Revision ID	0x00
Class Code	0xff0000 (Device does not fit into defined class codes)
Interrupt Line	0xff
Interrupt Pin	A
Multifunction Device	No
Build In Self Test	No
Latency Timer	0x00
Minimum Grant	0x00
Maximum Latency	0x00
Expansion ROM Size	None

Table 2.1: CPCI Configuration Registers

2.2 PCI BASE ADDRESS REGISTERS

The card requests base address regions from the CPCI system after RESET, based on the values stored in the NVRAM device read by the AMCC PCI interface chip.

The decode addresses of these regions are assigned by the host processor. The **CPCI-AD16** uses 1 of the 5 AMCC mapped base address registers. The AMCC is normally programmed at the factory to request the following resource from the CPCI BIOS:

BAR	From	To	Description	Type
0	0x00000000	0x00000003F	AMCC PCI Operation Registers	MEM

Table 2.2: Base Address and Use

NOTE: The AMCC has been programmed to request memory above 1 Mbytes.

2.3 CPCI OPERATION REGISTERS

The host processor communicates with the **CPCI-AD16** card via the AMCC pass-through interface. After the base address register has been programmed by the CPCI configurator, incoming CPCI I/O or Memory cycles are used to access the registers of the AMCC chip. The PCI Operation Registers of the AMCC 5933 chip are depicted below:

Offset	Register Name
0x00	OMB1 Outgoing Mailbox Register 1
0x04	OMB2 Outgoing Mailbox Register 2
0x08	OMB3 Outgoing Mailbox Register 3
0x0C	OMB4 Outgoing Mailbox Register 4
0x10	IMB1 Incoming Mailbox Register 1
0x14	IMB2 Incoming Mailbox Register 2
0x18	IMB3 Incoming Mailbox Register 3
0x1C	IMB4 Incoming Mailbox Register 4
0x20	FIFO Register Port (bi-directional)
0x24	MWAR Master Write Address Register
0x28	MWTC Master Write Transfer Counter
0x2C	MRAR Master Read Address Register
0x30	MRTC Master Read Transfer Counter
0x34	MBEF Mailbox Empty/Full Status
0x38	INTCSR Interrupt Control/Status Register
0x3C	MCSR Bus Master Control/Status Register

Table 2.3: AMCC Registers (HOST)

For more information about these registers refer to the AMCC PCI controller manual.

3. C31 SIDE

3.1 INTERNAL ORGANIZATION

The **CPCI-AD16** card is divided into different sections. Each section and its relationship to other sections will be discussed. The **CPCI-AD16** sections are:

- CPCI interface
- Analog Input

3.2 CPCI INTERFACE

The local DSP processor communicates with the CPCI bus through the AMCCS9533 chip that provides bi-directional FIFO and Mailbox registers. The **CPCI-AD16** can function as both a servant (CPCI target) or as a master (CPCI initiator) for DMA access. The following interface descriptions refer to the CPCI interface as seen by the local DSP. The AMCC registers are located at DSP address 0xf00080.

3.2.1 BI-DIRECTIONAL FIFO

Two separate FIFO data paths are implemented within the AMCCS9533, a read FIFO that allows data transfers from the module to the CPCI bus and a write FIFO that transfers data from the CPCI to the module. Size of the FIFO is 32 bit X 8. Read and write DMA access to the host can occur via the FIFO registers if it is supported by the software on the HOST and is enabled. Alternatively, the FIFO registers can utilize a polled scheme on the HOST and

DSP. Both FIFOs are accessed via access to the same location as seen by the DSP, offset 0x08.

3.2.2 MAILBOX REGISTERS

The Mailbox registers of the AMCCS9533 provide a bi-directional data path that can be used to send data or software control information between the HOST and DSP of that half of the **CPCI-AD16** module. Interrupts can be enabled based on a specific mailbox event. There are 4 incoming mailboxes and 4 outgoing mailboxes. Each mailbox is 32 bits wide. The address offsets for the mailboxes are shown below in Table 3-1.

3.2.3 ADDITIONAL REGISTERS

The AMCC S5933 PCI controller has a set of additional registers to control and monitor the behavior of the CPCI interface.

The address offsets of these registers are shown below in Table 3-1.

Offset	Register Name
0x00	Incoming Mailbox Reg 1
0x01	Incoming Mailbox Reg 2
0x02	Incoming Mailbox Reg 3
0x03	Incoming Mailbox Reg 4
0x04	Outgoing Mailbox Reg 1
0x05	Outgoing Mailbox Reg 2
0x06	Outgoing Mailbox Reg 3
0x07	Outgoing Mailbox Reg 4
0x08	Add-on FIFO port
0x09	Bus master write Address Register
0x0A	Add-on Pass through Address
0x0B	Add-on Pass trough Data
0x0C	Bus master read Address Register
0x0D	Add-on Mailbox Empty/full Status
0x0E	Add-on Interrupt Control
0x0F	Add-on General Control/Status Register

Table 3.1: AMCC Registers (DSP)

For more information about these registers refer to the AMCC PCI controller manual.

3.3 ANALOG INPUT

The **CPCI-AD16** has sixteen analog inputs each with its own instrumentation amplifier and digitally programmed gain. Several input modes are selectable, including full differential, and single ended. The inputs are +/- 10 Volts.

Input signals can be optionally routed to an analog filtering / sample and hold daughter-board, which can be configured to custom specifications.

The inputs are then routed to a pair of 10 uS 16 bit A/D converter via a pair of 8 to 1 analog multiplexers.

The input circuits and A/D converters can be powered by the +/- 12 volts available from the CPCI bus, or by an externally provided +/- 15 volts supply.

The instrumentation amplifier also provides over-voltage protection to the input circuits.

3.3.1 Input Mode

The sixteen analog inputs can operate in one of several modes, depending upon the jumper selections at the inputs. These jumpers are labeled J1 – J16 and correspond to channels 1 through 16 based on the following table:

Input Channel	Jumper	Input Channel	Jumper
1	J1	9	J9
2	J3	10	J11
3	J5	11	J13
4	J7	12	J15
5	J2	13	J10
6	J4	14	J12
7	J6	15	J14
8	J8	16	J16

Table 3.2: Jumpers for Input Channels

The following input modes are available. If selected, the return path is through a 10 Megohm resistor to local ground.

Input Mode	Jumpers
Full Differential	1-2
Full Differential with Return Path	1-2, 5-6
Single Ended referenced to Local (card) Ground	7-8
Single Ended referenced to Remote Ground (RG)	3-4
Single Ended referenced to Remote Ground (RG) with Return Path	3-4, 5-6

Table 3.3: Input Mode Selection

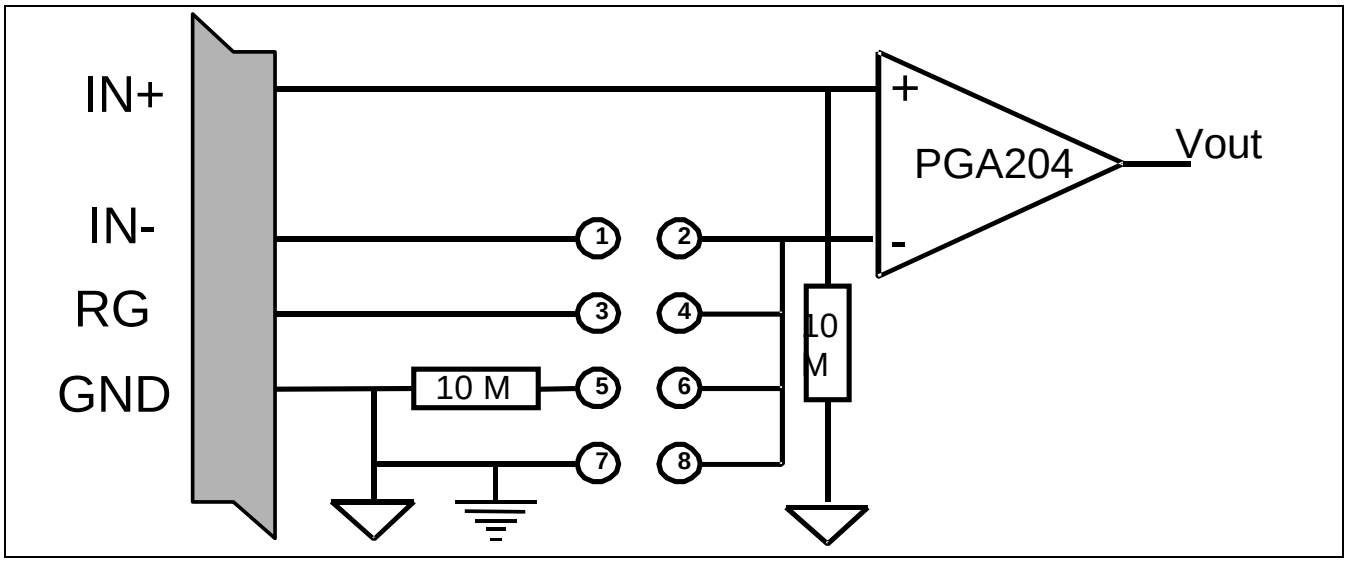

Figure 3.1: Input Equivalent Circuit

3.3.2 Gain Selection

The instrumentation amplifier gains are easily set by the DSP through the ***AD_GAIN*** register. The gains can be set to 1, 10, 100, or 1000. See the description of the ***AD_GAIN*** register for more details.

3.3.3 Input Multiplexer Selection

Two one of eight analog multiplexers route the input signals to one of the two A/D converters. Inputs 1 through 8 are connected to one A/D converter and inputs 9 through 16 are connected to the second. Input routing is controlled via the ***AD_MUX*** register. See the description of the ***AD_MUX*** register for more details.

3.3.4 Conversion

The two 16 bit A/D converters can be clocked from the following sources:

- Internal sampling clock provided by DSP timer 1 (output on **SAMPLE_CLK_OUT**)
- Internal sampling clock provided by DSP timer 0
- External sampling clock provided on **SAMPLE_CLK_IN** and enabled by **SAMPLE_CLK_GATE**.
- Triggered by the DSP writing to ***SAMPLE_AD***

The DSP will be interrupted on INT2 when the conversions are complete.

The data is read from a 32 bit register, ***AD_DATA*** with one channel in the low WORD and the other in the high WORD.

3.4 DSP MEMORY AND REGISTER MAP SUMMARY

NAME	START	END	DATA	R/W	COMMENTS
SRAM	0x000000	0x01FFFF	D00-D31	R/W	Zero wait state static RAM
FLASH	0x400000	0x41FFFF	D00-D07	R/W	128K x 8 Protected
AD_DATA	0xF00000	0xF00000	D00-D31	R	Results from A/D converters
CONTROL	0xF00020	0xF00020	D00-D07	W	Control Register
STATUS	0xF00028	0xF00028	D00-D05	R	Status Register
AD_GAIN	0xF00030	0xF00030	D00-D31	W	Channel Gains
AD_MUX	0xF00031	0xF00031	D00-D07	W	Input Multiplexer
AD_FILTER	0xF00032	0xF00032	D00-D31	W	Reserved to control filter
STROBE	0xF00038	0xF00038	N/A	WS	Manually start conversion
AMCC	0xF00080	0xF0008F	D00-D31	R/W	AMCC REGISTERS
WRFIFO	0xF000A0	0xF000A0	D00-D31	W	Write to AMCC FIFO
RDFIFO	0xF000A0	0xF000A0	D00-D31	R	Read from AMCC FIFO

Table 3.4: DSP Memory Map

3.4.1 AD_DATA (Read Only)

BITS 31 – 16	BITS 15 – 00
A/D Channels 01 – 08	A/D Channels 09 – 16

This 32 bit register contains the results from both input converters. Each result is a 16 bit 2's complement integer. A count of 0x7FFF represents +10 V (if the input gain is 1), and a count of 0x8000 represents –10 V.

Multiplexer signal routing is accomplished via the ***AD_MUX*** register.

3.4.2 CONTROL (Write Only)

BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 00
N/A	TIM_1	TIM_0	N/A	N/A	N/A	N/A	EXT_SAMP_CLK_EN

EXT_SAMP_CLK_EN ***External Sampling Clock/Gate Enable***

When this bit is set to 1, a rising edge on **SAMPLE_CLK_IN** when **SAMPLE_CLK_GATE** is high, or a rising edge on **SAMPLE_CLK_GATE** when **SAMPLE_CLK_IN** is high, will start a single A/D conversion. When this bit is cleared to 0, **SAMPLE_CLK_IN** and **SAMPLE_CLK_GATE** are ignored (except as causes of interrupts).

TIM_0, TIM_1 ***Sampling Clock Selection***

See the following table for selecting the source of the sampling clock.

TIM_1	TIM_0	Result
0	0	Writes to ***STROBE*** will trigger a single conversion.
0	1	DSP Timer 0 will trigger a single conversion.
1	0	DSP Timer 1 will trigger a single conversion.
1	1	No internal source will trigger a conversion.

Table 3.5: Sampling Clock Selection

3.4.3 STATUS (Read Only)

BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 00
N/A	TIM_1	TIM_0	RDEMPTY	N/A	EXT_SAMP_CLK_EN

EXT_SAMP_CLK_EN, TIM_0, TIM_1 Read back of control bits

These bits allow for reading back the current state of the ***CONTROL*** bits.

RDEMPTY AMCC FIFO is empty

This bit is a redundant flag to one in the AMCC chip.

3.4.4 AD_GAIN

Bits	Channel	Bits	Channel	Bits	Channel	Bits	Channel
31, 30	IN16	23, 22	IN12	15, 14	IN08	07, 06	IN04
29, 28	IN15	21, 20	IN11	13, 12	IN07	05, 04	IN03
27, 26	IN14	19, 18	IN10	11, 10	IN06	03, 02	IN02
25, 24	IN13	17, 16	IN09	09, 08	IN05	01, 00	IN01

Two bits select the gain for each of the 16 input channels. The following table describes the gains available.

MSB	LSB	Gain
0	0	x1
0	1	x10
1	0	x100
1	1	x1000

Table 3.6: Available Gain Selections

3.4.5 AD_MUX

This register controls the two analog input multiplexers. The low bits select one of channel 1 through 8 to one A/D converter, and the high bits select one of channel 9 through 16 to the second. The following tables describe the necessary programming.

BIT 03	BIT02	BIT01	BIT00	Selected
1	0	0	0	IN01
1	0	0	1	IN02
1	0	1	0	IN03
1	0	1	1	IN04
1	1	0	0	IN05
1	1	0	1	IN06
1	1	1	0	IN07
1	1	1	1	IN08
0	X	X	X	Do not use.

Table 3.7: Multiplexer selection for converter 1

BIT 07	BIT06	BIT05	BIT04	Selected
1	0	0	0	IN09
1	0	0	1	IN10
1	0	1	0	IN11
1	0	1	1	IN12
1	1	0	0	IN13
1	1	0	1	IN14
1	1	1	0	IN15
1	1	1	1	IN16
0	X	X	X	Do not use.

Table 3.8: Multiplexer selection for converter 2

For maximal speed conversion, the input multiplexers should be changed to the next selection just after the conversion has been started for the current selection. The settling time of the A/D multiplexers is less than the conversion time of the A/D converters.

3.4.6 AD_FILTER

This register is reserved for use with an optional Nyquist filter / sample and hold daughter-board. Contact the factory for more details.

3.4.7 STROBE (Write Strobe Only)

If the **CONTROL** Register is configured to allow it, a write to this location will trigger an A/D conversion.

3.5 RESET SIGNALS

The **CPCI-AD16** can be reset from two different sources:

- At power on or when the PCI RESET is asserted, the watchdog timer will hold the C31 RESET line low for 200 ms.
- The AMCC has a bit called SYSRST which the HOST can toggle to reset the DSP. Software should hold the RESET asserted for 200 mS.

3.6 LOCAL DSP INTERRUPT SOURCES

The local DSP has four interrupt lines. The source of each interrupt is listed in the table below. Additionally, at reset, the INT1 line is pulsed to tell the C31 to find the FLASH image at 0x400000 (if boot mode is MC).

SOURCE	ENABLE SIGNAL	INTERRUPT LEVEL
SAMPLE_CLK_GATE	None	INT0
AMCC FIFO: WR not Full RD not Empty	Inside AMCC	INT1
A/D Conversions Complete	None	INT2
SAMPLE_CLK_IN	None	INT3

Table 3.9: Interrupt Sources

4. JUMPER DESCRIPTIONS

JUMPER	FACTORY SETTING	DESCRIPTION
W1	2-3	Analog Power (pos): 1-2 for external +15V, 2-3 for CPCI bus power.
W2	2-3	Analog Power (neg): 1-2 for external -15V, 2-3 for CPCI bus power.
W3	Present	Factory use only.
W5	2-3	DSP clock: 1-2 for CPCI bus, 2-3 for internal 32 MHz clock.
W6	None	When shorted, provides DSP and IP reset.
W7	None	DSP Boot Mode: MC/~MP. The DSP's boot mechanism is designed to operate in MC mode, booting from the FLASH.

Table 4.1 Jumper Descriptions

5. CONNECTIONS

5.1 EXTERNAL I/O CONNECTOR (P2)

A 80 pin subminiature D shelled connector is used to route all the analog and digital signals off the card. ALPHI Technology can supply transition modules and cable assemblies to meet any special requirements. Contact the factory for additional information.

Connectors are manufactured by AMP.

Use	Model
On PC Board	787190-8
Suggested Plug	749111-7

Table 5.1: I/O Connector Model Numbers

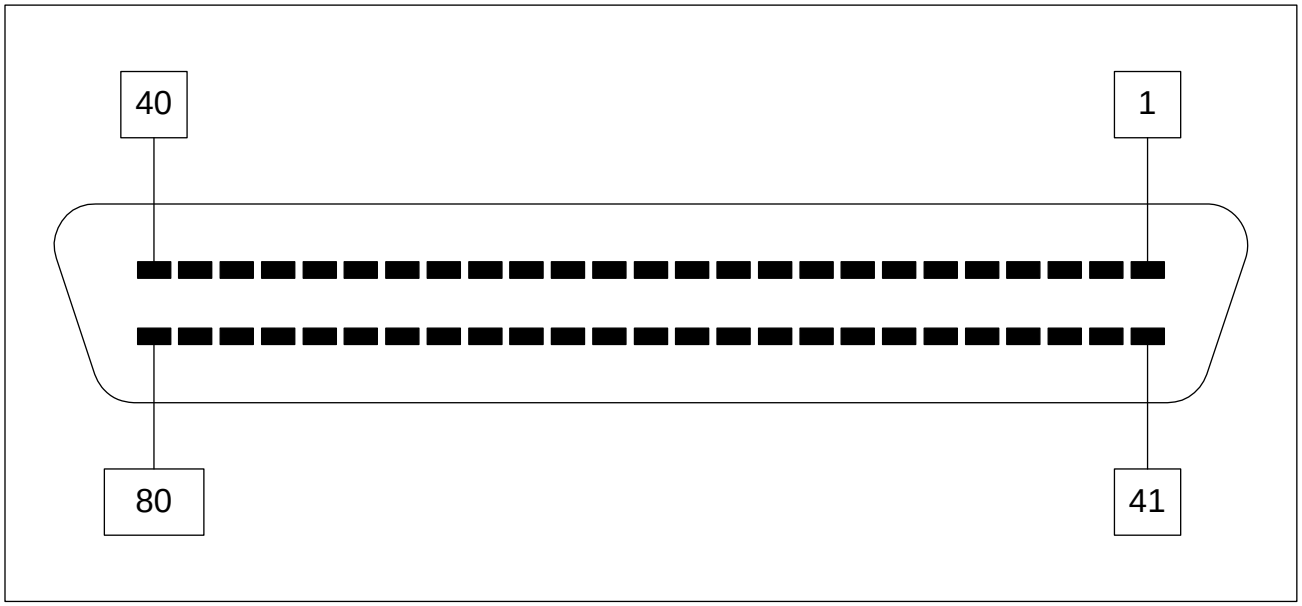

Figure 5.1: External I/O Connector

Pin	Connection	Pin	Connection
1	-15V EXTERNAL	41	D_GND
2		42	+5V OUT
3		43	D_GND
4		44	+15V EXTERNAL
5	SAMPLE CLK OUT	45	A_GND
6	SAMPLE CLK IN	46	D_GND
7	SAMPLE CLK GATE	47	REMOTE GND (RG)
8	D_GND	48	REMOTE GND (RG)
9	IN16-	49	A_GND
10	IN16+	50	A_GND
11	IN15-	51	A_GND
12	IN15+	52	A_GND
13	IN14-	53	A_GND
14	IN14+	54	A_GND
15	IN13-	55	A_GND
16	IN13+	56	A_GND
17	IN12+	57	A_GND
18	IN12+	58	A_GND
19	IN11+	59	A_GND
20	IN11+	60	A_GND
21	IN10+	61	A_GND
22	IN10+	62	A_GND
23	IN09+	63	A_GND
24	IN09+	64	A_GND
25	IN08-	65	A_GND
26	IN08+	66	A_GND
27	IN07-	67	A_GND
28	IN07+	68	A_GND
29	IN06-	69	A_GND
30	IN06+	70	A_GND
31	IN05-	71	A_GND
32	IN05+	72	A_GND
33	IN04-	73	A_GND
34	IN04+	74	A_GND
35	IN03-	75	A_GND
36	IN03+	76	A_GND
37	IN02-	77	A_GND
38	IN02+	78	A_GND
39	IN01-	79	A_GND
40	IN01+	80	A_GND

Table 5.2: External I/O Connector

5.2 EMULATOR CONNECTION (P11)

This connector is used to connect the emulator to the C31 DSP. It follows the standard form as described by TI in their processor manual.

5.3 FACTORY USE (P12)

This connector is used at the factory for programming the FPGA.

5.4 32 BIT CPCI BUS (P1)

This connector plugs into the backplane and provides the standard CPCI signals for all CPCI systems.

5.5 A/D INPUT CONFIGURATION (J1 – J16)

These jumpers are fully described in section 3.3.1.

5.6 FACTORY USE (JJ1, JJ2)

This connector is used at the factory for testing purposes.

5.7 ADD-ON NYQUIST FILTER / SAMPLE AND HOLD CONNECTORS (P3, P4)

These connectors allow for the connection of an optional input filtering card. If the card is not present, then P3 must have the following pins jumpered.

1-2, 3-4, 5-6, 7-8, 9-10, 11-12, 13-14, 15-16, 21-22, 23-24, 25-26, 27-28, 29-30, 31-32, 33-34, 35-36.