CPCI-48IN

48 Channels of Optically Isolated Digital Inputs for 3U *CPCI*™ Systems

REFERENCE MANUAL

741-11-000-4000
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Part Number: 741-11-000-4000

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1. GENERAL DESCRIPTION

1.1 INTRODUCTION

The **CPCI-48IN** is a CPCI expansion card in a 3U form factor. The **CPCI-48IN** allows:

- 48 optically isolated digital inputs readable by the CPCI HOST computer
- Implemented by means of three 8536 chips
- Ability to have the 8536 chips interrupt the host when significant events occur
- Direct memory mapped access to the 8536 chips
- Front panel I/O connectors for all inputs

1.2 FUNCTIONAL DESCRIPTION

A functional block diagram of the **CPCI-48IN** is presented below in Figure 1-1. The jumper placement and the connector placement is depicted in Figure 1-2. The **CPCI-48IN** operates as a slave that is managed by the host processor on the CPCI bus.

The **CPCI-48IN** is supported by ALPHI Technology under *Windows NT* by a **Board Support Package** which is supplied with the card. Other documentation supplied with the card will describe this support in full detail.

This is provided in a manner consistent across ALPHI Technology platforms.

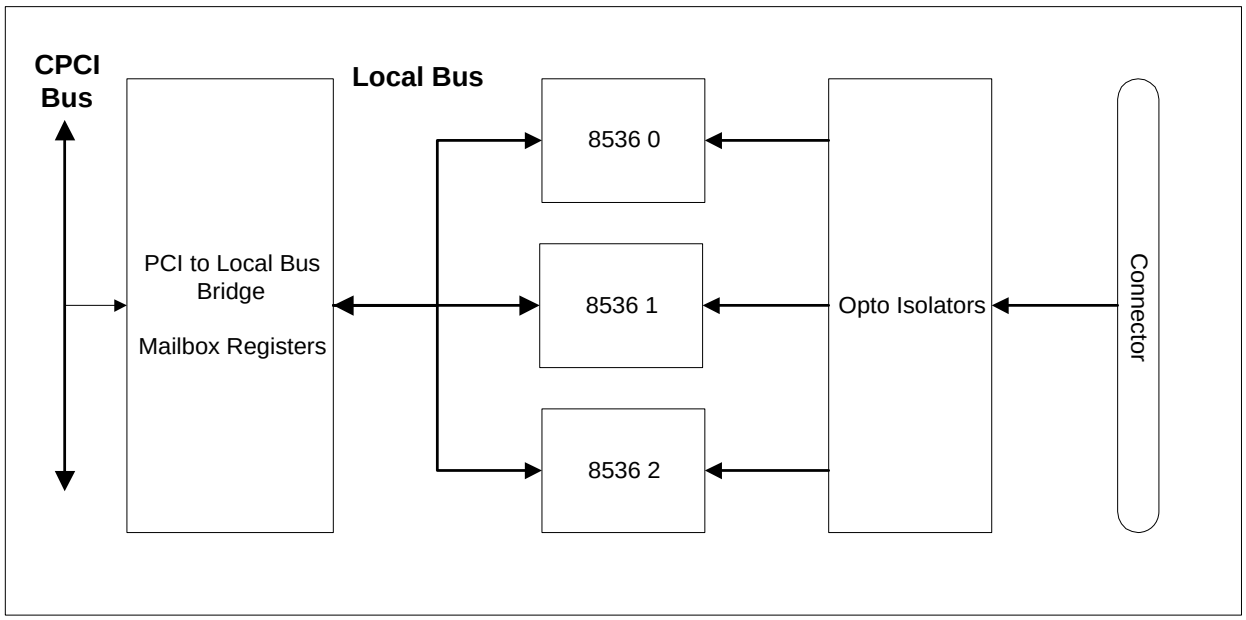

Figure 1.1: Block Diagram

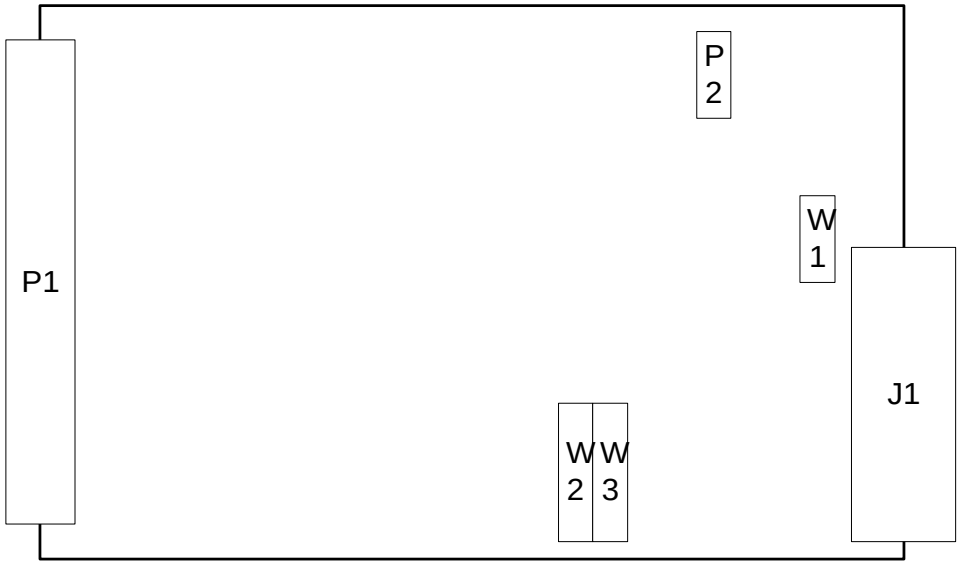

Figure 1.2: Jumper and Connector Locations

1.3 REFERENCE MATERIALS LIST

The reader should refer to the PCI Local Bus Specification for a detailed explanation of the PCI bus architecture and timing requirements. This specification is available from the following source:

PCI Special Interest Group
PO Box 14070
Portland, OR 97214
Tel: (800) 433-5177
Tel: (503) 797-4207
Fax: (503) 234-6762

The reader is also referred to the S5933 PCI Controller data book:

AMCC Applied Micro Circuits Corporation
6195 Lusk Boulevard
San Diego, CA 92121-2793
Tel: (800) 755-2622
http://www.amcc.com

WindowsNT and Windows95 Programming Tools:

BlueWater Systems
144 Railroad Ave. Suite #217
Edmonds, WA 98020
Tel: (206) 771-3610
Fax: (206) 771-2742
E-Mail: info@bluewatersystems.com
Web: http://www.bluewatersystems.com

2. HOST (CPCI) SIDE

2.1 PCI CONFIGURATION REGISTERS

The card presents the following configuration values to the CPCI system, based on the values stored in the NVRAM device read by the AMCC PCI interface chip.

Register	Value (Meaning)
Vendor ID	0x13c5 (ALPHI Technology)
Device ID	0x0106 (CPCI-IN48)
Revision ID	0x00
Class Code	0xff0000 (Device does not fit into defined class codes)
Interrupt Line	0xff
Interrupt Pin	A
Multifunction Device	No
Build In Self Test	No
Latency Timer	0x00
Minimum Grant	0x00
Maximum Latency	0x00
Expansion ROM Size	None

Table 2.1: CPCI Configuration Registers

2.2 PCI BASE ADDRESS REGISTERS

The card requests base address regions from the CPCI system after RESET, based on the values stored in the NVRAM device read by the AMCC PCI interface chip.

The decode addresses of these regions are assigned by the host processor. The **CPCI-48IN** uses 2 of the 5 AMCC mapped base address registers. The AMCC is normally programmed at the factory to request the following resources from the CPCI BIOS:

BAR	From	To	Description	Type
0	0x00000000	0x0000003F	AMCC PCI Operation Registers	MEM
1	0x00000000	0x000000FF	Host Control Region	MEM

Table 2.2: Base Addresses and Use

NOTE: The AMCC has been programmed to request memory above 1 Mbytes.

2.3 CPCI OPERATION REGISTERS

The host processor communicates with the **CPCI-48IN** module via the AMCC pass-through interface. After the base address registers have been programmed by the CPCI configurator, incoming CPCI I/O or Memory cycles are translated into either accesses to the AMCC chip or passed through to the 8536 or internal registers as described in the next section. The PCI Operation Registers of the AMCC 5933 chip are depicted below:

Offset	Register Name
0x00	OMB1 Outgoing Mailbox Register 1
0x04	OMB2 Outgoing Mailbox Register 2
0x08	OMB3 Outgoing Mailbox Register 3
0x0C	OMB4 Outgoing Mailbox Register 4
0x10	IMB1 Incoming Mailbox Register 1
0x14	IMB2 Incoming Mailbox Register 2
0x18	IMB3 Incoming Mailbox Register 3
0x1C	IMB4 Incoming Mailbox Register 4
0x20	FIFO Register Port (bi-directional)
0x24	MWAR Master Write Address Register
0x28	MWTC Master Write Transfer Counter
0x2C	MRAR Master Read Address Register
0x30	MRTC Master Read Transfer Counter
0x34	MBEF Mailbox Empty/Full Status
0x38	INTCSR Interrupt Control/Status Register
0x3C	MCSR Bus Master Control/Status Register

Table 2.2: AMCC Registers (HOST)

For more information about these registers refer to the AMCC PCI controller manual.

2.3.1 IMB4 Incoming Mailbox Register 4 and Interrupts

Interrupting the HOST when one of the 8536 chips requests an interrupt is somewhat indirect. The HOST software needs to set up the AMCC 5933 to generate its interrupt when the contents of incoming mailbox 4 byte 3 are written.

The hardware on the card will write the contents of the Interrupt Pending Register to this mailbox when any of the 8536 chips requests an interrupt, this generating the HOST interrupt.

Then the HOST software will need to clear the cause and reset the interrupt pending bit in the appropriate 8536 chip.

2.4 HOST CONTROL REGION

Accesses to the following offsets from BAR1 will allow for communication with the card. There are three 8536 chips at offsets 0x00, 0x04, and 0x08. Additional registers allow the host to determine which 8536 chips are causing interrupts, and allow the user to illuminate an LED under software control.

Offset	Register Name
0x00	Handshake 0
0x01	Inputs 8 - 15
0x02	Inputs 0 - 7
0x03	Control Register 0
0x04	Handshake 1
0x05	Inputs 24 – 31
0x06	Inputs 16 – 23
0x07	Control Register 1
0x08	Handshake 2
0x09	Inputs 40 – 47
0x0a	Inputs 32 – 39
0x0b	Control Register 2
0x80	Interrupt Pending Register
0x88	LED Register

Table 2.3: Host Control Region

For more information about some of these registers, refer to the AMD Am8536 Reference Manual.

2.4.1 Control of 8536s

Each 8536 consists of 2 8 bit ports internally called A and B which are connected to the optical isolators and the input connector. An additional 4 bit port C can be used for handshaking in certain modes.

Internally, each 8536 consists of several configuration registers accessed through the Control Register port. These registers must be configured for the correct operation of the card. The following table outlines the available registers. Writes are accomplished by writing the address then the new value to the control register. Reads are accomplished by writing the address then reading the value from the control register.

Register	Offset	Name
MIC	0x00	Master interrupt control
MCC	0x01	Master config control
PAIV	0x02	Port A interrupt vector
PBIV	0x03	Port B interrupt vector
CTIV	0x04	Counter/Timer interrupt vector
PCDPP	0x05	Port C data path polarity
PCDD	0x06	Port C data direction
PCIOC	0x07	Port C I/O control
PACS	0x08	Port A command and status
PBCS	0x09	Port B command and status
CT1CS	0x0A	Counter/Timer 1 command and status
CT2CS	0x0B	Counter/Timer 2 command and status
CT3CS	0x0C	Counter/Timer 3 command and status
PAD	0x0D	Port A data
PBD	0x0E	Port B data
PCD	0x0F	Port C data
CT1CCH	0x10	Counter/Timer 1 current count MSB
CT1CCL	0x11	Counter/Timer 1 current count LSB
CT2CCH	0x12	Counter/Timer 2 current count MSB
CT2CCL	0x13	Counter/Timer 2 current count LSB
CT3CCH	0x14	Counter/Timer 3 current count MSB
CT3CCL	0x15	Counter/Timer 3 current count LSB
CT1TCH	0x16	Counter/Timer 1 time constant MSB
CT1TCL	0x17	Counter/Timer 1 time constant LSB
CT2TCH	0x18	Counter/Timer 2 time constant MSB
CT2TCL	0x19	Counter/Timer 2 time constant LSB
CT3TCH	0x1A	Counter/Timer 3 time constant MSB
CT3TCL	0x1B	Counter/Timer 3 time constant LSB
CT1MS	0x1C	Counter/Timer 1 mode spec
CT2MS	0x1D	Counter/Timer 2 mode spec
CT3MS	0x1E	Counter/Timer 3 mode spec
CVECT	0x1F	Current vector

Table 2.4: 8536 Registers

For a simple mode of operation, program the following registers in order for each 8536.

Register	Value	Task
MIC	0x01	Reset
MIC	0x00	
MCC	0x00	Disable all ports
PAMS	0x00	Port A Mode Spec BIT PORT
PADD	0xFF	Port A Data Direction ALL INPUTS
PADPP	0xFF	Port A Data Polarity INV ALL BITS
PBMS	0x00	Port B Mode Spec BITS PORT
PBDD	0xFF	Port B Data Direction ALL INPUTS
PBDPP	0xFF	Port B Data Polarity INV ALL BITS
PCDPP	0xFF	Port C Data Polarity INV ALL BITS
PCDD	0xFF	Port C data direction ALL INPUTS
MCC	0x94	Enable Ports A,B,C

Table 2.5: Values for Simple Input

2.4.2 Interrupt Pending Register (Read Only)

BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 00
W1: 1-2	W1: 3-4	W1: 5-6	W1: 7-8		INTREQ2	INTREQ1	INTREQ0

INTREQ0 Interrupt Pending on 8536 0

The 8536 which handles inputs 0 – 15 is requesting an interrupt.

INTREQ0 Interrupt Pending on 8536 1

The 8536 which handles inputs 16 – 31 is requesting an interrupt.

INTREQ0 Interrupt Pending on 8536 2

The 8536 which handles inputs 32 – 47 is requesting an interrupt.

W1: 1-2, W1: 3-4, W1 5-6, W1: 7-8 User Jumpers

The four jumpers on W1 can be read on the high order bits of the register. IF the jumper is present, a 0 is read.

2.4.3 LED Register (Write Only)

BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 00
							LED

LED Front Panel LED

When high, illuminates the front panel LED.

2.5 RESET SIGNALS

The **CPCI-48IN** is reset when the CPCI bus is reset.

3. HARDWARE EQUIVALENT

The card is available with three dash options, which specify the input voltage range and the threshold voltages as specified in the following table. Since the SHF620A opto-isolator has two LEDs, one in each direction, the polarity of the connection does not matter.

DASH	R	Voltage Range	Threshold Voltage
-1	4700	4 V – 30 V	3 V
-2	10K	7.5 V – 44 V	5.4 V
-3	20K	14 V – 60 V	9.8 V

Table 3.1: Dash options and associated voltages

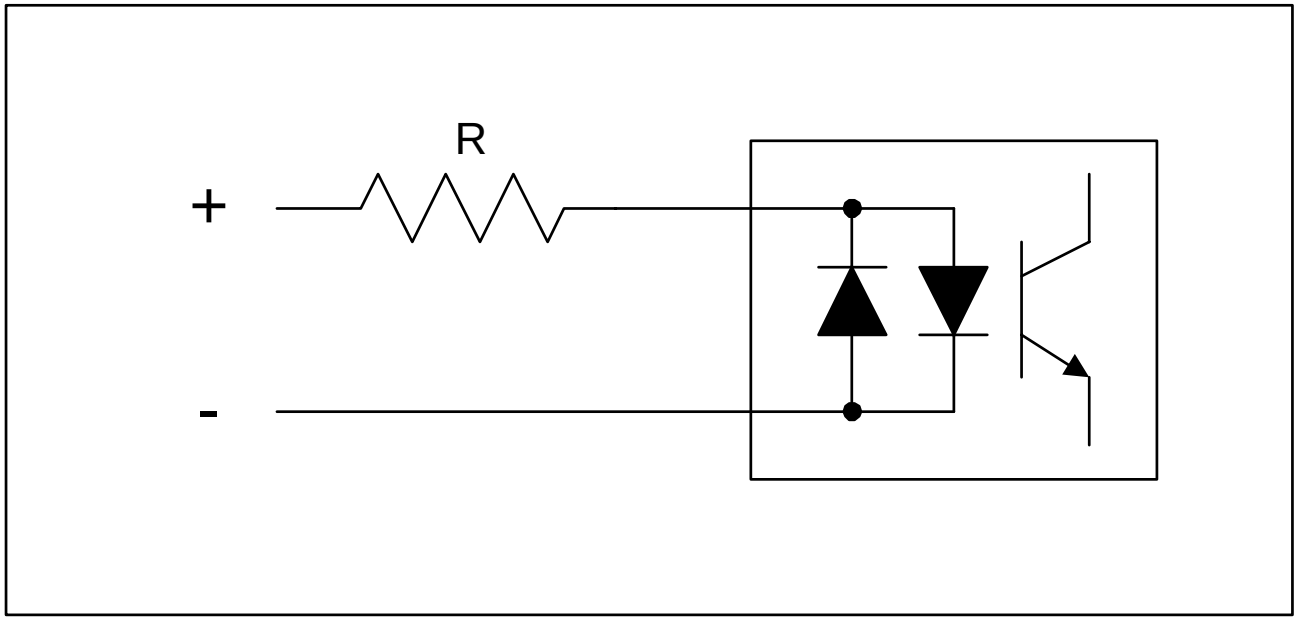

Figure 3.1: Input Circuit

The input current can be estimated by the following formula. *Vin* is in volts.

$$i = \frac{Vin - 1}{R}$$

Custom resistor values can also be installed. Discuss this with the factory at the time of order.

4. JUMPER DESCRIPTIONS

The high 4 bits of the Interrupt Pending Register are dependent on the state of the user jumper W1.

There are two optically isolated digital outputs on the card which can be used for general purpose output or for certain strobe modes of the 8536. These outputs are routed via jumpers W2 and W3.

W2	Route to OSTROB1
1-2	Bit C0 of 8536 0
3-4	Bit C2 of 8536 0
5-6	Bit C0 of 8536 1
7-8	Bit C2 of 8536 1
9-10	Bit C0 of 8536 2
11-12	Bit C2 of 8536 2

Table 4.1 W2 Jumper Descriptions

W3	Route to OSTROB2
1-2	Bit C0 of 8536 0
3-4	Bit C2 of 8536 0
5-6	Bit C0 of 8536 1
7-8	Bit C2 of 8536 1
9-10	Bit C0 of 8536 2
11-12	Bit C2 of 8536 2

Table 4.2 W3 Jumper Descriptions

5. LED INDICATORS

There are four LED indicators visible at the CPCI card bracket. They are marked with a legend on the bracket, and they are labeled on the PCB as L1 through L4 where L1 is at the top of the card. The LEDs have the following meanings:

LED	LEGEND	Meaning
L1	W	HOST is writing to the card.
L2	R	HOST is reading from the card.
L3	IT	Card is requesting an interrupt.
L4	L	HOST has written to register LED.

Table 5.1 LED Descriptions

6. CONNECTIONS

6.1 DIGITAL INPUT CONNECTOR (P1)

A 100 pin subminiature D shelled connectors are used to route all the digital input signals off the card. ALPHI Technology can supply transition modules and cable assemblies to meet any special requirements. Contact the factory for additional information.

Connectors are manufactured by AMP and the style is LIMIT.05 Series 3.

Use	Model
On PC Board	787082-9
Suggested Plug	749111-8

Table 6.1: I/O Connector Model Numbers

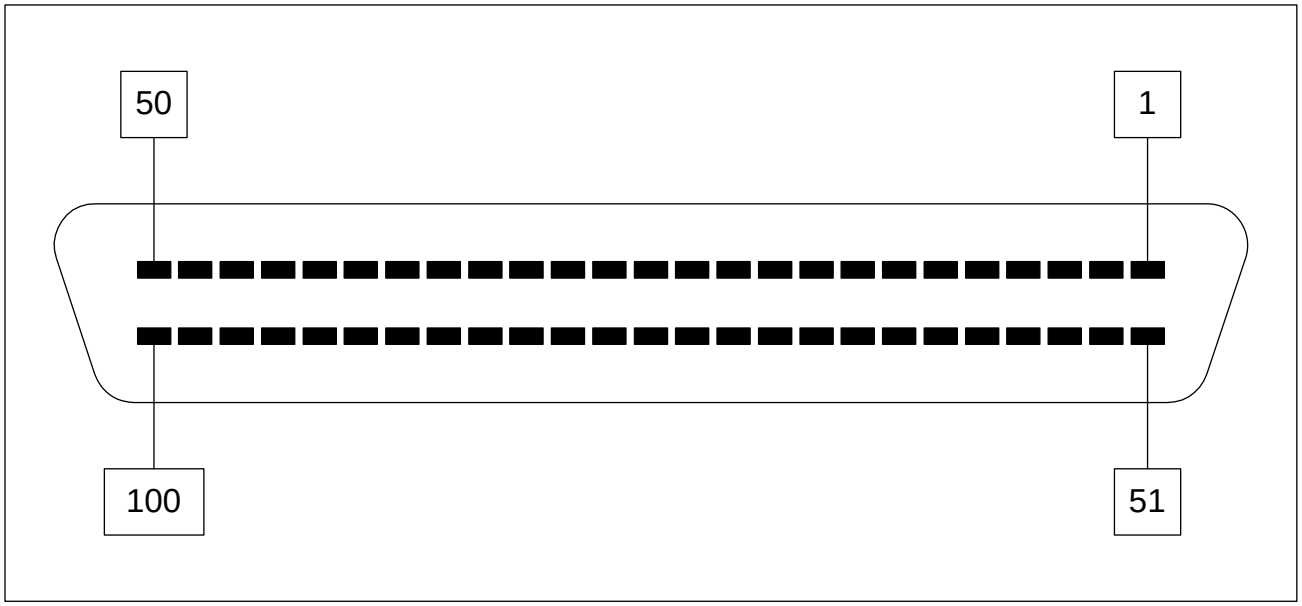

Figure 6.1: Digital Input Connector

Pin	Connection	Pin	Connection
1	STROB1+	51	STROB2+
2	STROB1-	52	STROB2-
3	IN47+	53	IN48+
4	IN47-	54	IN48-
5	IN45+	55	IN46+
6	IN45-	56	IN46-
7	IN43+	57	IN44+
8	IN43-	58	IN44-
9	IN41+	59	IN42+
10	IN41-	60	IN42-
11	IN39+	61	IN40+
12	IN39-	62	IN40-
13	IN37+	63	IN38+
14	IN37-	64	IN38-
15	IN35+	65	IN36+
16	IN35-	66	IN36-
17	IN33+	67	IN34+
18	IN33-	68	IN34-
19	IN31+	69	IN32+
20	IN31-	70	IN32-
21	IN29+	71	IN30+
22	IN29-	72	IN30-
23	IN27+	73	IN28+
24	IN27-	74	IN28-
25	IN25+	75	IN26+
26	IN25-	76	IN26-
27	IN23+	77	IN24+
28	IN23-	78	IN24-
29	IN21+	79	IN22+
30	IN21-	80	IN22-
31	IN19+	81	IN20+
32	IN19-	82	IN20-
33	IN17+	83	IN18+
34	IN17-	84	IN18-
35	IN15+	85	IN16+
36	IN15-	86	IN16-
37	IN13+	87	IN14+
38	IN13-	88	IN14-
39	IN11+	89	IN12+
40	IN11-	90	IN12-
41	IN9+	91	IN10+
42	IN9-	92	IN10-
43	IN7+	93	IN8+
44	IN7-	94	IN8-
45	IN5+	95	IN6+
46	IN5-	96	IN6-
47	IN3+	97	IN4+
48	IN3-	98	IN4-
49	IN1+	99	IN2+
50	IN1-	100	IN2-

Table 6.2: Digital Input Connector

6.2 32 BIT CPCI BUS (J1)

This connector plugs into the backplane and provides the standard CPCI signals for all CPCI systems.

6.3 FACTORY USE (P2)

This connector is used at the factory for programming the FPGA.