ATC-ALTERA

IP MODULE
ALTERA

HARDWARE REFERENCE MANUAL
792-10-000-4000

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TABLE OF CONTENTS

1. Introduction

1.1 Functional description

The IP_ALTERA module is populated with a FLEX 10K family Embedded Programmable Logic Family . A wide range of 10K package can be selected.
Another PLD from Altera (EPM7128) is used to provide all the timings and interface between the IPBUS, FLEX 10KXX chip and the 512Kbytes of Dual Access Memory.

Key Features are:

- Up to 48 I/O Pin available
- UP TO 512Kbytes of Dual Ported SRAM
- 8 or 32 MHz clock
- 2 interrupts and 2 DMA

The ATC_ALTERA use two chips:

- A EPM7128 chip use for all timing related to the IPBUS, DPR, FLEX10K30.
- A FLEX10K30RQF240-3 chip

Interconnection between the DPR and the 10K30 is provided
Up to 48 pins of TTL signals are available to the user.
The pins are grouped by 8 using a 74FCT245 as bi-directional buffer.
An optional crystal allows the user to run the 10K30 at a different speed than the IPBUS.
Customer must have ALTERA development tools to implement they own design.

2. MAP ADDRESS

The IP_ALTERA module use the three available spaces defined in the Industries Pack specifications.

2.1 IDSPACE

Up to 32 bytes of registered data provide information about the module to the User. The lower address contains data related to the type of module, revision, etc. ..
Only ODD address are valid.

ID space address	Description	Value
$01	ASCII “I”	$49
$03	ASCII “P”	$50
$05	ASCII “A”	$41
$07	ASCII “C”	$43
$09	Manufacturer identification	$11
$0B	Module type	$10
$0D	Revision module	$0A
$0F	Reserved	
$11	Driver ID,low byte	
$13	Driver ID,high byte	
$15	Number of bytes used	$0A
$17	CRC	
$19-$3F	User space	

Table 2-1 IDSEL0 SPACE byte content

2.2 IOSPACE

IP_ALTERA use the IOSPACE for the following:

2.2.1 Control Register # 0 (Read and Write)

Address: IOSPACE + $00

BD03	BD02	BD01	BD00
DMAEND_EN	FPGA1	FPGA0	nCONFIG

nCONFIG:
Configuration control input. A low Transition resets the target device; a low-to-high transition begins configuration. All I/Os go tri-state when setting nCONFIG low.

FPGA0, FPGA1:
General purpose bit user available to communicate with 10K30

DMAEND_EN:
When set to a “1” the ATC module will generate a DMAEND signal to the IPbus at the same time the /IPACK signal is active. The 10K30 that is the DMA source request should be programmed in such a way the DMARQx line is deactivated.

BD07	BD06	BD05	BD04
INTREQ1_EN	INTREQ0_EN	DMAREQ1_EN	DMAREQ0_EN

When set to a “1” enable the corresponding line to be active on the IPbus If activated by the 10K30.

2.2.2 Status Register (Just Read)

Address: IOSPACE + $02
This register provides information related to the 10K30 setting and the 10K30 interrupt pending.

BD07	BD06	BD05	BD04	BD03	BD02	BD01	BD00
NCONFIG	nSTATUS	INIT_DONE	CONF_DONE	Pull-Up	Clk32_8	MSEL1	MSEL0

MSEL0,MSEL1:

MSEL[1..0]	Description
00	Passive serial download using Bitblaster
01	Not used
10	Passive parallel synchronous
11	Passive parallel asynchronous

CLK32_8:
When set to a “1” the IPbus clock is 32 MHZ.

Pull-Up:
Not used should read “1”.

CONFIG_DONE:
Status output. The target device drives the CONF_DONE pin low before and during configuration. Once all configuration data is received without error and the initialization clock cycle starts, the target device relases CONF_DONE.
Status input. After all data is receiving and CONF_DONE goes high, the target device initializes and enters user mode.

INIT_DONE:
This signal drives low during configuration. After initialization, it is released and pulled high externally.

nSTATUS:
The device drives nSTATUS low immediately after power-up and releqses it within 5us. If an error occurs during configuration, nSTATUS is pulled low by the target device.

NCONFIG:
Configuration control input. A low Transition resets the target device; a low-to-high transition begins configuration. All I/Os go tri-state when setting nCONFIG low.

2.2.3 IVR Interrupt Vector Register

-INTREQ0

Address: IOSPACE + $04

This eight bit register located at address IOSPACE + $04 can be read and written by the Host Carrier module. The vector is automatically provided upon INTSPACE cycle perform by the Host with lower address XLA01 = “0”.

-INTREQ1

Address: IOSPACE + $06

This eight bit register located at address IOSPACE + $04 can be read and written by the Host Carrier module. The vector is automatically provided upon INTSPACE cycle perform by the Host with lower address XLA01 = “1”.

2.2.4 10K30 ALTERA PROG

Address: IOSPACE + $08

The 10K30 can be programmed in asynchronous mode by writing at the address IOSPACE + $08 word access BD00-BD07 are used. The programmation is made in byte to an internal parallel to serial register that will convert the byte in a serial stream.

2.2.5 10K30 ALTERA USER

Address: IOSPACE + $0A to IOSPACE + $3E

This address is used in the example program to write and read into a 16 bit register that will enable and select the direction of each of the 6 buffer 74 fct245 that connect the 10k30 lines to the I./O pin connector. Other application can use this feature.

FD07	FD06	FD05	FD04	FD03	FD02	FD01	FD00
SEL0	Not used	OE40	OE32	OE24	OE16	OE08	OE00

OE00-OE40:
A “1” enable the buffer output. A”0” (as upon reset) disable the buffer.
Oexx lines are pull-up.

SEL0:
To connect DIR24 and DIR40 to /EXRW

FD15	FD14	FD13	FD12	FD11	FD10	FD09	FD08
Not used	Not used	DIR40	DIR32	DIR24	DIR16	DIR08	DIR00

DIR00-DIR40:

A”1” set the buffer as an output buffer. A”0” (as upon reset) set the buffer as Input.

2.3 INTSPACE

When the 10K30 has an interrupt pending the Carrier module can read the IVR register that has been program early by the carrier. The ATC_ALTERA support two (2) interrupts.
Interrupt vector is transferred from the 10K30 through a buffer to the IPbus.
Upon receiving an interrupt cycle (INTESELA) an Interrupt vector register is provided.
Each interrupt has it own interrupt vector.

2.4 MEMORY SPACE

Up to 1 Mbytes of SRAM is mapped into the Memory space.
The SRAM is Dual access by the IP interface using the Memory space or by the 10K30.

An example program is provided in such a way that I/O lines are programmed as memory address, data bus and controls signals.
The EPM7128 chip provides arbitration between DPR accessed by the I/O connector through the 10K30 and the IPbus.

2.5 SRAM INTERCONNECTION WITH 10K30

SRAM ADDRESS	10K30 PIN		SRAM DATA	10K30 PIN
FA01	129		FD00	174
FA02	61		FD01	158
FA03	126		FD02	156
FA04	127		FD03	154
FA05	131		FD04	14
FA06	128		FD05	167
FA07	132		FD06	166
FA08	138		FD07	134
FA09	137		FD08	163
FA10	134		FD09	17
FA11	48		FD10	175
FA12	199		FD11	171
FA13	105		FD12	7
FA14	142		FD13	173
FA15	100		FD14	169
FA16	148		FD15	159
FA17	102			
FA18	198			
FA19	103			

Table 2-2 SRAM to 10K30 connection

3. Jumpers

JUMPER	FACTORY SETTING	DESCRIPTION
W1	none	Select the signal strobe from the IPbus to be an Input or an Output. 1-2,3-4 Output 1-3,2-4 Input
W2	none	Select the I/O EX_Userclk to be an input or an output signal 1-2 Input the signal is routed through an buffer 2-3 Output the signal comes from a buffer witch source is the optional oscillator .
W3		Select the CLKUSR pin from the 10K30 source 1-2 Optional oscillator buffered 2-3 External EX_USRCLK signal buffered
W4	1-2,3-4	When the jumper are set the signal MSEL0 and MSEL1 are grounded. The jumpers defines the Programmation mode that is use for the 10K30 FLEX.

Table 3-1 Jumper factory setting

4. Connectors

4.1 JTAG mode

Pin	Signal name	Description
1	TCK	Clock Signal
2	GND	Ground
3	TDO	Data from device
4	VCC	Power supply
5	TMS	JTAG state machine control
6	NC	No connect
7	NC	No connect
8	NC	No connect
9	TDI	Data to Device
10	GND	Ground

4.2 Ps mode

Pin	Signal name	Description
1	DCLK	Clock Signal
2	GND	Ground
3	CONF_DONE	Configuration done
4	VCC	Power supply
5	nCONFIG	Configuration control
6	NC	No connect
7	nSTATUS	Configuration status
8	NC	No connect
9	DATA0	Data to Device
10	GND	Ground

4.3 10K30

4.3.1 Bitblaster or Byteblaster

The 10K30 can be programmed using the Bitblaster or the Byteblaster. Connector J1 provides the interface with the ALTERA pod chip.

J1 Pin	Signal
Pin 1	TCK
Pin2	GND
Pin3	TMS
Pin4	+5V
Pin5	TDI
Pin6	TDO

Table 4-2 Bitblaster pod

4.3.2 Programmation Pod

Slave Serial programmation use connector J2 for programmation. Jumper W3 should have no Jumper.

J2 Pin	Signal
Pin 1	DCLK
Pin2	GND
Pin3	DONE
Pin4	+5V
Pin5	nCONF
Pin6	nc
Pin7	nSTATUS
Pin8	nc
Pin9	DIN
Pin10	GND

Table 4-3 Serial mode probe

5. SERIAL EPROM

The 10K30 need an EPC1 serial EEPROM to store the programmed data.

5.1 IP bus interface

		P4		
Pin 1	GND		Pin 26	GND
Pin 2	+5V		Pin 27	+5V
Pin 3	IPRESET*		Pin 28	IPRW*
Pin 4	XLD00		Pin 29	IDSEL0*
Pin 5	XLD01		Pin 30	DMAREQ0*
Pin 6	XLD02		Pin 31	MEMSEL0*
Pin 7	XLD03		Pin 32	DMAREQ1*
Pin 8	XLD04		Pin 33	INTESEL0*
Pin 9	XLD05		Pin 34	DMACK*
Pin 10	XLD06		Pin 35	IOSEL0*
Pin 11	XLD07		Pin 36	
Pin 12	XLD08		Pin 37	XLA01
Pin 13	XLD09		Pin 38	DMAEND*
Pin 14	XLD10		Pin 39	XLA02
Pin 15	XLD11		Pin 40	ERROR*
Pin 16	XLD12		Pin 41	XLA03
Pin 17	XLD13		Pin 42	INTREQ0*
Pin 18	XLD14		Pin 43	XLA04
Pin 19	XLD15		Pin 44	INTREQ1*
Pin 20	IPBS0*		Pin 45	XLA05
Pin 21	IPBS1*		Pin 46	STROBE*
Pin 22			Pin 47	XLA06
Pin 23			Pin 48	IPACK*
Pin 24	+5V		Pin 49	+5V
Pin 25	GND		Pin 50	GND

Table 5-1 IPBUS connector

5.2 I/O Port

I/O	CONNECTOR			Direction line	Output enable line
Pin 1	I/O 00	Pin 26	I/O 01	Dir00	OE00*
Pin 2	I/O 02	Pin 27	I/O 03	Dir00	OE00*
Pin 3	I/O 04	Pin 28	I/O 05	Dir00	OE00*
Pin 4	I/O 06	Pin 29	I/O 07	Dir00	OE00*
Pin 5	I/O 08	Pin 30	I/O 09	*Dir08*	*OE08**
Pin 6	I/O 10	Pin 31	I/O 11	*Dir08*	*OE08**
Pin 7	I/O 12	Pin 32	I/O 13	*Dir08*	*OE08**
Pin 8	I/O 14	Pin 33	I/O 15	*Dir08*	*OE08**
Pin 9	I/O 16	Pin 34	I/O 17	Dir16	OE16*
Pin 10	I/O 18	Pin 35	I/O 19	Dir16	OE16*
Pin 11	I/O 20	Pin 36	I/O 21	Dir16	OE16*
Pin 12	I/O 22	Pin 37	I/O 23	Dir16	OE16*
Pin 13	I/O 24	Pin 38	I/O 25	*Dir24*	*OE24**
Pin 14	I/O 26	Pin 39	I/O 27	*Dir24*	*OE24**
Pin 15	I/O 28	Pin 40	I/O 29	*Dir24*	*OE24**
Pin 16	I/O 30	Pin 41	I/O 31	*Dir24*	*OE24**
Pin 17	I/O 32	Pin 42	I/O 33	Dir32	OE32*
Pin 18	I/O 34	Pin 43	I/O 35	Dir32	OE32*
Pin 19	I/O 36	Pin 44	I/O 37	Dir32	OE32*
Pin 20	I/O 38	Pin 45	I/O 39	Dir32	OE32*
Pin 21	I/O 40	Pin 46	I/O 41	*Dir40*	*OE40**
Pin 22	I/O 42	Pin 47	I/O 43	*Dir40*	*OE40**
Pin 23	I/O 44	Pin 48	I/O 45	*Dir40*	*OE40**
Pin 24	I/O 46	Pin 49	I/O 47	*Dir40*	*OE40**
Pin 25	EX_CLKUSR	Pin 50	GND		

Table 2 IP connector I/O

6. Example program

The 10K30-example program uses two type of access to the Dual Ported Ram.

- Parallel address input from the I/O connector
- Counter with auto incrementation of address lines

Bit SELO inside the 10K30 makes the selection.

6.1 Parallel address input

The mode allows random selection of the data within the memory space. Buffers are selected in accordance with the following I/O pin.

		I/O		
Pin 1	EXMEMRQ*	Input	Pin 26	EXCSMEM*
Pin 2	EXRESET*	Input	Pin 27	EXRW*
Pin 3	ADDR17	Input	Pin 28	I/O 05
Pin 4	I/O 06	Input	Pin 29	I/O 07
Pin 5	ADDR01	Input	Pin 30	ADDR02
Pin 6	ADDR03	Input	Pin 31	ADDR04
Pin 7	ADDR05	Input	Pin 32	ADDR06
Pin 8	ADDR07	Input	Pin 33	ADDR08
Pin 9	ADDR09	Input	Pin 34	ADDR10
Pin 10	ADDR11	Input	Pin 35	ADDR12
Pin 11	ADDR13	Input	Pin 36	ADDR14
Pin 12	ADDR15	Input	Pin 37	ADDR16
Pin 13	DAT00	Input	Pin 38	DAT01
Pin 14	DAT02	Input	Pin 39	DAT03
DAT04	DAT04	Input	Pin 40	DAT05
Pin 16	DAT06	Input	Pin 41	DAT07
Pin 17	DAT08	Input	Pin 42	DAT09
Pin 18	DAT10	Input	Pin 43	DAT11
Pin 19	DAT12	Input	Pin 44	DAT13
Pin 20	DAT14	Input	Pin 45	DAT15
Pin 21	EXMEMGNT*	Output	Pin 46	Output
Pin 22	EXACK*	Output	Pin 47	Output
Pin 23	EXCLK	Output	Pin 48	Output
Pin 24		Output	Pin 49	Output
Pin 25	EX_CLKUSR		Pin 50	GND

Table 3 IP connector I/O

The I/O connector is behaving essentially as a BUS(I/O BUS) with:

-16 address (ADDR01-ADDR17)
The address lines are input to the ATC_ALTERA module. Lower address represents a 16-bit word.
-16 data lines (DAT00-DAT15)
Bi-directional data lines

- a reset line (EXRESET*) active low
- a memory request line (EXMEMRQ*) active low
- upon EXMEMRQ* signal set active (low) the EPM7128 will synchronize the signal with the IPCLK and arbitrate between the IPBUS and the I/O BUS.
  Then signal EXMEMGNT* is activated low signaling the I/O BUS that it has control of the DPR.
  -An active EXMEMCS* with valid address and EXRW signal can then be set (low).
  If it is a read signal (EXRW = “1”) the data will be available upon receiving the EXACK signal low.
  If it is a write signal (EXRW = “0”) data will be written upon the EXACK* signal is send.
  Signals are generally synchronized to the IPCLK.

6.2 Serial address

This mode allows consecutive address selection of the data within the memory space.
Buffers are selected in accordance with the following I/O pin.
Memory appears as a “FIFO”.
Upon receiving EXMEMGNT* from the arbiter the address will be incremented on the raising edge of EXACK* signal.
Signal reset need to be activated first before starting to access memory. No counter has been implemented to follow the progress of the memory access. It is left to the designer to implement it.

		I/O		
Pin 1	EXMEMRQ*	Input	Pin 26	EXCSMEM*
Pin 2	EXRESET*	Input	Pin 27	EXRW*
Pin 3	ADDR17	Input	Pin 28	I/O 05
Pin 4	I/O 06	Input	Pin 29	I/O 07
Pin 5			Pin 30	
Pin 6			Pin 31	
Pin 7			Pin 32	
Pin 8			Pin 33	
Pin 9			Pin 34	
Pin 10			Pin 35	
Pin 11			Pin 36	
Pin 12			Pin 37	
Pin 13	DAT00	Input	Pin 38	DAT01
Pin 14	DAT02	Input	Pin 39	DAT03
DAT04	DAT04	Input	Pin 40	DAT05
Pin 16	DAT06	Input	Pin 41	DAT07
Pin 17	DAT08	Input	Pin 42	DAT09
Pin 18	DAT10	Input	Pin 43	DAT11
Pin 19	DAT12	Input	Pin 44	DAT13
Pin 20	DAT14	Input	Pin 45	DAT15
Pin 21	EXMEMGNT*	Output	Pin 46	Output
Pin 22	EXACK*	Output	Pin 47	Output
Pin 23	EXCLK	Output	Pin 48	Output
Pin 24		Output	Pin 49	Output
Pin 25	EX_CLKUSR		Pin 50	GND

Table 4 IP connector I/O

6.3 Timing for external Read and Write in memory space.