ADM31

HIGH PERFORMANCE
DATA ACQUISITION SYSTEM
USER'S MANUAL

Revision 1.1
March 1994

ALPHI TECHNOLOGY CORP.
6202 S. Maple Avenue #128
Tempe, AZ 85283 USA
Tel : (602) 838 - 2428
Fax: (602) 838 - 4477

TABLE OF CONTENTS

INTRODUCTION

1.0 INTRODUCTION

This manual includes an overall specification, general description, unpacking information, hardware preparation, installation instructions, operating instructions, functional description and support information for the **ADM31** VME data acquistion system. The system consists of the **ADM31** control card and up to two optional analog input cards - any combination of either an **AD-24D** A/D card with 24 differential inputs or an **AD-48S** A/D card with 48 single-ended inputs.

MODULE SYSTEM SPECIFICATIONS

2.0 MODULE SYSTEM SPECIFICATIONS

Specifications for the data acquisition system are broken into three parts - **Table 1** includes the **ADM31** baseboard CPU control card, **Table 2** includes the **AD-24D** A/D card, and **Table 3** includes the **AD-48S** A/D card.

Characteristics	Specifications
microprocessor	68EC030, up to 24 MHz
system memory (master or slave)	
extended access	A32/D08 (OE) A32/D16 A32/D32, A32/D32 BLT, A32 /D32 UAT
standard access	A24/D08 (OE) A24/D16 A24/D32, A24/D32 BLT, A24/D32 UAT
memory size capability EPROM SRAM EEPROM host/control SRAM	 up to 512 Kbytes up to 6 Mbytes up to 64 Kbytes up to 128 Kbytes
indicators	scan run fail
operators	ABT (abort) RST (reset)
operating temperature	0° C to +50° C
storage temperature	-20° C to +80° C
operating humidity	90% non-condensing
power requirements	+5 VDC
physical characteristics board dimensions front panel	double height VME board with front panel 9.32 inches (233 mm) 6.4 inches (160 mm) 10.48 inches (262 mm) 0.8 inches (20 mm)

Table 1. **ADM31** Control Card Specifications.

Characteristics	Specifications
number of A/D channels	24 channels with 24 A/D's
type of A/D channel	true differential
acquisition time	10 microseconds
sampling rate	200 Ksamples/sec interleaved
input capacitance	< 70 pF
resolution	16 bits
quantization error	± .5 LSB
integral non linearity	± 0.005% FSR maximum
input overvoltage protection	± 25 V
type of code output	no missing codes, binary 2's complement
common mode rejection	>80 dB typical
common mode voltage	± 10 V minimum
low bias current	± 2 pA typical, ± 20 pA maximum at 25 °C
input impedance	> 10 GΩ (limited to 10 MΩ by resistor)
temperature range	0° C to +50° C
storage temperature	-20° C to +80° C
operating humidity	90% non-condensing
power requirements	+5 VDC, .8 A ± 12 VDC, 100 mA
physical characteristics board dimensions front panel	double height VME board 9.32 inches (233 mm) 6.4 inches (160 mm) 10.48 inches (262 mm) 0.8 inches (20 mm)

Table 2. **AD-24D** A/D Card Specifications.

Characteristics	Specifications
number of A/D channels	48 with 48 D/A's
type of A/D channel	single-ended
acquisition time	10 microseconds
sampling rate	200 Ksamples/sec interleaved
input capacitance	< 70 pF
resolution	16 bits
quantization error	± .5 LSB
integral non linearity	± 0.005% FSR maximum
input overvoltage protection	± 25 V
type of code output	no missing codes, binary 2's complement
channel-to-channel crosstalk	>96 dB at ± 10 V
bias current	< 20 pA
slew rate	13 V/microsecond
temperature range	0° C to +50° C
storage temperature	-20° C to +80° C
operating humidity	90% non-condensing
power requirements	+5 VDC, .8 A ± 12 VDC, 100 mA
physical characteristics board dimensions front panel	double height VME board 9.32 inches (233 mm) 6.4 inches (160 mm) 10.48 inches (262 mm) 0.8 inches (20 mm)

Table 3. **AD-48S** A/D Card Specifications.

GENERAL DESCRIPTION

3.0 GENERAL DESCRIPTION

The VME-based **ADM31** data acquistion system supports up to 48 differential or up to 96 single-ended analog inputs. The **ADM31** control card is an intelligent A/D subsystem master or slave device that controls the analog A/D cards. Up to two A/D cards can be configured with the control card to complete the A/D system.

The **ADM31** control card is designed with a high performance 32 bit 68EC030 processor clocked at up to 24 MHz. Two VLSI chips are used to interface the module with the VMEbus and are able to handle master and slave transfers as specified by the VMEbus specification ANSI/IEEE standard 1014-1987 Rev C.1.

The **ADM31** control card can:

- operate as a master system controller or slave in a VME card cage,
- be controlled by an external PC in terminal mode through the front panel serial port with PC-based data display information available through the parallel I/O port also on the front panel.

A hardware-based state machine on the A/D cards provide all of the independent timings to drive the high speed A/D or D/A converters. The **AD-24D** (differential analog input) or **AD-48S** (single-ended analog input) modules can be interconnected on the backplane with the **ADM31** control card using a standard VSB connector system to form a complete multi-channel data acquisition system. See **Figure 1** below for the various combinations available for an **ADM31** data acquisition system.

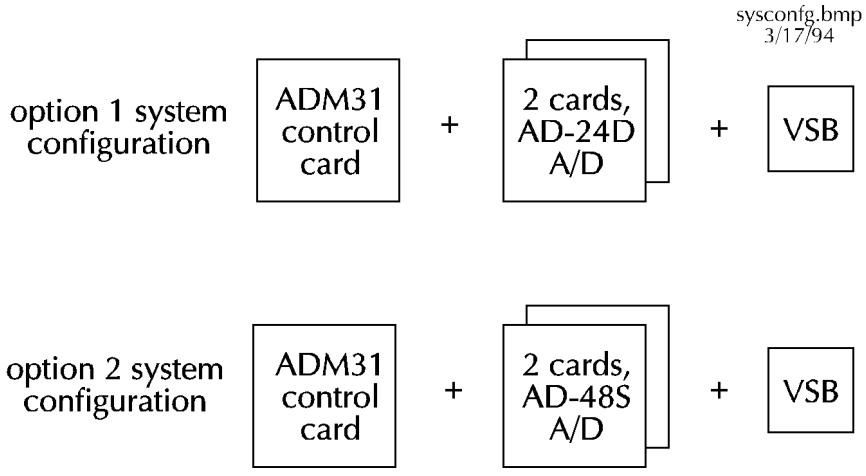


Figure 1. **ADM31** Data Acquistion System Configuration Options.

UNPACKING INSTRUCTIONS

4.0 UNPACKING INSTRUCTIONS

Unpack the data acquisition system from the shipping carton. Make sure that the included packing list and the contents match. Save packing material for storing or reshipping the data acquisition system. When removing the cards from the anti-static envelopes, make sure that appropriate grounding rules are followed. Ungrounded static discharge may destroy VLSI components.

NOTE

If shipping carton is damage upon receipt, request carrier's agent to be present during unpacking and inspection of the carton and the equipment inside the carton.

HARDWARE PREPARATION

5.0 HARDWARE PREPARATION

To ensure proper operation of the data acquisitions system, certain procedures must be followed to guarantee proper operation. The following cooling requirements, jumper configurations, backplane connector assembly mountings, I/O connectors and cable assemblies, and switches must be properly prepared and installed.

5.1 COOLING REQUIREMENTS

The **ADM31** data acquisition system is designed to operate reliably with an incoming air temperature range from 0° C to +50° C with forced air cooling. The following conditions should be met to match manufacturing testing procedures with in-the-field operation:

- The temperature cooling requirements must be performed in a standard VME chassis.
- The airflow from three axial fans should be greater than 71 CFM per fan.
- The incoming air temperature should be measured between the forced air fan cooling assembly and the VME card cage.
- Test software should be run while the data acquistion systems is operational. The test software should exercise the entire data acquisition system. If a failure due to heat occurs, the test procedure should indicate that an abnormal stop has occurred.
- Case temperatures of critical VLSI components should also be monitored to guarantee safe temperature operation and to ensure compliance with component vendor temperature guidelines. The VLSI case temperatures typically should be below +85° C for correct operation. Consult the various manuals that are suggested reading in **Section 9.0** for actual temperature limits.

5.2 JUMPERS

Only the **ADM31** control card has jumpers that can be modified. Five sets of jumpers can be reconfigured on the jumper blocks to alter the **ADM31** system controller mode of operation and EPROM and EEPROM memory sizes. **Figure 2** illustrates where the jumpers are located on the **ADM31** card.

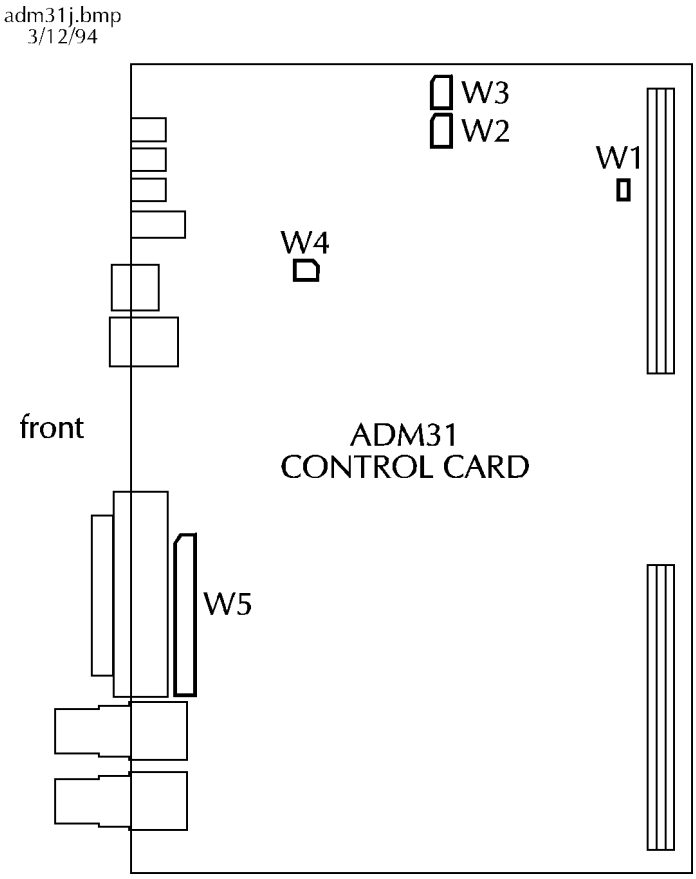
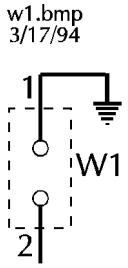


Figure 2. **ADM31** Control Card Jumper Locations.

5.2.1 W1 JUMPERS

The W1 jumper controls the basic mode of operation for the **ADM31** control card. **Figure 3** shows the W1 jumper setting, and **Table 4** illustrates the jumper functions. The factory delivered W1 jumper is "no jumper" as shown.



factory installed
with no jumper

Figure 3. W1 Jumper Setting.

jumper	function
W1	**ADM31** system controller mode of operation installed ("0") = ADM31 is the system controller not installed ("1") = ADM31 is the system slave (factory delivered)

Table 4. W1 Jumper Function.

5.2.2 W2 JUMPERS

The W2 jumpers select **ADM31** control card EPROM size. **Figure 4** shows the W2 settings, and **Table 5** illustrates the jumper functions. The factory delivered W2 jumpers are configure the **ADM31** control card for a 27C010 EPROM.

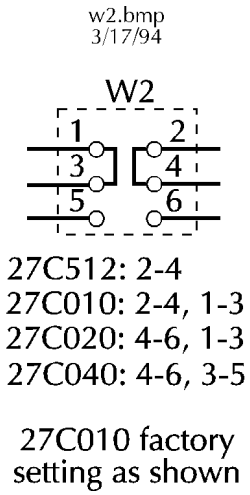


Figure 4. W2 Jumper Settings.

jumper	function
W2	**ADM31** control card EPROM choices: 27C512, 64K X 8 CMOS EPROM, or 27C010, 128K X 8 CMOS EPROM, or 27C020, 256K X 8 CMOS EPROM, or 27C040, 512K X 8 CMOS EPROM

Table 5. W2 Jumper Functions.

5.2.3 W3 JUMPERS

The W3 jumpers select **ADM31** control card EEPROM size. **Figure 5** shows the W2 settings, and **Table 6** illustrates the jumper functions. The factory delivered W2 jumpers are configure the **ADM31** control card for a 28C256 EEPROM.

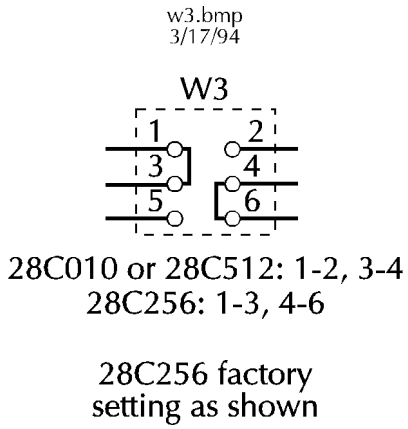


Figure 5. W3 Jumper Settings.

jumper	function
W3	**ADM31** control card EEPROM choices: 28C010 or 28C512, 128K X 8 CMOS EEPROM, or 28C256, 32K X 8 CMOS EEPROM

Table 6. W3 Jumper Functions.

5.2.4 W4 JUMPERS

The W4 jumpers select **ADM31** control card test functions and are not meant to be altered. **Figure 6** shows the W4 settings. The factory delivered W4 jumpers are “not installed.”

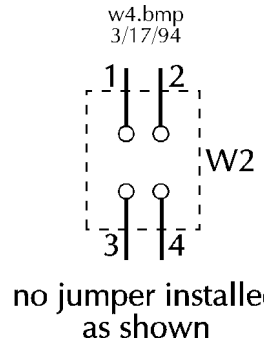


Figure 6. W4 Jumper Settings.

5.2.4 W5 JUMPERS

The W5 jumpers select **ADM31** control card parallel signaling and are not meant to be altered. **Figure 7** shows the W5 settings. The factory delivered W5 jumpers as shown and should not be removed.

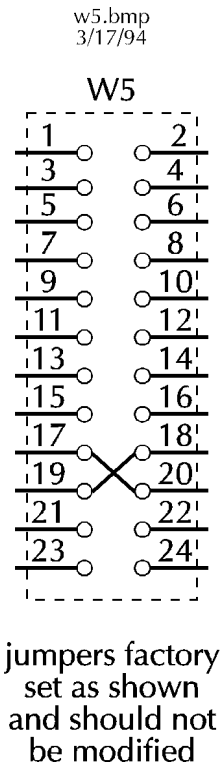


Figure 7. W5 Jumper Settings.

5.3 BACKPLANE CONNECTORS

Both of the backplane connectors on the **ADM31**, **AD-24D**, and **AD-48S** conform to VME standards.

- P1 is the standard address (A23:0) and data bus (D15:0) with VME master/slave signaling.
- P2 has the extended addressing (A24:31) and data (D31:16) signal pins.
- Both of P2's outer connector rows contain application specific non-standard signaling implementing specialized backplane I/O for the AD-24D and AD-48S A/D cards.

Figure 8 shows the location of P1 and P2 connectors on the **ADM31** for illustration purposes, **Figure 9** shows the pinout of P1 backplane connector, and **Figure 10** shows the pinout of P2 backplane connector.

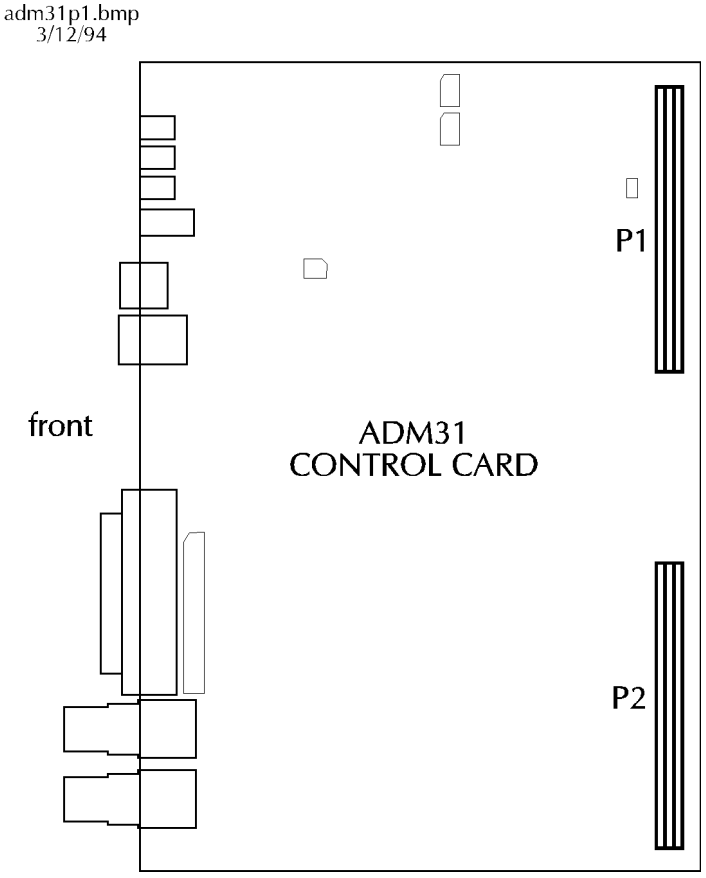


Figure 8. P1 and P2 Connector Location, **ADM31**.

p1a.bmp
3/12/94

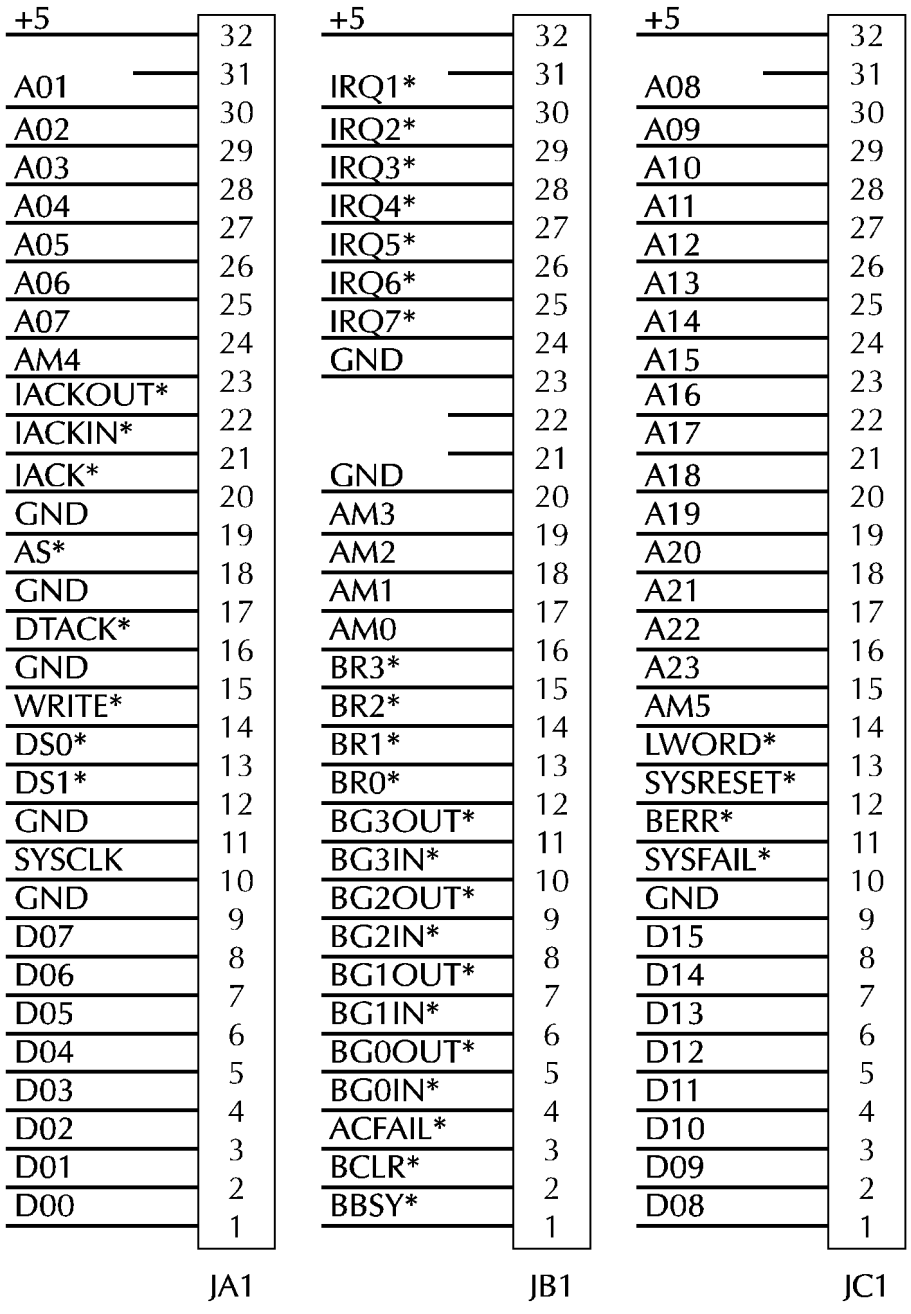


Figure 9. P1 Connector Pinout.

p2a.bmp
3/13/94

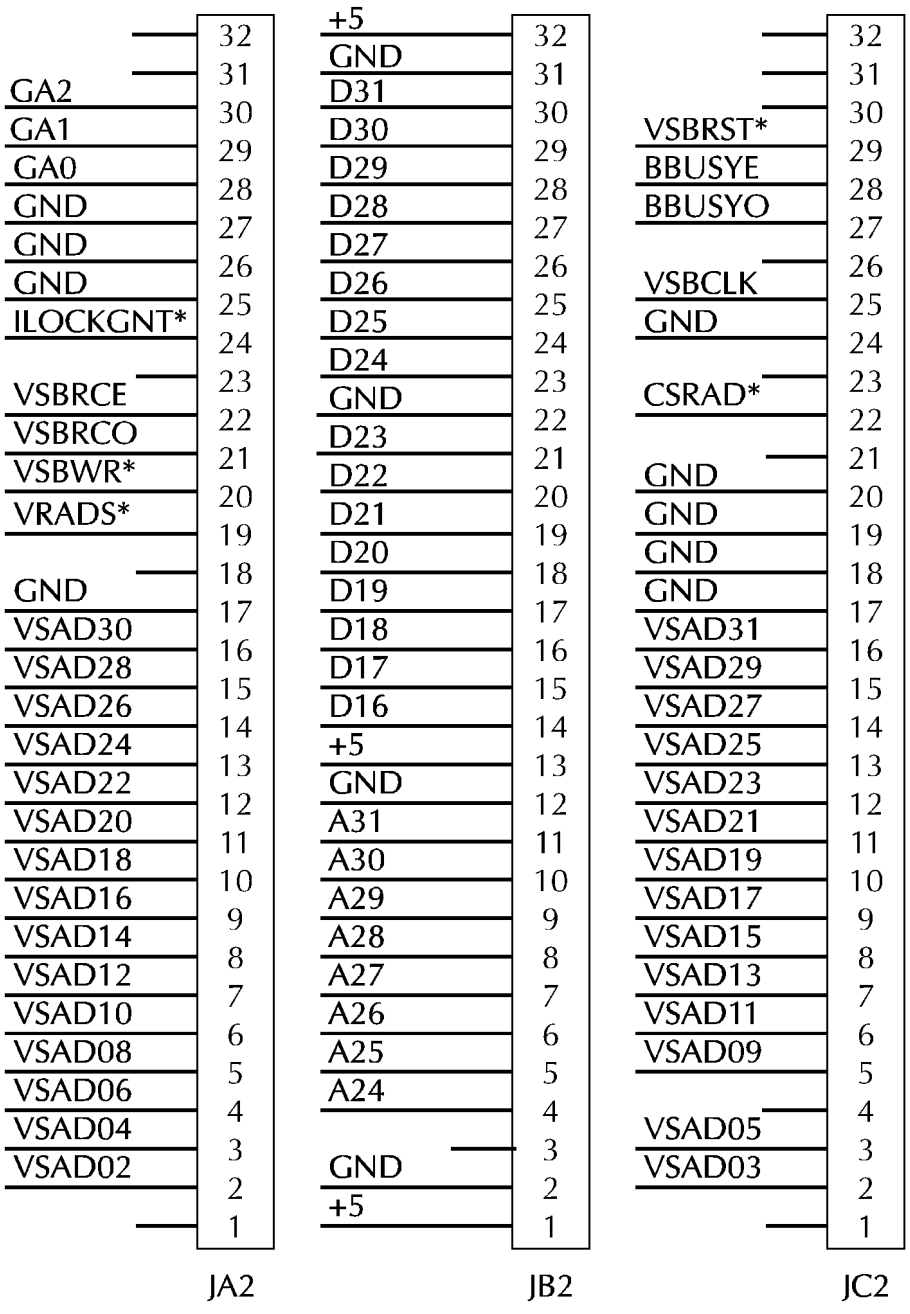


Figure 10. P2 Connector Pinout.

5.4 FRONT PANEL I/O CONNECTORS, ADM31

A serial port (P3) connector, a parallel port (P4) connector, a SCANCLK (scan clock) input (P5) connector, and a GATE input (P6) connector are available on the **ADM31** front panel**.**

- Differentials signals inputs are required for P5 and P6.
- The input impedance Ze of P5 and P6 needs to be 100Ω for proper operation.
- A 34C86 receiver buffer transforms the RS-422 signals of P5 and P6 into a TTL signal.
- The GATE signal of P6 is active when no signal is present at the connector level upon receiving a "low input" signal the state machine scanning is momentarily stopped.

Figure 11 illustrates the location of these four connectors, **Figure 12** illustrates the pinouts of P3, Figure **13** illustrates the pinout of P4, and **Figure 14** illustrates the pinout of P5 and P6.

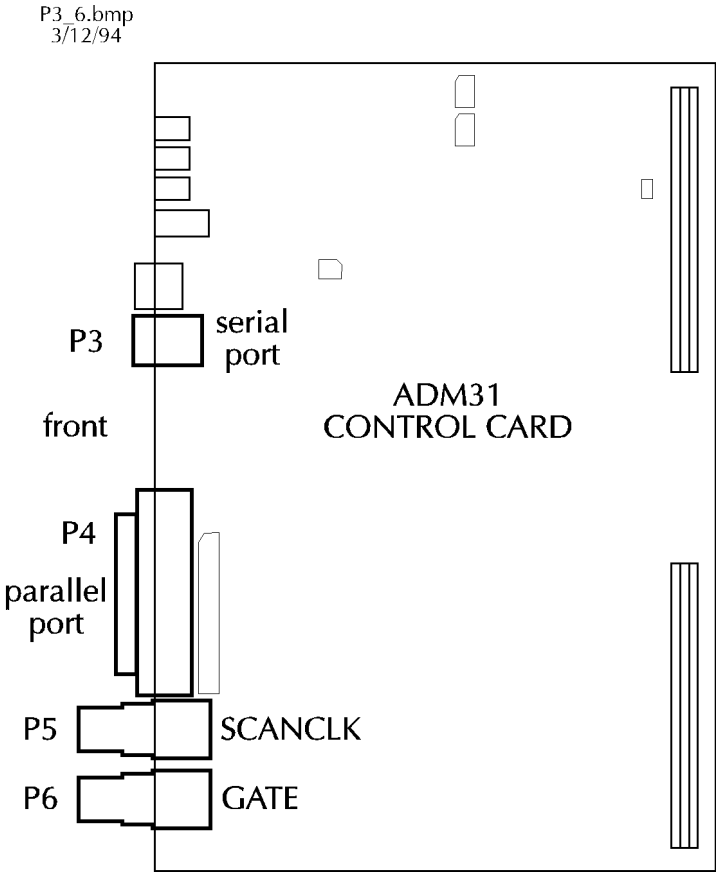


Figure 11. P3, P4, P5, and P6 Connector Location, **ADM31**.

p3.bmp
3/17/94

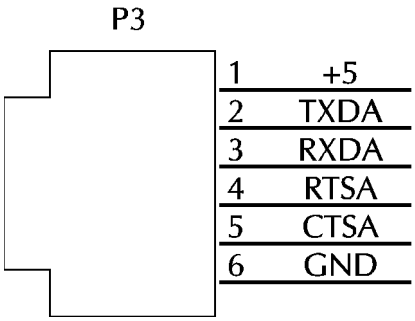


Figure 12. P3 Connector Pinout, **ADM31**.

p4.bmp
3/17/94

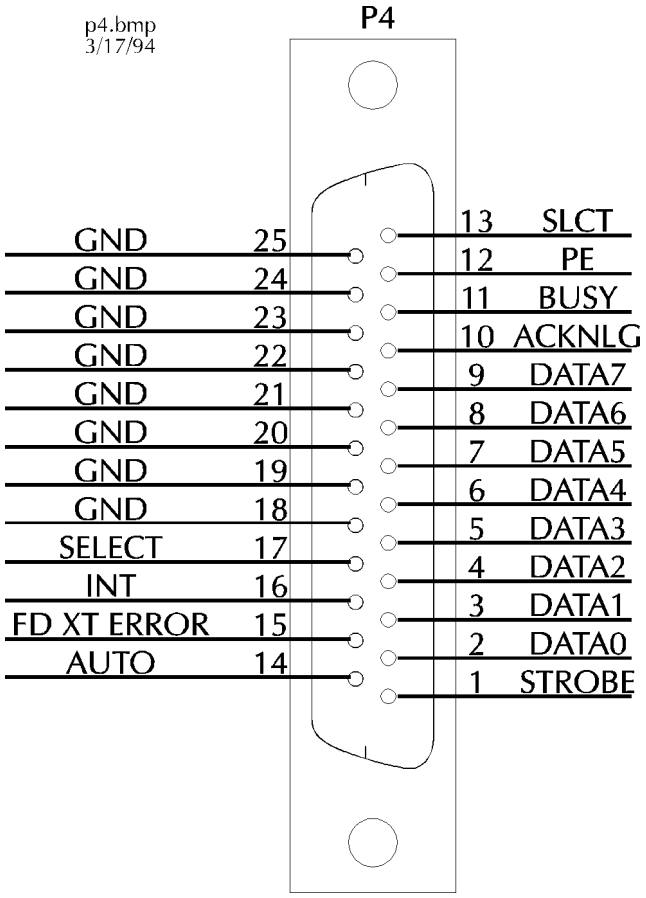


Figure 13. P4 Connector Pinout, **ADM31**.

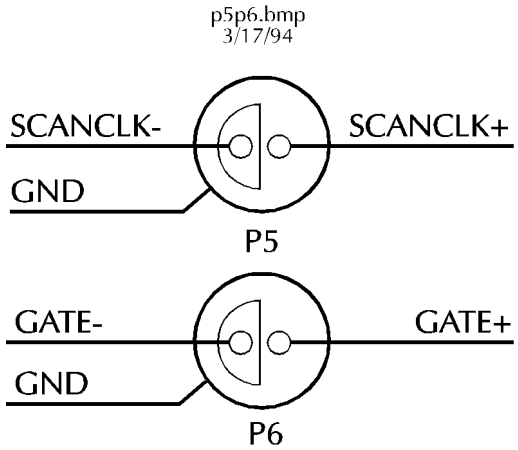


Figure 14. P5 and P6 Connector Pinouts, **ADM31**.

5.5 FRONT PANEL I/O CONNECTORS, AD-48S

The **AD-48S A/D** card has I/O connectors on the front panel, P1 and P2, for 48 single-ended analog channel inputs. P1 contains analog channels 1 through 24, and P2 contains analog channels 25 through 48. **Figure 15** illustrates the connector pinout for both connectors.

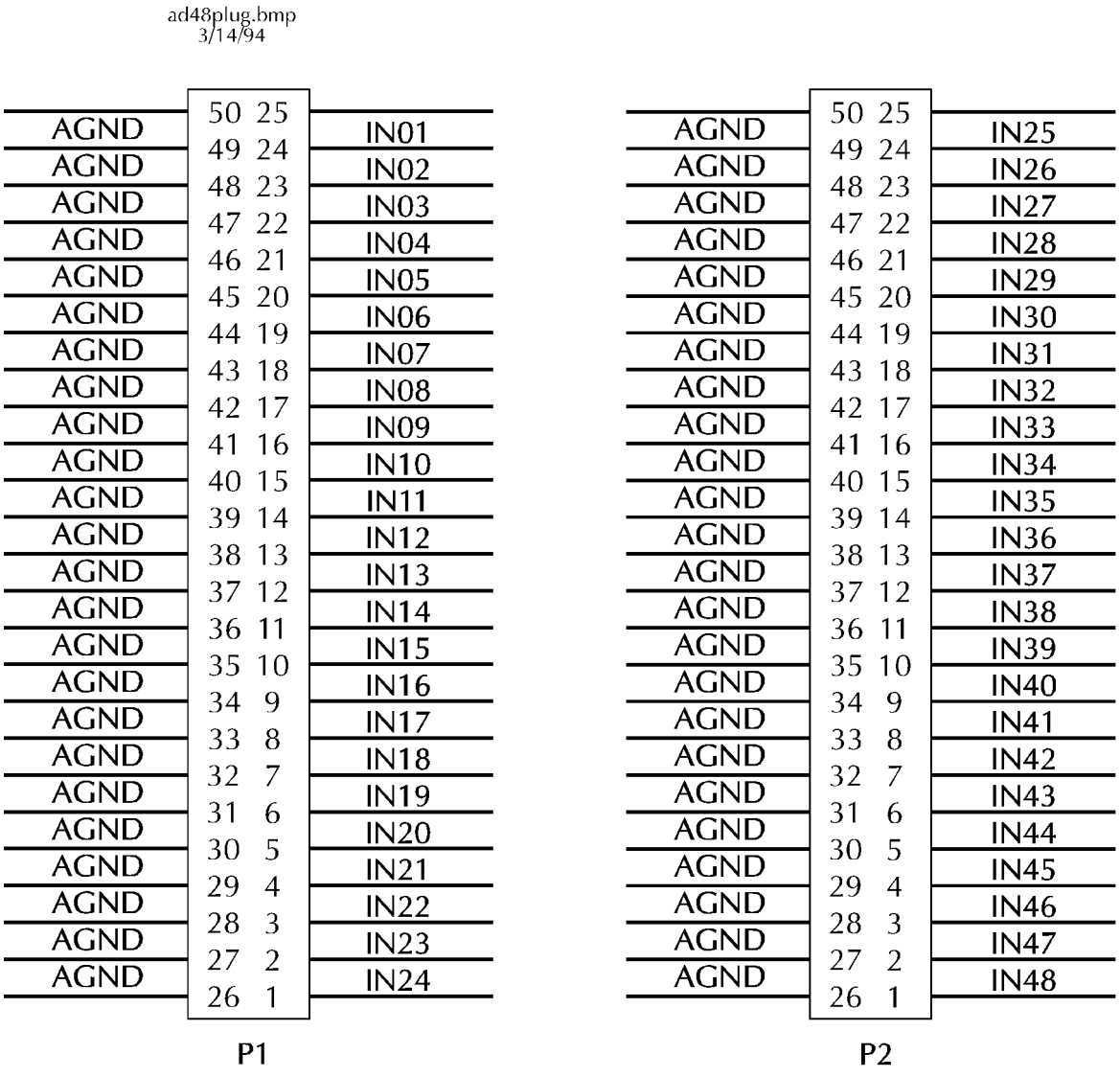


Figure 15. **AD-48S** Connector Pinout.

5.6 FRONT PANEL I/O CONNECTORS, AD-24D

The **AD-24D** A/D card has I/O connectors on the front panel, P1 and P2, for 24 true differential analog channel inputs. P1 contains analog channels 1 through 12, and P2 contains analog channels 13 through 24. **Figure 16** illustrates the connector pinout for both connectors.

ad24plug.bmp
3/14/94

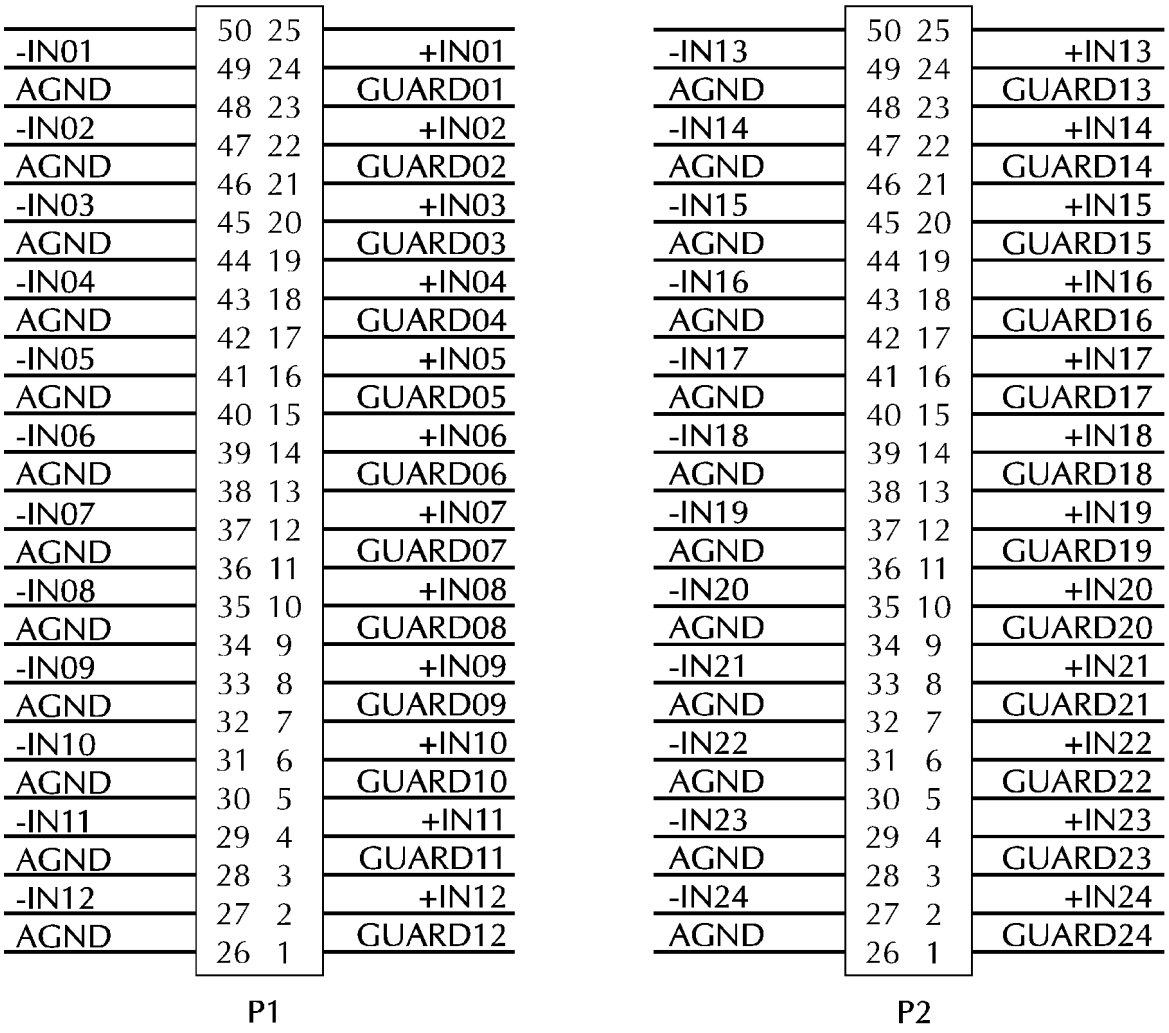


Figure 16. **AD-24D** Connector Pinout.

5.7 SWITCHES

Only the **ADM31** control card has manually operated switches. SW2 controls the **ADM31** control card's VMEbus address; the top three rocker switches form a binary address. The lowest rocker switch position on SW2 controls the **ADM31**'s mode of operation. SW1 controls how the **ADM31** handles reset; SW1 is a three position switch with momentary operation to the left and right. **Figure 17** illustrates where the switches are located on the card, **Figure 18** illustrates SW1's normal switch positioning, **Figure 19** illustrates SW2's normal switch positioning, **Table 7** details the SW1's functions, and **Table 8** details the SW2's functions.

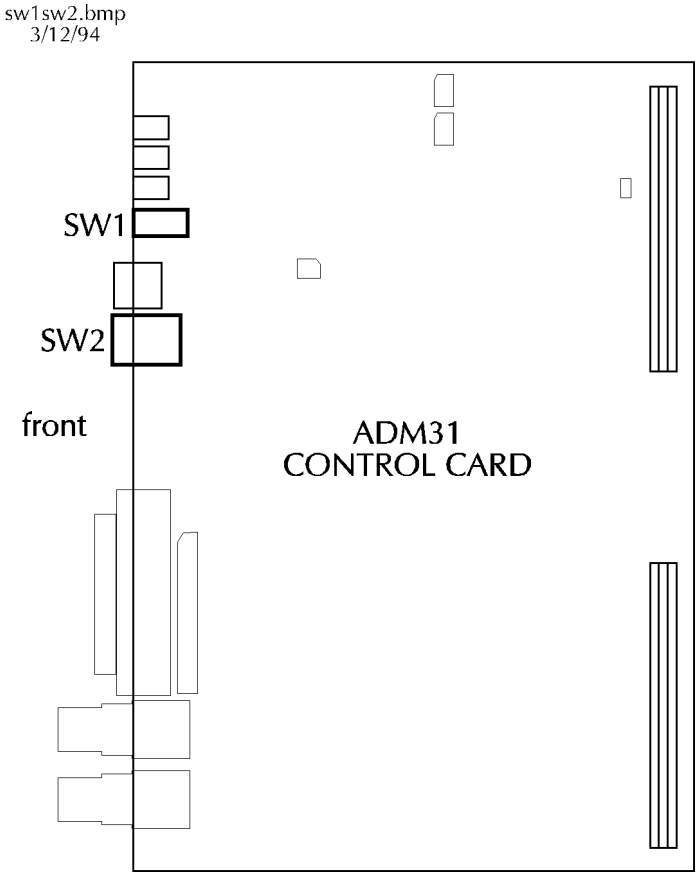


Figure 17. **ADM31**'s Switch Location and Positioning.

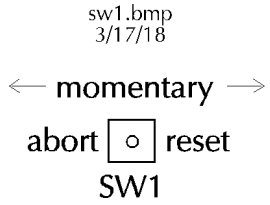


Figure 18. SW1 Normal Switch Positionings.

switch	function
SW1	momentary right = **ADM31** internal power up reset enabled or external reset enabled (or SYSRESET*) if SCON VIC input bit = “0” with jumper W1 installed momentary left = software-based ABORT command stops the active program

Table 7. **ADM31** Control Card SW1 Functions.

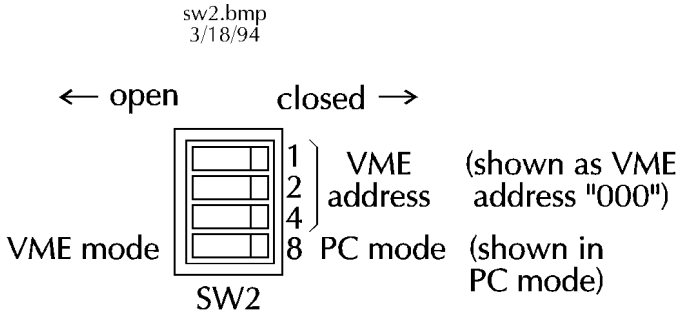


Figure 19. SW2 Normal Switch Positionings.

switches	function
SW2, positions 1, 2, and 4	used to identify the location of the **ADM31** control card in the VMEbus; binary input with 8 possible settings; “000” or all switches closed (moved to the right) are the normal positions
SW2, position 8	**ADM31** control card mode selection “0” = PC master through the serial and parallel port; switch closed “1” = VMEbus host master; switch open

Table 8. **ADM31** Control Card SW2 Functions.

5.8 LED INDICATORS

The following **Table 9** illustrates the various LED indicators that are available on the **ADM31** control card front panel and the functions they support. See **Figure 20** for the location of the LED's.

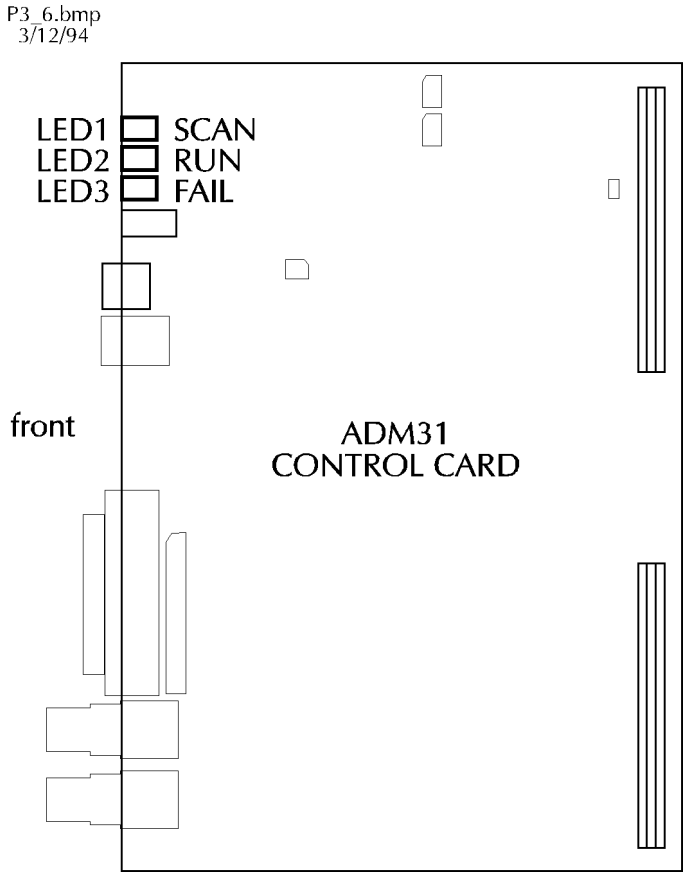


Figure 20. LED Locations.

front panel LED	function
SCAN, LED1	This yellow LED is activated when the A/D converters are active
RUN, LED2	This green LED is activated when the local processor is running in a supervisor mode
FAIL, LED3	This red LED is activated by the SYSFAIL VMEbus signal or the bit #1 in the CTRLREG_1 control register

Table 9. **ADM31** Control Card Front Panel Indicators.

INSTALLATION

6.0 INSTALLATION

The **ADM31** control card and any combination of the **AD-24D** and/or **AD-48S** A/D cards need to be installed together as a standalone or integrated data acquisition system. The P2 VMEbus assembly - the VSBbus card - also needs to be installed on the backside of the VME card rack.

6.1 P2 BUS ASSEMBLY

The P2 VMEbus carries application specific signals required for the **ADM31** data acquisition system only. These signals are carried on the two outside rows of the **ADM31** P2 backplane connector. Therefore, a P2 bus assembly - the VSBbus backplane - needs to be installed behind the VMEbus backplane to connect these applications specific signals for the ADM31 data acquisition system. A standard VSBbus backplane is used for interconnection between modules. See **Figure 21** for an illustration of the P2 bus assembly; both the back view and top view are included.

The VSBbus has three lines - GA0, GA1, GA2 - that can be jumpered to "1" or "0" on the backside of the VSBbus assembly. A board connected to the VSBbus from the front can recognize its own position on the bus. This position can be read from the **STATREG_1** register. Access to the register is allowed only when the state machine has released the bus. The following **Table 10** is an example of an **ADM31** card and two **AD-48S** cards and their corresponding bit assignment. **ADM31** occupies the first slot, and the remaining two **AD-48S** cards the next two adjacent slots.

card	GA0 bit	GA1 bit	GA2 bit
ADM31 control card	0	0	0
AD-48S, first card	1	0	0
AD-48S, second card	0	1	0

Table 10. GA0, GA1, and GA2 Bit Assignment Example.

6.2 P2 BUS TERMINATION RESISTORS

Address lines that are generated on the **ADM31** control card need to be terminated on the backside of the P2 bus assembly. The two outside connectors support bus termination resistors, but not the middle row. If the **ADM31** control card is placed on one end of the P2 bus assembly, install the bus termination resistors on the far end of the P2 bus assembly. The **ADM31** can be the master of the VMEbus and also generate and receive interrupts. If the jumpers are not configured properly on the backplane, these jumpers are prime suspects of systems problems.

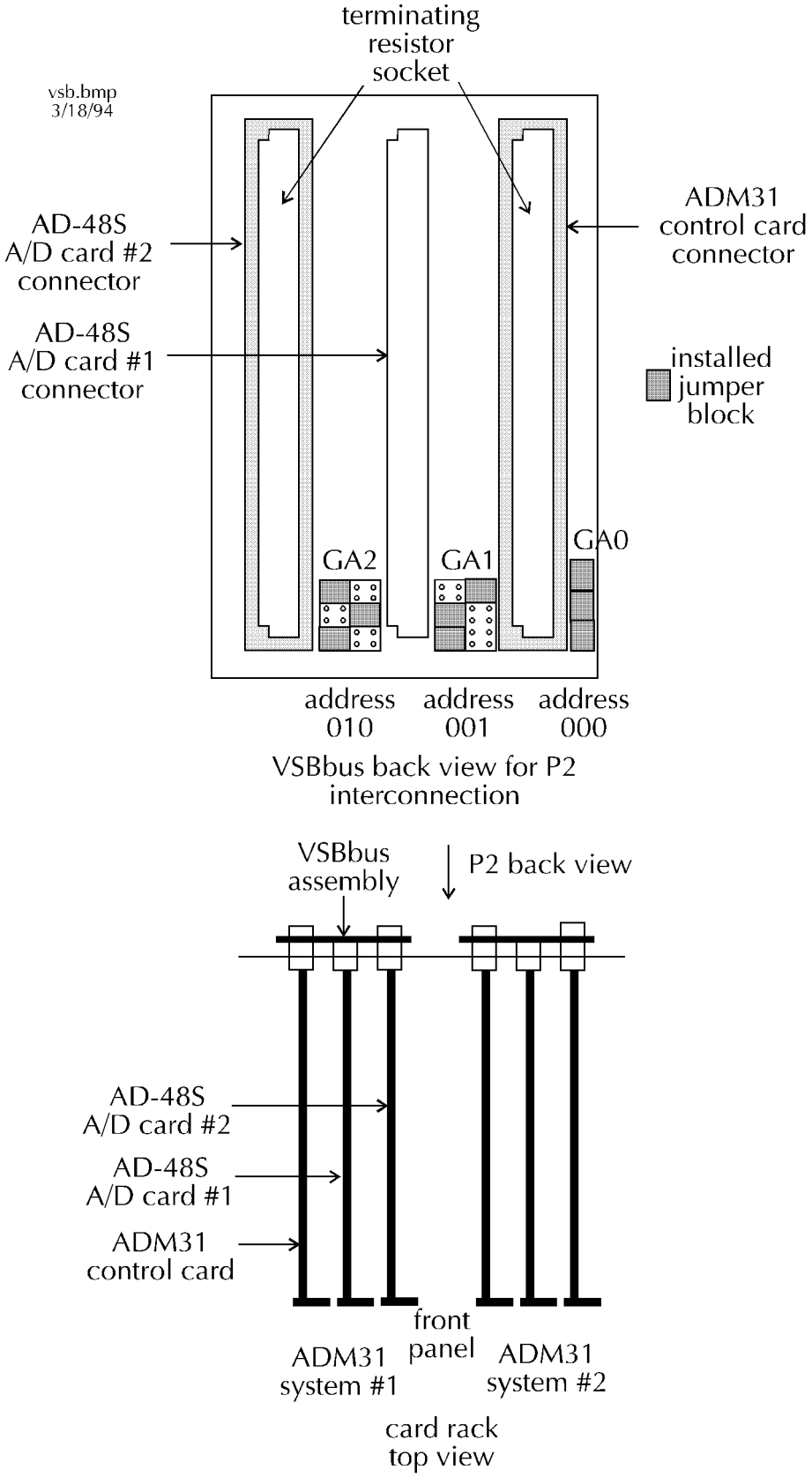


Figure 21. Back and Top View of the VSBbus Card and **ADM31** Data Acquisition System.

6.3 CARD INSTALLATION

Each of the three cards in the ADM31 family are dual high VME cards, and need to be installed in a VMEbus card cage in adjacent card slots. Make sure that the cards are completely seated and screwed down. See **Figure 22** for a suggested front view mechanical layout of a three card data acquisition system using the **ADM31** and two **AD-48S** cards.

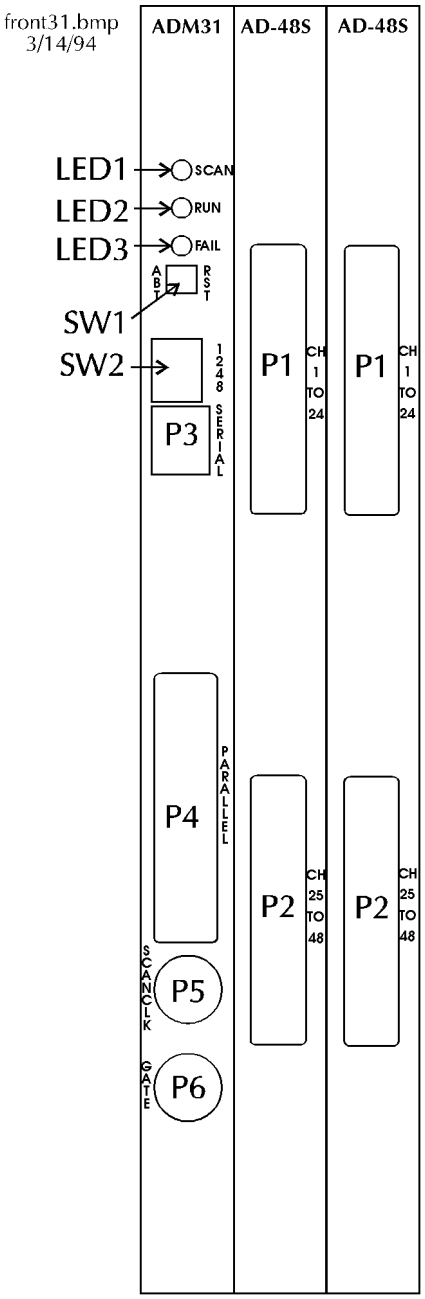


Figure 22. Suggested Card Installation.

THEORY OF OPERATION

7.0 THEORY OF OPERATION

Initialization parameters are downloaded through the VMEbus to the local **ADM31** control card memory. Upon receiving the parameters, the 68EC30 programs the timers and loads the channels with the corresponding timer into the CHRAM. Each timer shares 256 bytes of the CHRAM memory.

The state machine waits to receive an external or internal gate. Upon receiving an internal or external clock, all the A/D converters start a conversion at the maximum speed define by the fastest channel and convert synchronously. The state machine waits to receive a BUSY signal; it then activates the first location assigned to the timer number 0. The sampled DATA and the channel number are stored in the first memory location. A counter increments the address for the next sampling result.

7.1 KEY FEATURES

- 68EC030 processor running at up to 24 MHz
- VIC068 VME interface chip with support for slave block transfer
- VAC068 VME and local interface with support for master block transfer
- Up to Six Mbytes of SRAM for analog to digital converted data
- Up to128 Kbytes of SRAM for communication between host and local processor
- Up to 512 Kbytes of EPROM
- Up to 64 Kbytes of EEPROM
- External and internal scan trigger
- External and internal gate signal
- One RS-232C interface
- One Parallel port interface (COM_2)
- Full VMEbus Rev C compatible
- Full VME master /slave capabilities
- Eight programmable scanning timers

7.2 LOCAL RESOURCES

The **ADM31** control card's resources include:

- the MC68EC030 microprocessor,
- the VIC and the VAC VME interface chips,
- VME backplane dual-port buffer memory,
- timers for data acquisition control,
- a serial port,
- a LPT1 compatible parallel port,
- EPROM,
- EEPROM, and
- channel SRAM for data acquistion storage.

7.2.1 PROCESSORS

The **ADM31** base board module use a high performance processor. A MC68EC030 32-bit processor handles communication with the VME host and initiates data transfers on the VME bus. The 68EC30 in conjunction with the VIC068 and VAC068 support chips facilitate stand-alone operation as a VME bus master or as an intelligent slave device.

7.2.2 SAMPLE BUFFER MEMORY

The **ADM31** is equipped with 6 Mbytes of dual ported 70 ns SRAM devices. This SRAM is used to store the data that has been sampled by the A/D sections. Internally, the SRAM is organized as a 4M X 24 bit block. Externally, the SRAM appears on the VMEbus as:

- 8 Mbytes 32 bit wide SRAM with the following structure:
Condition: bit #7 of CTRLRREG_1 = "0" ($00)

VME base address is defined in the VAC68 register $FFFD0200 and $FFFD0300

SAMPLE #1 Base address + $800000 + $00

D31 - D24	D23 - D16	D15 - D08	D07 - D00
DATA15-08	DATA07-00	CHANNEL#	NOTE 1

SAMPLE #2 Base address + $800000 + $04

D31 - D24	D23 - D16	D15 - D08	D07 - D00
DATA15-08	DATA07-00	CHANNEL#	NOTE 1

NOTE 1:

On VME bus read access, D00-D07 are read back as zeros.
On VMEbus write access, D00-D07 writes are not enabled.
On VMEbus or local write access, only D08-D15 can be written

- 4 Mbytes 32 bit wide SRAM with the following structure:

Condition : bit # 7 of CTRLREG_1 = "1" ($80)

SAMPLE #1 + SAMPLE #2 Base address + $800000 + $00

D31 - D24	D23 - D16	D15 - D08	D07 - D00
DATA 15-08	DATA 07-00	DATA 15-08	DATA 07-00
SAMPLE # 1		**SAMPLE # 2**	

SAMPLE #3 + SAMPLE #4 Base address + $800000 + $04

D31 - D24	D23 - D16	D15 - D08	D07 - D00
DATA 15-08	DATA 07-00	DATA 15-08	DATA 07-00
SAMPLE # 3		**SAMPLE # 4**	

NOTE 1:

On VMEbus write access, D00-D07 writes are not enabled.
On VMEbus or local write access, data can be written.

7.2.3 HOST COMMUNICATION MEMORY

The **ADM31** module contains a 128 Kbytes dual ported SRAM which is shared by the VMEbus and the local 68EC30 processor. This memory is mapped to a user defined space on the VMEbus. The 68EC30 uses this memory for program storage and to process information downloaded from the VME host. Base address of the HOST COMMUNICATION MEMORY is defined using the VAC068 register $FFFD0200 and $FFFD0300. It occupies the lower part of the 16 Mbytes region seen by the VMEbus. Th UPPER part of the region is for the DATA SAMPLE RAM. Some redundancy is generated.

The host communication SRAM is independent of the SRAM used for the sample buffer. The separation of program from sample data memory increase efficiency of the digitizer that run independely of the activity on the local bus.

7.2.4 TIMERS

Eight 16 bits timer allow the user to select up to eight different sample clock rate in 65535 steps. Each channel can be connected to one of the eight timer.

7.2.5 TIMER SAMPLE CLOCK

The sample clock reference is derived from either a ÷ 1 or ÷2 prescaler which is fed by an on-board crystal reference. This reference is routed to a 32 bit timer providing an effective internal sample clock rate of 200 Hz to 200 KHz.

An external clock reference, routed from the front panel, provides external trigger support. The external trigger is TTL differential with programmable active edge. Internal or external trigger operation is defined by software.

7.2.5 CHANNEL RAM

The channel RAM stores the activated channel.

7.2.6 VMEbus INTERFACE

The **ADM31** module uses the VIC068 and VAC068 to provide an interface between the VMEbus and local busses. These two industry standard products provide maximum performance for a VMEbus master/slave module. The VIC068 provides all VME bus system controller functions plus many other features which simplify the development of a VME interface. Its CMOS high drive buffers provide direct connection to the address and data lines. It also connects directly to the arbitration, interrupt, address modifier, utility and strobe lines. The VAC068 associated with the VIC068 provide a complete solution for VMEbus master/slave interface.

The VAC068 design includes VMEbus and I/O DMA capability for 32-bit processors. 42 registers allow complete local memory map decoding and control signal generation such as :

- Programmable LDTACK*, IOWR*, IORD*, CSx*
- Dual UARTs
- Block transfers over 256-byte boundaries with :
- Address counters for VMEbus A[31:8] and local LA[31:8] to complete the VIC068 counters.
- Double path capabilities
- Local DMA capabilities

7.3 AD-48S AND AD-24D OPERATION

All the A/D converter are converting at the same time when they receive a trigger signal provide by the **AMD31** control card state machine through the P2 connector. Conversion starts with the reception of the RCE (start conversion signal) by the **AD-48S** OR **AD-24D** logic. Duration of the signal is 80 nS. Selection of the 200KSPS mode is made through a latch controlled by the **ADM31** control card. A PAL provides the appropriate signal to each A/D converter.

OPERATING INSTRUCTIONS

8.0 OPERATING INSTRUCTION

The data acquisition can be controlled by a VME system controller with the **ADM31** data acquisition system in the VME mode, or from the **ADM31** control card itself in a standalone configuration with an externally connected PC in the PC mode.

8.1 INTERNAL OPERATION

Either the system controller or **ADM31** control card can initiate data acquisition internally. By momemtarily operating SW1 (VME or PC master mode toggle switch), either the system controller (VME) or the **ADM31** control card (PC mode) will start the scanning process. The **ADM31** control card provides the clocking and timing functions.

8.2 EXTERNAL OPERATION

A PC can be attached to the **ADM31** data acquisition system. A serial port connection to P3 on the front panel of the **ADM31** control card sends and receives commands; the parallel port P4 of the **ADM31** sends data for graphic display update on the PC monitor. P4 is LPT1 compatible.

8.3 EXTERNAL CONTROL

An external clock and gate can control the scanning process regardless of whether the a system controller or the **ADM31** control card has initiated the scanning process. In addition, an externally connected PC can also monitor the scanning process through the parallel port. The PC's LPT1 port is directly connected to the P4 parallel port with the port providing the aquired data path for PC screen display.

8.3.1 EXTERNAL SCAN CLOCK

The front panel external SCAN clock is derived from a user supplied differential TTL signal with a minimum frequency of 1 Hz to a maximum sampling frequency of 200 KHz. The active edge of the SCAN clock is software programmable. The external SCAN clock is also enabled or disabled through software control. The SCAN clock initiates the reading of a the channel listed on the channel list once and wait until the next define active edge. The clock EDGE is selected by the bit # in the CTRLREG_2. Minimum clock pulse with must by $\geq$ 300 nsec.

8.3.2 EXTERNAL GATE

The front panel external GATE is derived from a user supplied differential TTL signal. It is active high when not connected, when set to a "low" level the state machine is waiting to acquire sampling data. This signal synchronizes with the scanning clock. An active scan function will occur when both the external gate and clock are active.

8.4 MEMORY ORGANIZATION

The **ADM31** control card's overall memory map is displayed in **Figure 23**; the local I/O map in found in **Figure 24**. The VAC internal registers are in **Table 11** and the VIC internal registers are in **Table 12**. This memory consists of:

- EPROM for program storage

- EEPROM for programmable parameter storage that needs to be retained even with power removed
- dual-access SRAM common to both the ADM31 control card and the VME system
- channel SRAM for data acquisition storage; the SRAM is indirectly accessible from other VME backplane controllers

The VAC controls the basic boundaries of the memory space with three programmable boundaries and three fixed memory boundaries supporting EPROM and EEPROM, VMEbus dual byte (16 bit) access, and local I/O including the VAC's own register set. Therefore, the overall memory space is divided into 6 regions. In the ADM31 control card, the programmable boundaries are:

- region 0/region 1 boundary = $08000000
- region 1/region 2 boundary = $10000000
- region 2/region 3 boundary = $E0000000

The fixed memory boundaries are:

- region 3/region 4 boundary = $FF000000
- region 4/region 5 boundary = $FFF00000
- region 5/region 6 boundary = $FFFE0000

The **ADM31** control card supports up to a 4 Mbit EPROM for program storage. On initialization, this EPROM will be used to bootstrap the 68EC030. The 68EC030 bootstrap code will copy itself to local RAM for better performance.

Size of the EPROM is selecteable from 25Kbits to 1 Mbits using the jumper W4.

An on-board 64K X 8 EEPROM is used to store system configurations, A/D calibration offsets or other valuable data. The EEPROM can be programmed only if the bit #4 WRE2PRNGNT of the CTRLREG_1 register is set.

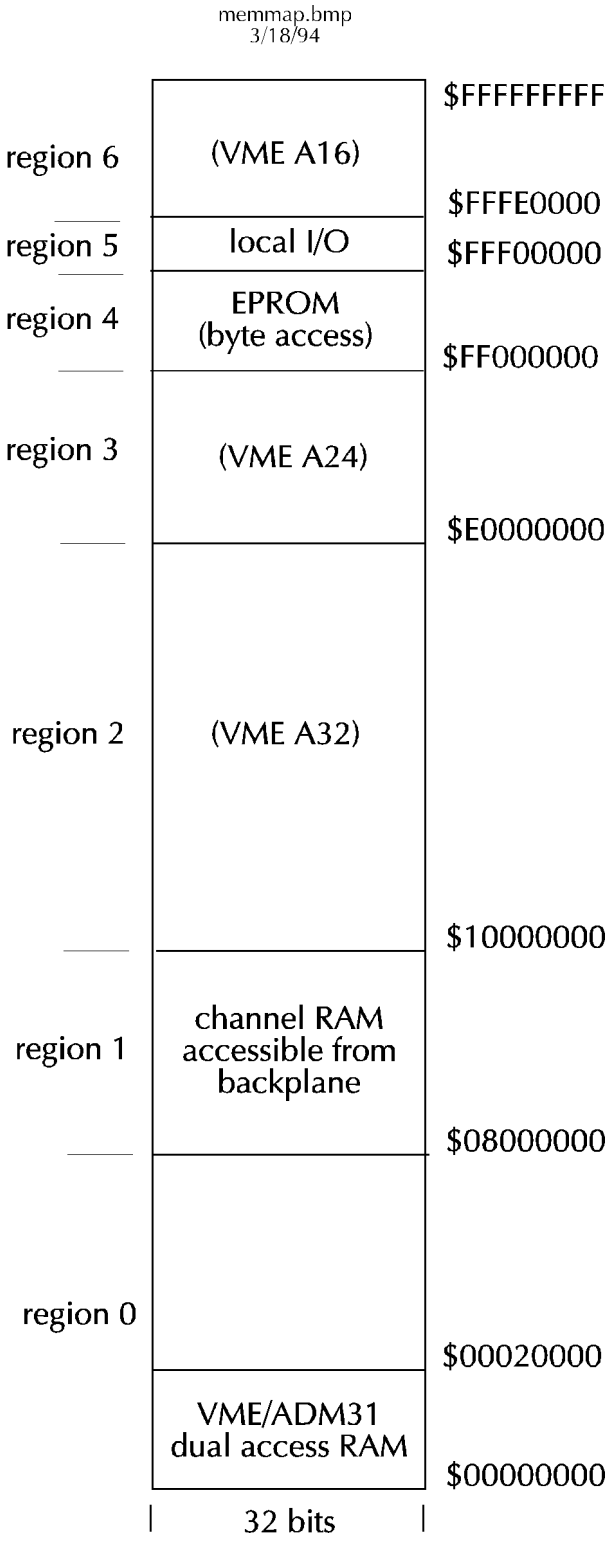


Figure 23. Overall System Memory Map.

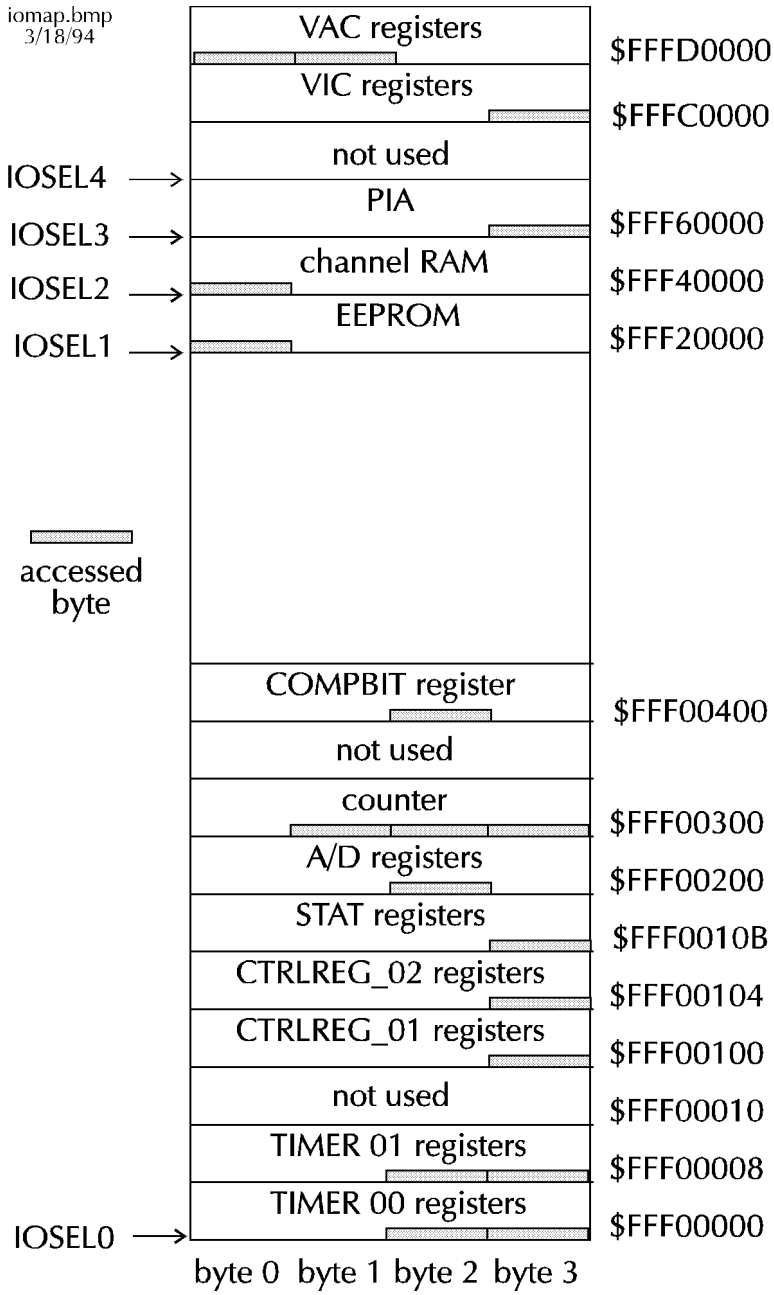


Figure 24. I/O Memory Map.

local address	register description	size (bits)
FFFD 00XX	SLSEL1* address mask register	16

FFFD 01XX	SLSEL1* base address register	16
FFFD 02XX	SLSEL0* base address register	16
FFFD 03XX	SLSEL0* address mask register	16
FFFD 04XX	ICFSEL* base address register	16
FFFD 05XX	DRAM upper limit mask register	16
FFFD 06XX	boundary 2 address register	16
FFFD 07XX	boundary 3 address register	16
FFFD 08XX	A24 base address register	13
FFFD 09XX	region 1 attribute register	6
FFFD 0AXX	region 2 attribute register	6
FFFD 0BXX	region 3 attribute register	6
FFFD 0CXX	IOSEL4* DSACK control register	16
FFFD 0DXX	IOSEL5* DSACK control register	16
FFFD 0EXX	SHRCS* DSACK control register	16
FFFD 0FXX	EPROMCS* DSACK control register	16
FFFD 10XX	IOSEL0* DSACK control register	16
FFFD 11XX	IOSEL1* DSACK control register	16
FFFD 12XX	IOSEL2* DSACK control register	16
FFFD 13XX	SLSEL3* address mask register	16
FFFD 14XX	decode control register	16
FFFD 15XX	interrupt status register	8
FFFD 16XX	interrupt control register	16
FFFD 17XX	device location register	6
FFFD 18XX	PIO data out register	14
FFFD 19XX	PIO pin register	14
FFFD 1AXX	PIO direction register	15
FFFD 1BXX	PIO function register	16
FFFD 1CXX	CPU clock divisor register	8
FFFD 1DXX	UART channel A mode register	12
FFFD 1EXX	UART channel A transmit data register	8
FFFD 1FXX	UART channel B mode register	12
FFFD 20XX	UART channel A receiver FIFO	11
FFFD 21XX	UART channel B receiver FIFO	11
FFFD 22XX	UART channel B transmit register	8
FFFD 23XX	UART channel A interrupt mask register	6
FFFD 24XX	UART channel B interrupt mask register	6
FFFD 25XX	UART channel A interrupt status register	8
FFFD 26XX	UART channel B interrupt status register	8
FFFD 27XX	timer data register	16
FFFD 28XX	timer control register	8
FFFD 29XX	VAC068A ID register	16

Table 11. VAC Control Registers.

local address	register description
FFFC 0003	VMEbus interrupter interrupt control register
FFFC 0007-1F	VME bus interrupt control registers 1-7
FFFC 0023	DMA status register
FFFC 0027-3F	local interrupt control registers 1-7
FFFC 0043	ICGS interrupt control register
FFFC 0047	ICMS interrupt control register
FFFC 004B	error group interrupt control register
FFFC 004F	ICGS vector base register
FFFC 0053	IDMS vector base register

FFFC 0057	local interrupt vector base register
FFFC 005B	error group interrupt vector base register
FFFC 005F	interprocessor communications switch register
FFFC 0063-73	interprocessor communications registers 0-4
FFFC 0077	interprocessor communications register 5
FFFC 007B	interprocessor communications register 6
FFFC 007F	interprocessor communications register 7
FFFC 0083	VMEbus interrupt request status register
FFFC 0087-9F	VMEbus interrupt vector base registers 1-7
FFFC 00A3	transfer timeout register
FFFC 00A7	local bus timing register
FFFC 00AB	block transfer definition register
FFFC 00AF	interface configuration register
FFFC 00B3	arbiter/requester configuration register
FFFC 00B7	address modifier source register
FFFC 00BB	bus error status register
FFFC 00BF	DMA status register
FFFC 00C3	slave select 0 control register 0
FFFC 00C7	slave select 0 control register 1
FFFC 00CB	slave select 1 control register 0
FFFC 00CF	slave select 1 control register 1
FFFC 00D3	release control register
FFFC 00D7	block transfer control register
FFFC 00DB	block transfer length register 0
FFFC 00DF	block transfer length register 1
FFFC 00E3	system reset register
FFFC 00EB-FF	reserved locations

Table 12. VIC Control Registers.

8.5 VME MODES OF OPERATION

The VIC068 supports the three arbitration schemes as defined by the VME bus specifications:

- PRI prioritized
- RRS round robin
- SLG single level

8.5.1 BUS MASTER OPERATIONS

The VIC068 within a FAIR REQUEST scheme uses the different modes of bus releases:

- ROR Release on request
- RWD Release when done
- ROC Release on clear
- BCAP Bus capture and hold

The VIC supports the following VMEbus standard address modes and data transfer types :

- A24 / D08 (OE)
- A24 / D16
- A24 / D32, A24 /D32 BLT, A24 /D32 UAT

The VIC supports the following VMEbus extended address modes and data transfer types :

- A32/ D08 (OE)
- A32/ D16
- A32 / D32, A32 /D32 BLT, A32/D32 UAT

The VIC supports the following VMEbus short address modes and data transfer types :

- A16 / D08 (OE)
- A16 / D16

8.5.2 BUS SLAVE OPERATIONS

The VIC068 supports access to :

- Inter processor Communications Registers (ICRs)
- Inter processor Global Switches Registers (ICGRs)
- Inter processor Communications Module Switches (ICMs)
- On board dual ported RAM

As a VMEbus Slave, the **ADM31** board provides user selectable addresses within VMEbus short, standard, and extended address boundaries. As a VMEbus Slave, the **ADM31** also supports the following VMEbus short address modes and data transfer types :

- A16 / D08 (OE)
- A16 / D16

The **ADM31** also supports the following VMEbus standard address modes and data transfer types :

- A24 / D08 (OE)
- A24 / D16
- A24 / D32, A24 /D32 BLT, A24 /D32 UAT

In addition, the **ADM31** supports the following VMEbus extended address modes and data transfer types :

- A32/ D08 (OE)
- A32/ D16
- A32 / D32, A32 /D32 BLT, A32/D32 UAT

8.5.3 VME BUS BLOCK TRANSFERS

The VIC068 is capable of both performing (as master) and receiving (as slave) block transfers. The master VIC068 supports two modes of block transfer on the VMEbus:

- MOVEM type block transfer
- DMA type block transfer

Block transfer lengths beyond the VMEbus specification (256 bytes) are possible when the VIC068 is associated with the VAC068 without any glue logic. The VIC068 and the VAC068 combination provide a set of two 32 bit address counters which may drive either the VME or local busses.

RELATED DOCUMENTS

9.0 RELATED DOCUMENTS

The following publications found in **Table 13** are necessary for more detailed knowledge of the data acquisition system, VLSI and component operation.

Document Title	Publication Number
VAC068/VMEbus Address Controller	UG009/08901
VIC068/VMEbus Interface Controller	UG008/02902
M68EC30 Microprocessor Reference Manual	M68EC30UM
The VME Specification	HB212
ADS7805PB Datasheet/Burr-Brown	PDS-1157A
INA111 Instrumentation Amplifier	PDS-1143B
OP2107 Operational Amplifier	PDS-863B
OP-42 Operational Amplifier	7/89 REV C
9513 timer	
65C22 parallel device	

Table 13. Reference Documentation.

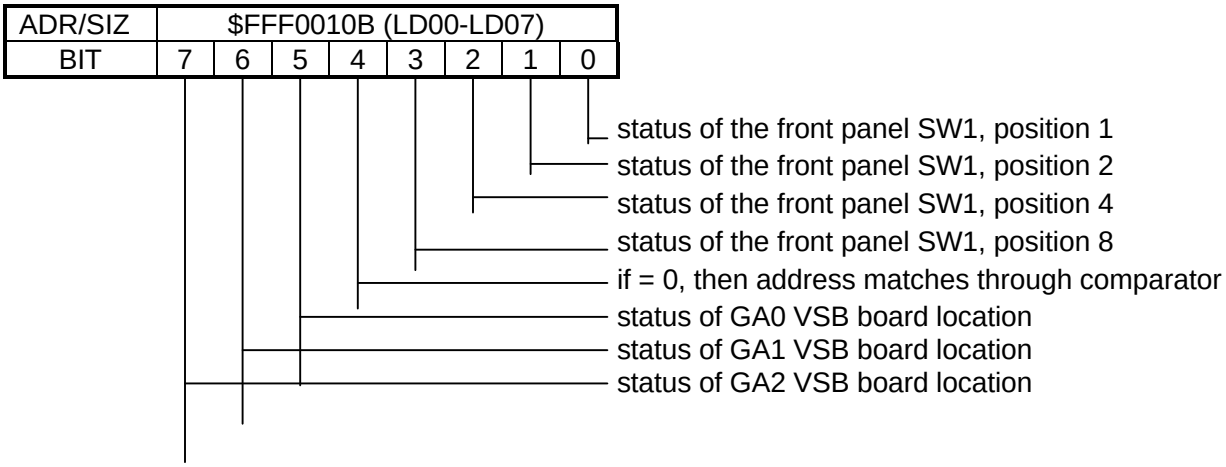
10.0 REGISTER SETS

Various on-board resources are managed through a local control register:

- software SYSFAIL bit
- EEPROM write protection
- half full and 3/4 full SRAM interrupts
- internal/ external switch trigger
- edge trigger selection

10.1 STATUS REGISTER

The status register provides current system configuration for **ADM31** access.



10.2 COUNTER REGISTER

$FFF00300 32 bits LD00-LD31

This 32 bit register can read the state of the counter used to drive the address of thr DATARAM. Care must be taken not to read the counter while the state machine is active. False reads can occurs.

10.3 TIMER REGISTERS

The ADM31 use two Am9513 timer from AMD. These timers have a base clock CLKTIM of 3Mhz provide by the PAL REGCNT. Internal clock is provide by the clock divider of the Am9513 which divides the base clock depending of the value of MM15 register. Source for the SCAN clock is internal or external. Gating for providing a "window" of acquisition is internal or external. A set of bit from the CTRL_1 and CTRL_2 control registers located at address $ FFF00103 and $FFF00107 give the different possibilites. The following **Table 14** illustrates the various clock source possibilities.

SCAN clock source	TRIGEXT	TRIGEXTPS
INTERCLK (internal)	0	X
SCANCLK (external)	1	0
SCANCLK (external) divide by timer 5 (AM9531-1)	1	0

Table 14. SCAN Clock Source Possibilities.

Timer number 10 (Am9513-2) is used as a delay to request the bus just before the acquisition is finished to speed the process. It must be program to 9 uS for normal sampling up to 100 KSPS or to 4.5 uS for sampling above 200 KSPS.

10.4 SERIAL PORT REGISTERS

ADM31 provides a serial port for diagnostic support through the VAC068.

10.5 PARALLEL PORT REGISTERS

ADM31 provides a parallel port for data transfert when the system is use with a PC terminal (PORT 2 bidirectional port). A 65C22 is used as parallel port. An interrupt LIRQ4 can be generated if programmed at the level of the 65C22 and VIC068. Signals description is provided in appendix.

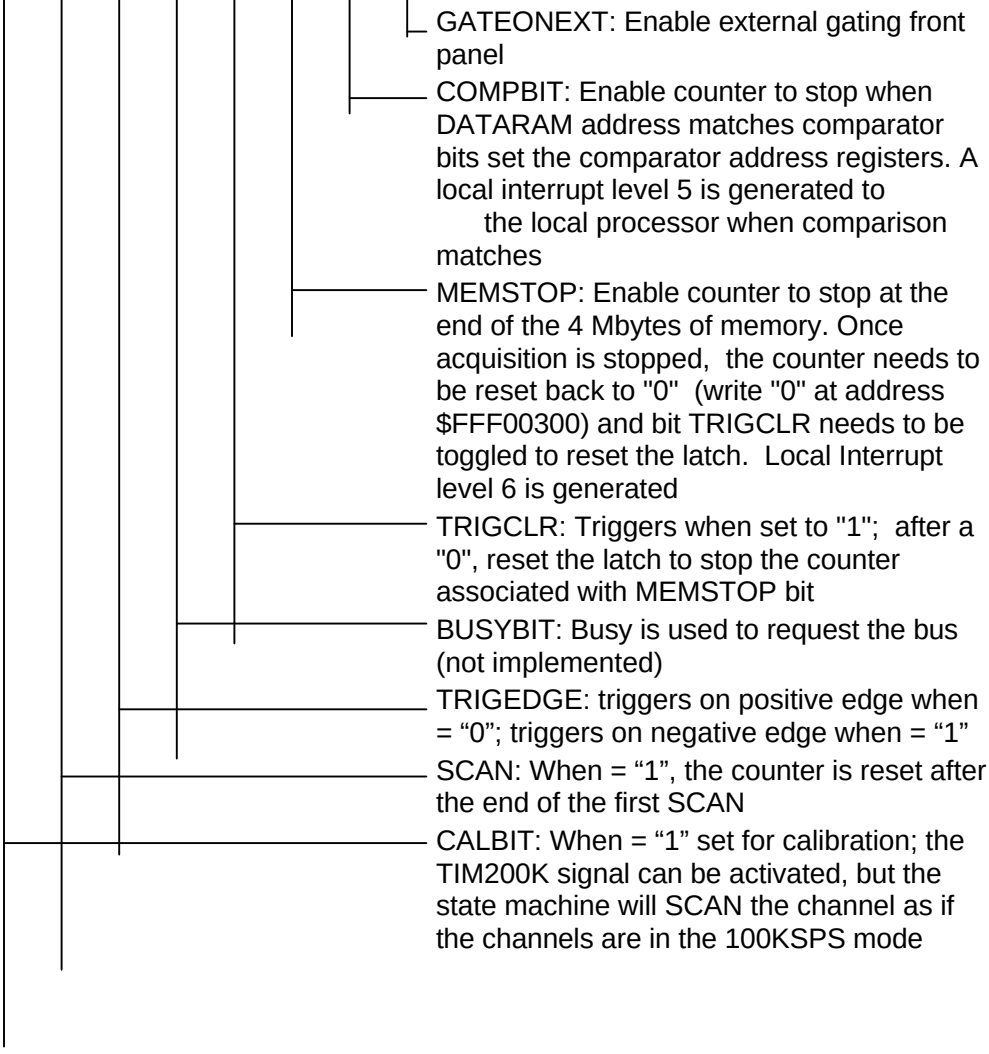
10.6 CTRL REG1 REGISTER

ADR/SIZ	$FFF00103 (LD00-LD07)							
BIT	7	6	5	4	3	2	1	0

- TRIGEXT: Sampling clock is External
- TRIGEXTPS: External Sampling clock needs a prescaler
- TRIGBIT: Start locals timers
- CNTRST: Not used
- WRE2PRNGNT: Enable write to the Flash EPROM
- SYSBIT: Drive "on" the front panel "RED" led
- TIM200K: 200 KSPS mode (timer 0)
- ONLY16: The data provide by the ADM31 to the VMEbus are the A/D data only; Address 0 contains data from the first sampled channel; Address 2 contains the second data sampled etc....

10.7 CTRL REG2 REGISTER

ADR/SIZ	$FFF00107 (LD00-LD07)							
BIT	7	6	5	4	3	2	1	0

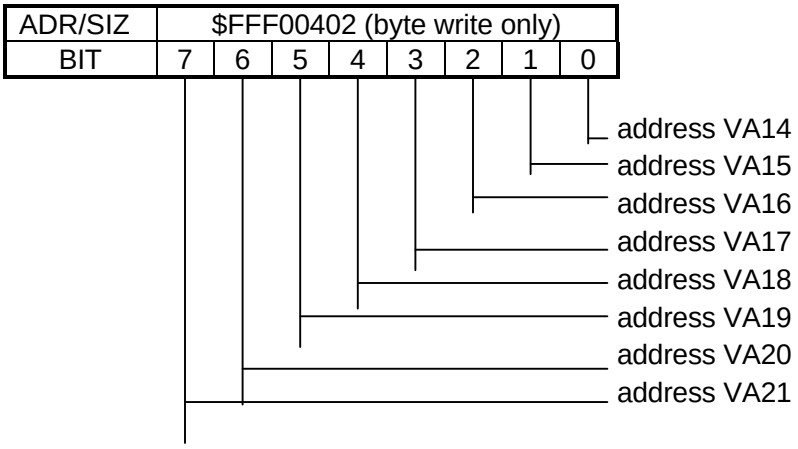


- GATEONEXT: Enable external gating front panel
- COMPBIT: Enable counter to stop when DATARAM address matches comparator bits set the comparator address registers. A local interrupt level 5 is generated to the local processor when comparison matches
- MEMSTOP: Enable counter to stop at the end of the 4 Mbytes of memory. Once acquisition is stopped, the counter needs to be reset back to "0" (write "0" at address $FFF00300) and bit TRIGCLR needs to be toggled to reset the latch. Local Interrupt level 6 is generated
- TRIGCLR: Triggers when set to "1"; after a "0", reset the latch to stop the counter associated with MEMSTOP bit
- BUSYBIT: Busy is used to request the bus (not implemented)
- TRIGEDGE: triggers on positive edge when = “0”; triggers on negative edge when = “1”
- SCAN: When = “1”, the counter is reset after the end of the first SCAN
- CALBIT: When = “1” set for calibration; the TIM200K signal can be activated, but the state machine will SCAN the channel as if the channels are in the 100KSPS mode

10.8 COMPBIT REGISTER

This register is used with an 8 bit comparator to detect the active location of the state machine use of the DATARAM. The comparator compares the addresses of the DATARAM with the content of the register. Minimum definition is 16 Ksamples. Upon a match, the signal LIRQ5* is activated (active low). This signal is connected to the VIC068 as local interupt 5.

The bit # 1 COMPBIT from the CTRLREG_2 will stop the state machine if set to a "1". The interrupt is disabled by moving the comparison upper address. The processor can disable the interrupt inside the VIC068. See the VIC068 programming manual for more information. This comparator is very useful when used as a pointer to start a DMA transfer or request when the state machine has already filled a portion of the memory. Care must be taken depending on the acquisition speed and DMA size not to create a PASSED state within the state machine. The comparator can be move along the memory until the memory is filled.



10.9 AD-48S REGISTERS

Each **AD-48S** card has the following registers activated by the signal CSADREG*. Selection between the **AD-48S** module belonging to one digitizer is made by the local position of the card on the P2 connector. The addresses in the registers given below are for the first of two **AD-48S** cards. The second **AD-48S** card has an address based on an offset of $20. **Table 15** illustrates the different register addressing for both **AD-48S** cards.

AD-48S card	register name	address
first card	CH200K_1	$FFF00202
first card	CH200K_2	$FFF00206
first card	CHK200K_3	$FFF0020A
first card	CH200K_4	$FFF0020E
first card	ADSTAT	$FFF00212
second card	CH200K_1	$FFF00222
second card	CH200K_2	$FFF00226
second card	CHK200K_3	$FFF0022A
second card	CH200K_4	$FFF0022E
second card	ADSTAT	$FFF00232

Table 15. **AD-48S** Register Addressing.

10.9.1 CH200K_1 REGISTER

The register is maintained in a RESET state unless the bit # 6 TIM200K in the CTRL_1 register is set to a "1". Each bit active the corresponding relay of the channel selected for a 200KSPS mode.

ADR/SIZ	$FFF00202 (LD15:08)							
BIT	7	6	5	4	3	2	1	0

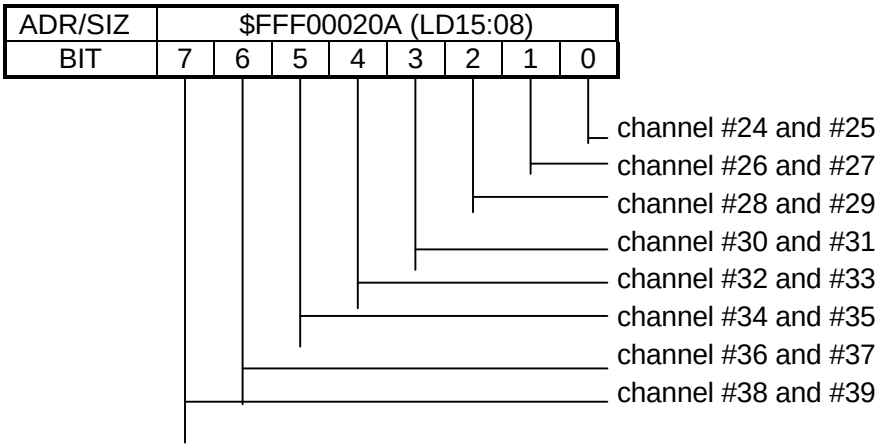
- channel #0 and #1
- channel #2 and #3
- channel #4 and #5
- channel #6 and #7
- channel #8 and #9
- channel #10 and #11
- channel #12 and #13
- channel #14 and #15

10.9.2 CH200K_2 REGISTER

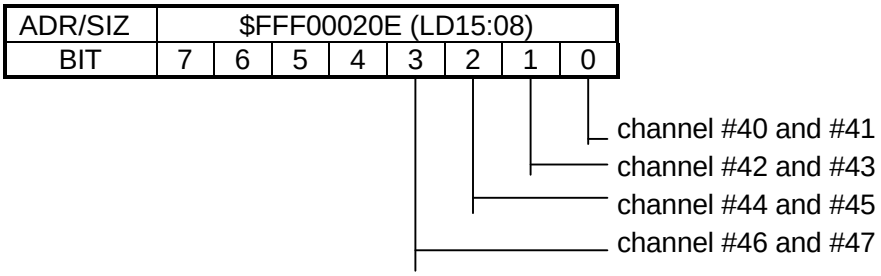
ADR/SIZ	$FFF00206 (LD15:08)							
BIT	7	6	5	4	3	2	1	0

- channel #16 and #17
- channel #18 and #19
- channel #20 and #21
- channel #22 and #23
- channel #24 and #25
- channel #26 and #27
- channel #28 and #29
- channel #30 and #31

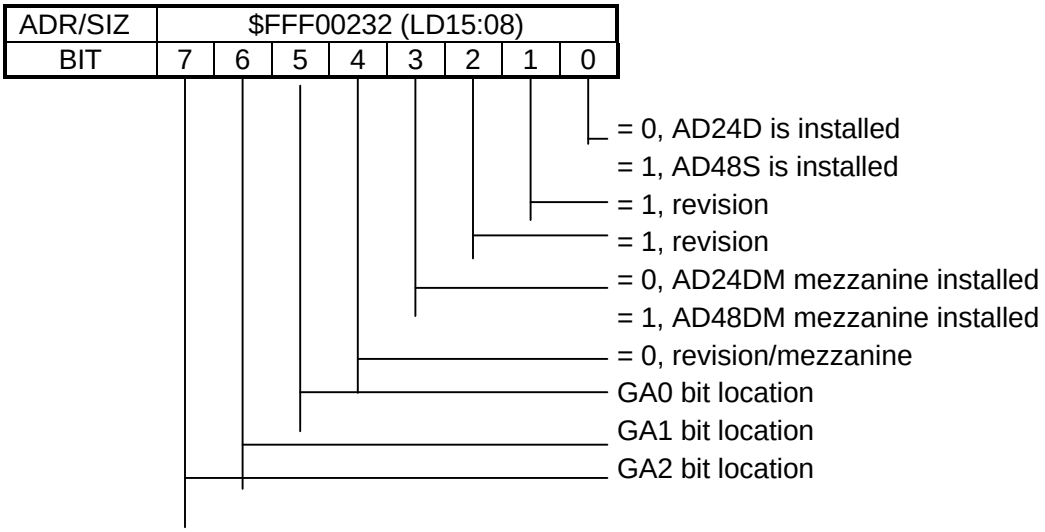
10.9.3 CH200K_3 REGISTER



10.9.4 CH200K_4 REGISTER



10.9.5 ADSTAT REGISTER



10.10 AD-24D REGISTERS

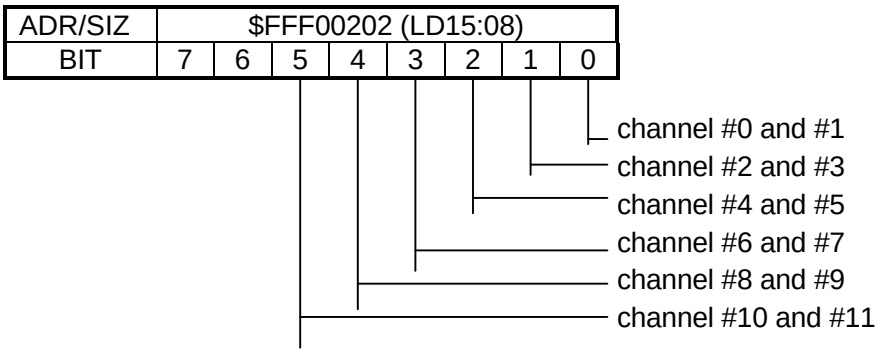
Each **AD-24D** card has the following registers activated by the signal CSADREG*. Selection between the **AD-24D** card belonging to one digitizer is made by the local position of the module on the P2 connector. The addresses in the registers given below are for the first of two **AD-24D** cards. The second **AD-24D** card has an address based on an offset of $20. **Table 16** illustrates the different register addressing for both **AD-24D** cards.

AD-48S card	register name	address
first card	CH200K_1	$FFF00202
first card	CHK200K_3	$FFF0020A
first card	ADSTAT	$FFF00212
second card	CH200K_1	$FFF00222
second card	CHK200K_3	$FFF0022A
second card	ADSTAT	$FFF00232

Table 16. **AD-24D** Register Addressing.

10.10.1 CH200K_1 REGISTER

The register is maintained in a RESET state unless the bit # 6 TIM200K in the CTRL_1 register is set to a "1". Each bit active the corresponding relay of the channel selected for a 200KSPS mode.



10.10.2 CH200K_3 REGISTER

ADR/SIZ	$FFF0020A (LD15:08)							
BIT	7	6	5	4	3	2	1	0

- bit 0: channel #12 and #13
- bit 1: channel #14 and #15
- bit 2: channel #16 and #17
- bit 3: channel #18 and #19
- bit 4: channel #20 and #21
- bit 5: channel #22 and #23

10.10.3 ADSTAT REGISTER

ADR/SIZ	$FFF00212 (LD15:08)							
BIT	7	6	5	4	3	2	1	0

- bit 0: = 0, AD24D is installed; = 1, AD48S is installed
- bit 1: = 1, revision
- bit 2: = 1, revision
- bit 3: = 0, AD24DM mezzanine installed; = 1, AD48DM mezzanine installed
- bit 4: = 0, revision/mezzanine
- bit 5: GA0 bit location
- bit 6: GA1 bit location
- bit 7: GA2 bit location