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IP-THERMISTOR

6 CHANNELS TEMPERATURE
8-CHANNEL VOLTAGE
Industry Pack module

HARDWARE REFERENCE MANUAL

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1 GENERAL DESCRIPTION

1.1 INTRODUCTION

The **IP-THERMISTOR** is a 24/16 bit precision temperature measurement single width IP module with fixed and optional programmable current source. Also a 16 bit A/D converter with 8 channels multiplexed allows measurement of input voltage in excess of +/- 20volts.

- Each analog input is software programmable separately from +/-10v, +/-5v, 0 -5v, 0-10v.
- A high precision voltage divider permit input voltage up to +/-20v.
- Sampling clock of 100 ksamples/second.
- Each temperature measurement channel has it own delta sigma A/D converter programmable for 16 or 24 bit precisions.
- Also the input has a software programmable gain from 1 to 128.
- Low pass filter with programmable filter cutoff are part of the package.
- Each delta sigma converter also provides two matched current source generator for rtd or thermistor.
- An additional two programmable current source is providing for high value thermistor that will exceed the range of the input amplifier.
- Last reading value is always available.
- Calibration can be manual or automatic.
- An EPROM allows data storage.
- IP bus operates at 8 or 32 MHz.

A data flow block diagram of the **IP-THERMISTOR** is presented in Figure 1-1.

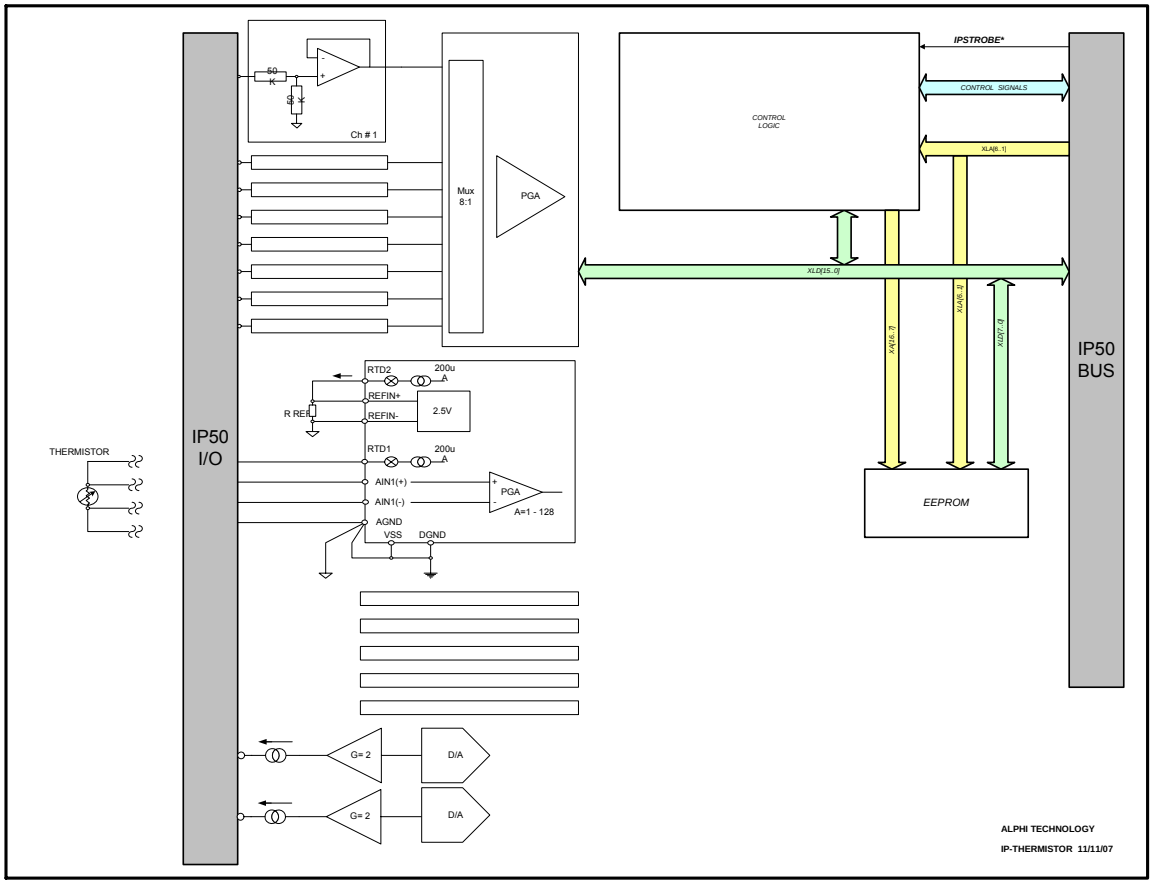


Figure 1.1: Data Flow Block Diagram

1.2 FUNCTIONAL DESCRIPTION

The IP-THERMISTOR has three main input/output blocks.

1.2.1 TEMPERATURE MEASUREMENT

The IP-THERMISTOR is designed around the delta sigma A/D converter AD7711 from Analog Devices.

The IP-THERMISTOR uses six Analog Digital AD7711 Signal Conditioning ADCs.

Each of the 6 temperature measurement channels has its own A/D converter with two matched 200 µA current sources.

To avoid error due to fluctuation of the current source the A/D reference voltage is externally provided by a precision resistor that will develop the 2.5V reference voltage using one of the current sources.

The AD7711 communicate through a serial interface. Transfer of the data or control word is slow. To avoid waiting for the end of an access different methods can be used, including an end of transfer interrupt.

At the end of each acquisition the conversion results are stored into holding registers. These holding registers are normally updated every 1.5 ms.

1.2.2 DELTA-SIGMA A/D CONVERTER WITH EXCITATION CURRENT

The IP_THERMISTOR provide temperature measurement by using thermistor or RTD sensors.

Different configurations are possible by using some jumper's settings.

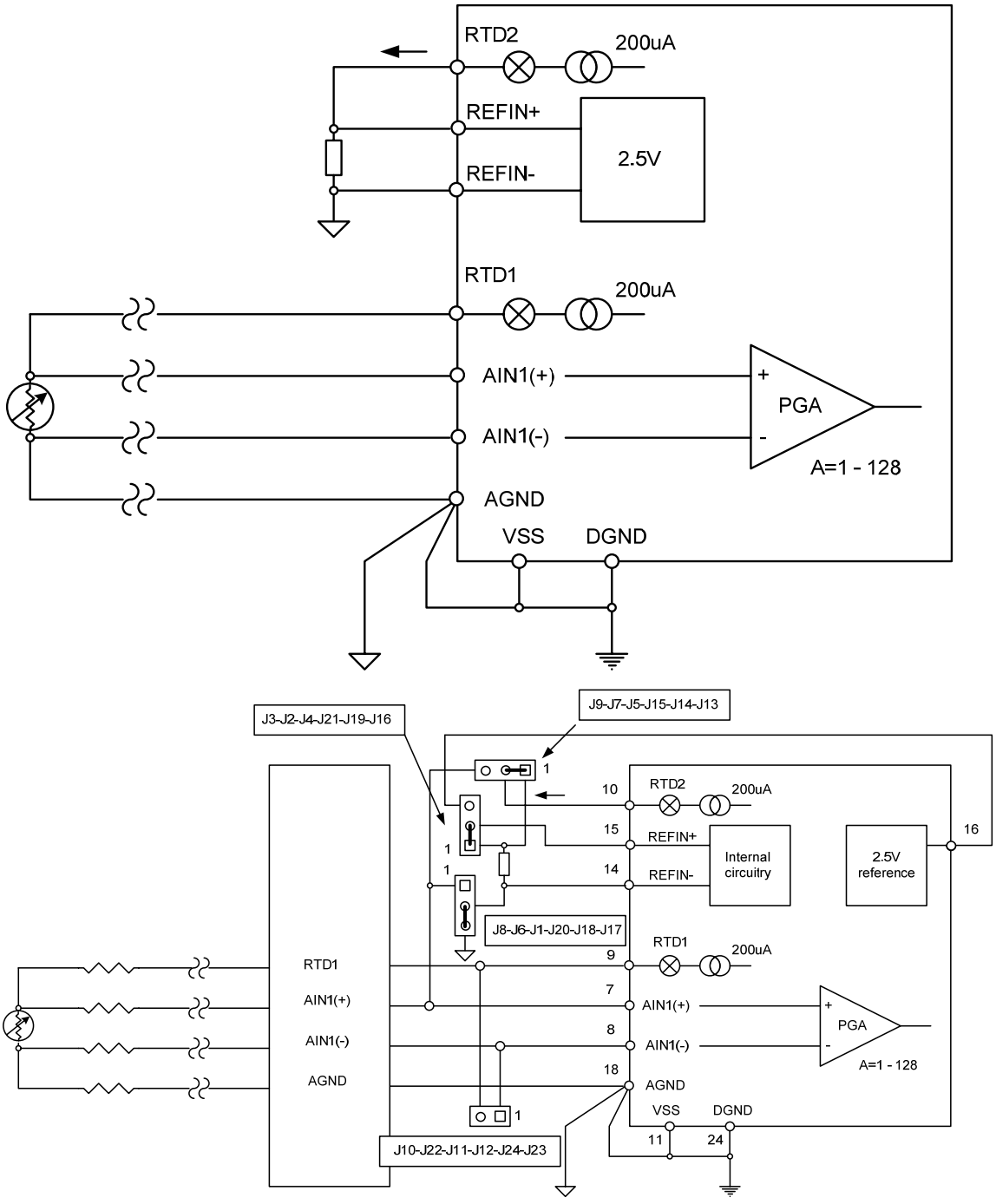
1.2.2.1 4-Wire configuration

Error temperature drift is reduced by using one of the current sources to generate the reference.

The current flows through a precision resistor developing an external reference of 2.5V. Temperature drift error is then compensated because two current sources are matched to less then 3 ppm / ˚ C.

The other precision current source flows through the temperature sensor. The voltage generated is measured with an A/D converter that can be programmed for a precision of either 16 or 24 bits.

A programmable analog front end amplifier adjusts the input signal to get the best resolution possible. Gain from 1 to 128 can be achieved. The AD7711 has a 2.5v internal reference. It has also two matched current source of 200 µA.



4 – Wire application

SIGNAL CHANNEL #1	PIN	SIGNAL CHANNEL #2	PIN	SIGNAL CHANNEL #3	PIN
IN_THERM. +	23	IN_THERM. +	18	IN_THERM. +	48
IN_THERM. -	24	IN_THERM. -	19	IN_THERM. -	49
CURRENT +	22	CURRENT +	17	CURRENT +	47

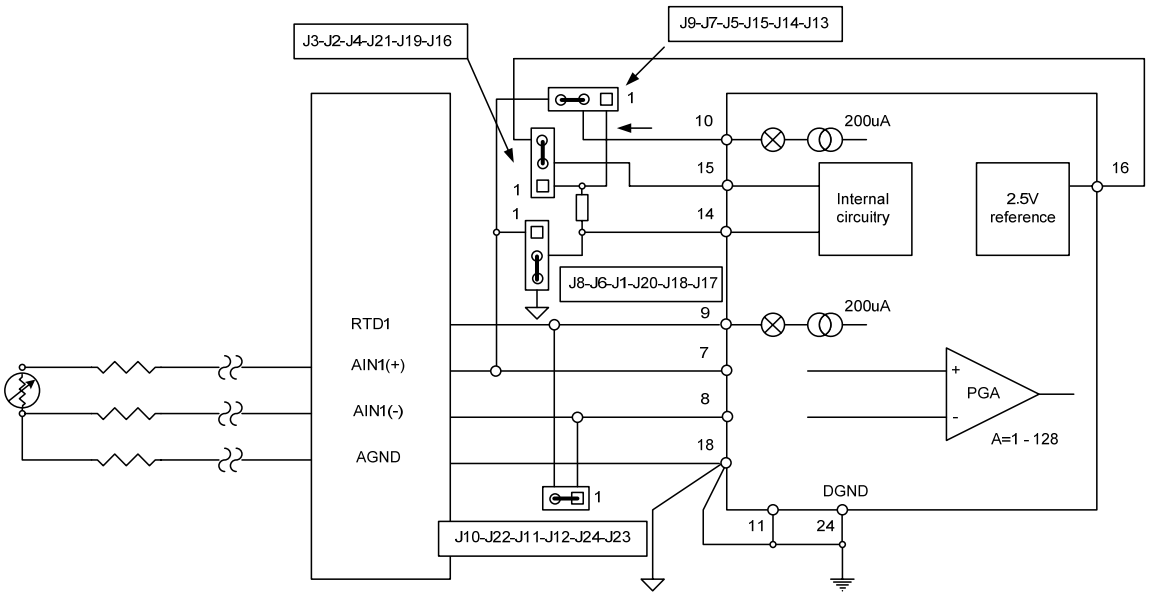
AGND (-)	25	AGND (-)	20	AGND (-)	50

SIGNAL CHANNEL #4	PIN	SIGNAL CHANNEL #5	PIN	SIGNAL CHANNEL #6	PIN
IN_THERM. +	43	IN_THERM. +	13	IN_THERM. +	38
IN_THERM. -	44	IN_THERM. -	14	IN_THERM. -	39
CURRENT +	42	CURRENT +	12	CURRENT +	37
AGND (-)	45	AGND (-)	15	AGND (-)	40

1.2.2.2 3-Wire configuration with internal reference

The internal reference is used.

The two current sources are used to compensate for the loss into the resistance wiring.

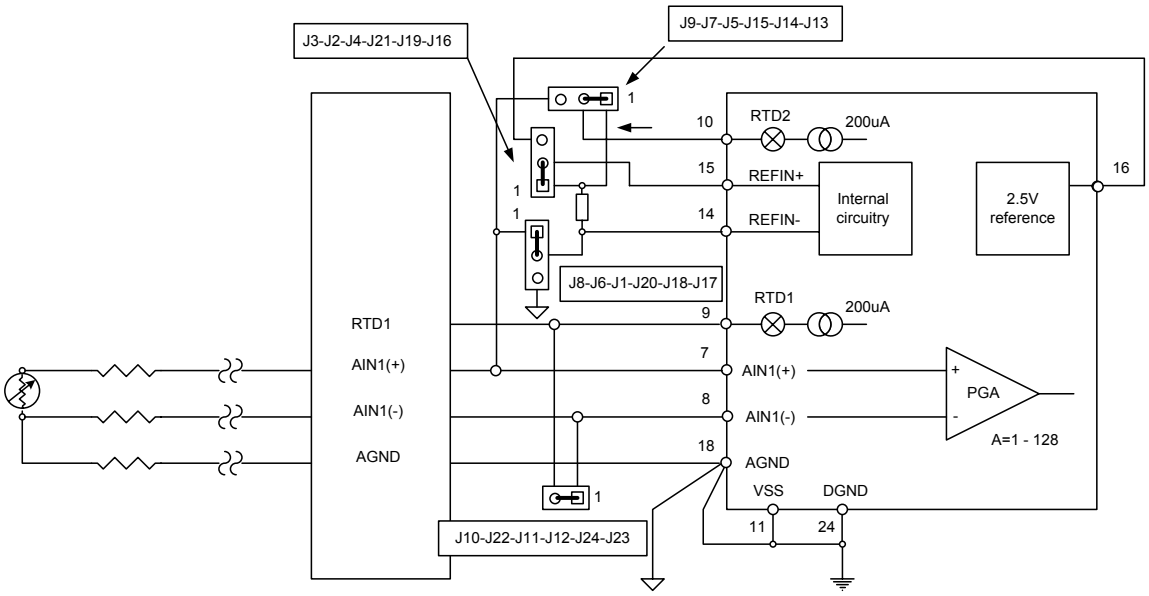


3 – Wire application with internal reference

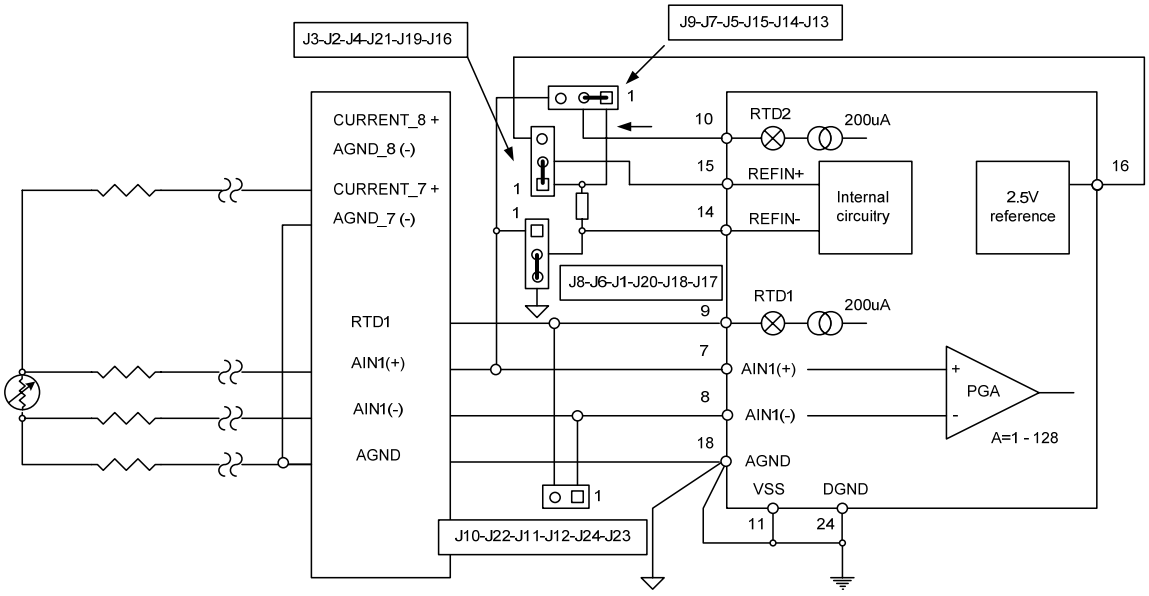
1.2.2.3 3-Wire configuration with external reference

The voltage reference is generated by using one of the current sources flowing through a precision resistance to generate the 2.5V.

Temperature drift error is reduced.



3 – Wire application with externally generated reference



4 – Wire application with programmable current source

PROGRAMMABLE CURRENT SOURCE # 7	PIN	PROGRAMMABLE CURRENT SOURCE # 8	PIN
CURRENT +	10	CURRENT +	35
AGND (-)	11	AGND (-)	36

1.2.3

1.2.4 HIGH VOLTAGE MEASUREMENT

The board features 8 single ended high-impedance analog inputs. The voltage is divided by 2 before reaching the A/D converter.

A 100ksps A/D converter, operating continuously, reads 8 command words and stores each acquisition result into the corresponding one of the 8 result registers.

Each input can be programmed for ±20V (seen from the input connector), ±10v, 0-20V or 0-10V. The divider by two allows the high input voltages.

Each input has a configuration register that is sent to the A/D converter while the result of the precedent conversion transferred to its holding register.

1.2.5 PROGRAMMABLE CURRENT GENERATOR

- Two programmable current sources if needed by the thermistor. Each current source uses a 16-bit D/A to set its output level.

2 INTERFACE TO THE IP CARRIER

2.1 IDSPACE

Up to 32 bytes of registered data provide information about the module. Although 16-bit access is used, only the lower byte contains the data. As provided in the IP-module specification, it contains manufacturer data, the type of module, revision, etc...

ID space address	Description	Value
$00	ASCII “I”	$49
$02	ASCII “P”	$50
$04	ASCII “A”	$41
$06	ASCII “H”	$48
$08	Manufacturer identification	$11
$0A	Module type	$32
$0C	Revision module	$0A
$0E	Reserved	$00
$10	Driver ID, low byte	$00
$12	Driver ID, high byte	$00
$14	Number of bytes used	$0A
$16	CRC	$00
$18-$3E	User space	$00

Table 2-1 IDSEL0 SPACE byte content

2.2 INTSPACE

During an interrupt acknowledge, the interrupt vector is sent to the processor.

2.3 IOSPACE

The Host IP carrier controls the module AD-thermistor using a set of registers located within the IOSPACE.

The accesses are 16-bit. All registers are located at EVEN addresses. Some registers use only the lower byte.

IP-THERMISTOR Address	Read/ Write	Access	Register
0x00	R/W	16-bit	Internal Clock Divisor 0
0x02	R/W	16-bit	Internal Clock Divisor 1
0x04	R/W	16-bit	D/A programmable current # 1

0x06	R/W	16-bit	D/A programmable current # 2
0x08	W		Synchronous load
0x0A	R/W	8-bit	Interrupt Vector Register
0x0C	W		Host start conversion
			LTC1859
0x10	R/W	8-bit	Configuration input channel # 1
0x12	R/W	8-bit	Configuration input channel # 2
0x14	R/W	8-bit	Configuration input channel # 3
0x16	R/W	8-bit	Configuration input channel # 4
0x18	R/W	8-bit	Configuration input channel # 5
0x1A	R/W	8-bit	Configuration input channel # 6
0x1C	R/W	8-bit	Configuration input channel # 7
0x1E	R/W	8-bit	Configuration input channel # 8
0x20	R	16-bit	A/D data result channel # 1
0x22	R	16-bit	A/D data result channel # 2
0x24	R	16-bit	A/D data result channel # 3
0x26	R	16-bit	A/D data result channel # 4
0x28	R	16-bit	A/D data result channel # 5
0x2A	R	16-bit	A/D data result channel # 6
0x2C	R	16-bit	A/D data result channel # 7
0x2E	R	16-bit	A/D data result channel # 8
			AD7711
0x40	R/W	Upper 8-bit	Holding Register # 1 [23..16]
0x42	R/W	16-bit	Holding Register # 1 [15..0]
0x44	R	Upper 8-bit	Data Register # 1 [23..16]
0x46	R	16-bit	Data Register # 1 [15..0]
0x48	R/W	Upper 8-bit	Holding Register # 2 [23..16]
0x4A	R/W	16-bit	Holding Register # 2 [15..0]
0x4C	R	Upper 8-bit	Data Register # 2 [23..16]
0x4E	R	16-bit	Data Register # 2 [15..0]
0x50	R/W	Upper 8-bit	Holding Register # 3 [23..16]

0x52	R/W	16-bit	Holding Register # 3 [15..0]
0x54	R	Upper 8-bit	Data Register # 3 [23..16]
0x56	R	16-bit	Data Register # 3 [15..0]
0x58	R/W	Upper 8-bit	Holding Register # 4 [23..16]
0x5A	R/W	16-bit	Holding Register # 4 [15..0]
0x5C	R	Upper 8-bit	Data Register # 4 [23..16]
0x5E	R	16-bit	Data Register # 4 [15..0]
0x60	R/W	Upper 8-bit	Holding Register # 5 [23..16]
0x62	R/W	16-bit	Holding Register # 5 [15..0]
0x64	R	Upper 8-bit	Data Register # 5 [23..16]
0x66	R	16-bit	Data Register # 5 [15..0]
0x68	R/W	Upper 8-bit	Holding Register # 6 [23..16]
0x6A	R/W	16-bit	Holding Register # 6 [15..0]
0x6C	R	Upper 8-bit	Data Register # 6 [23..16]
0x6E	R	16-bit	Data Register # 6 [15..0]
0X70	W	x	Reset AD7711 registers
0X70	R	16-bit	AD7711 Bit Counter #1,#2
0X72	R	16-bit	AD7711 Bit Counter #3,#4
0X74	R	16-bit	AD7711 Bit Counter #5,#6
0X76	R	8-bit	Transfer Status
0X78	W	8-bit	CONTROL register #0
0X7A	W	x	AD7711 Synchronization
0X7C	W	16-bit	Interrupt Status
0X7E	R/W	16-bit	Interrupt Mask

Table 2.1: IO Registers

2.3.1 INTERNAL SCAN CLOCK DIVISOR

The Scan clock is used by the A/D converter LTC1859.

Base I/O + 0x$00-0x$02

These two 16-bit registers combine to form one 24 bit register which serves as a divisor on the IP clock when internal sampling clock is selected.

$$SamplingRa\ te = \frac{IPClockFre\ q}{N+1}$$

EXAMPLE

At 8 MHz set the Internal Clock for 130µS do the following.

$00 - Internal clock, write $400 (any data within the appropriate range)

$02 - Internal clock, write $0

Each acquisition take 7uS * 8 = 56 µS. Minimum clock should be around 70/75 µS ($0 = 260)

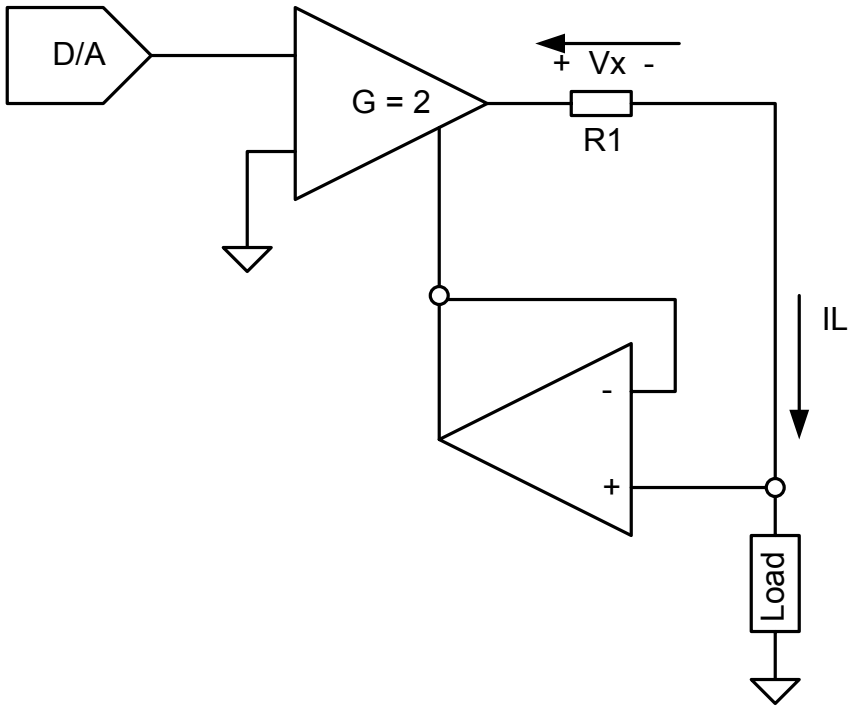
2.3.2 PROGRAMMABLE CURRENT SOURCE

Base I/O + 0x04-0x06

Two optional current sources are available. These voltage controlled current source use improved version of the Howland current pump. There is one D/A converter for each of the 2 current sources. The converters have 16-bit definition, with internal reference, 0 to 4.096 V output that is fed into a differential amplifier with a gain of 2.

A LTC1167 for each channel converts the incoming voltage to a current. They provide a usable current ranging from 100 nA to 50 µA, or 10 nA to 8 µA depending on the two jumper-selectable sets of resistances.

Jumper	Current source	Shunt between 1-2 R1 =1Mohm	Shunt between 2-3 R1 =100Kohm
J28	# 7	10 nA to 8 µA	100nA to 50µA
J27	# 8	10 nA to 8 µA	100nA to 50µA



To program a current first we need to select R1 as a function of chosen range.

If using the 100 KΩ resistor, the value to write in current source register is ***(current/10) * 8000***;

if using the 1 MΩ resistor, the value to write is ***current * 8000***

The current is expressed in µA. The register will accept a value between 0 and 65535.

With R_1 = 1 MΩ , $I_{L\ max}$ = 8µA.

With R_1 = 100KΩ, $I_{L\ max}$ = 80µA.

The total voltage, **(R_1 + Load) * current** should not exceed +10v.

When using the programmable current source, the AD7711 need to use the internal reference of the chip, removing some auto-correction error provided then by the two internal current source of 200µA.

Power-on reset is zero volts.

2.3.3 HIGH VOLTAGE ANALOG INPUTS

Measuring input voltage above the standard voltage supply of +/- 12V requires either:

A high voltage input amplifier with the support of a DC/DC converter providing at least +/- 18V min for +/- 15V input signal. Then the signal acquired is divided by a set of precision resistance.

Or a precision input voltage divider with capabilities power dissipation capabilities and the use of a buffer amplifier protected for reverse output change if input is exceeding the input voltage allows.

The IP-thermistor uses the second method due to the small real- estate available.

Input impedance is kept high by using a 50Kohms resistance.

The A/D converter features an 8-channel multiplexed input with possibilities to program each input with a different voltage range, in single or differential mode.

The default mode is single input with an input range of +/- 10V. Since we divide by 2 the voltage with the voltage divider, this means a real input range of +/- 20 Volts.

A programmable scan clock will provide new data every 75 µS Min.

Single acquisition can be made by a Host write command at address I/O + $0C.

Start acquisition using the Scan clock is enabling by setting Bit # 2 of the CTRL0 register to a "1".

A state machine allows scheduling 8 acquisitions, each with its own configuration word. Each configuration is 8-bit, defined as below. This configuration data is sent directly to the LTC1859. Please refer to the LTC1859 data sheet for a more complete explanation.

Upon a conversion start the configuration of the next channel to be converted is send to the A/D converter while the data result from the precedent conversion is output from the A/D converter to the appropriate data register.

2.3.3.1 Configuration registers LTC1859

I/O + $10-$12-$14-$16-$18-$1A-$1C-$1E

BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 00
Single/Diff	Odd sign	Sel1	Sel0	Uni	Gain	Nap	Sleep

Only the lower byte is used. They can be read back.

2.3.3.2 Example for 8 channels single ended and Gain of "1".

- Program the Internal Clock for 130µS do the following.

  $00 - Internal clock, write $400 (any data within the appropriate range)

  $02 - Internal clock, write $0

-Program the configuration of each channel

CH # 0 I/O + $10 = $84

CH # 1 I/O + $12 = $C4

CH # 2 I/O + $14 = $94

CH # 3 I/O + $16 = $D4

CH # 4 I/O + $10 = $A4

CH # 5 I/O + $12 = $E4

CH # 6 I/O + $14 = $B4

CH # 7 I/O + $16 = $F4

Start the conversion setting bit #2 of the CTRL0 register to "1".

Note: The CTRL0 register have also other bits used for other purpose.

The result of the conversions is stored from the address I/O + 0x20 for channel # 0 to I/O + 0x2E for channel #7.

Channel # 6 and channel # 7 can be use to monitor the output of the two D/A controlling the two current sources.

Jumpers J25 and J26 must be set accordingly.

Jumper	1-2	2-3
J25	Analog input # 6	Output D/A # 1
J26	Analog input # 7	Output D/A # 2

BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 00
Bit # 7	Bit # 6	Bit # 5	Bit # 4	Bit # 3	Bit # 2	Bit # 1	Bit # 0(LSB)

BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 09	BIT 08
Bit # 15(MSB)	Bit # 14	Bit # 13	Bit # 12	Bit # 11	Bit # 10	Bit # 9	Bit # 8

2.3.4 THERMISTOR INPUTS WITH SIGNAL CONDITIONING ADC AD7711

The AD7711 has a master clock derived from the IP clock of 8 MHz.

Communication with the AD7711 is by a serial port of 24 bits. The serial clock is 1/512 the frequency of the Master clock or 15625 Hz.

2.3.4.1 AD7711 Holding registers

I/O + 0x40-43, I/O + 0x48-4B, I/O + 0x5-53, I/O + 0x58-5B, I/O + 0x60-63, I/O + 0x68-6B

Read/write to the HOLDING register.

Each AD7711 use two words for each access.

When writing into the configuration or calibration registers, the first lower word is stored into a holding register then the second word, also store into an holding register, will initiate a serial transfer to the AD7711 at end of the second write access.

BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT160
MD2	MD1	MD0	G2	G1	G0	CH	PD

BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 09	BIT 08
WL	IO	BO	B/U	FS 11	FS 10	FS 9	FS 8

BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 00
FS 7	FS 6	FS 5	FS 4	FS 3	FS 2	FS 1	FS 0 (LSB)

Example access to control registers AD7711 # 1

Set A0 to “0”: I/O +$78 Bit # 0 = 0 and “Acquire data signal” Bit # 6 =0

Write Holding register I/O +$40 “D7A1” or “D0A1”

-7A1 DIGITAL FILTER

Note: Decimal digital filter value need to be more than 19 and less than 2000

-D 24 BIT, Excitation current “ON” ,Burn-out current “OFF” , Unipolar mode

-A0 Active background calibration, gain = “1”, channel # 0, Power active

Write Holding register I/O +$42 “00A0”

Read-back provide the output value of the HOLDING Registers only.

To read the content of the AD7711 internal control register, initiate a Read command by writing (any value) at location I/O +$44.

Wait a least 15 us or poll status of the counter or program an interrupt on read for this channel, then read at location I/O +$44, I/O +$46.

The pin A0 of the AD7711 must be set before to a “0” for control register access or to “1” for data/calibration registers.

To have continuous acquisition with result at address I/O +$44, I/O +$46 set operating mode MD[2..0] to [1.0.1] then pin A0 to “1” .

Pin A0 is controlled by the bit #0 of the control registerCTRL0 located at location I/O + $78

Then set (two steps) “Acquire data signal” to “1” into the CTRL0 register I/O + $78

Acquire signal is controlled by Bit # 6 of the control register.

2.3.4.2 AD7711 Data registers / Calibration registers

I/O + 0x44, I/O + 0x4c, I/O + 0x54, I/O + 0x5c, I/O + 0x64, I/O + 0x6c

These registers contain the results of a read request made to the internal registers of the AD7711.

Results can be configuration registers (A0 = “0”) or Data registers or Calibration registers (A0 = “1”)

Pin A0 = “1” is set by the bit # 0 of the control registerCTRL0 located at location I/O + $78

To write to the calibration registers we also use the Holding registers .

Read of an internal register, is made when a write command at address I/O +$44 (for AD7711 # 1) is generated.

Result is available then at address I/O +$44, I/O +$46.

A delay is needed between a write command and read of the result (15 µS to 20µS).

Difference between calibration register read or data read is made by programming of the Operation registers into the control registers MD[2..0].

It is important to monitor the status of a write command or a read command.

When in a continuous acquisition mode the data are stored into output register to allow access to the latest result, generally updated every 1.5 ms depending of the filter programmation.

2.3.4.3 BIT COUNTER AD7711

When transferring data to or from the AD7711, the data is sent as a low speed stream of 24 bits. Acquisition time is filter dependent and can take from 900 uS to more than 750 mS.

Example : Control register value :

- $A0D7A1 750 mS
- $A0D0A1 61 mS
- $A0D041 2.5 mS

Multiple possibilities are offered to check the transfer completion:

-Polling the Transfer Status Register at address I/O + 0x76. Because of the long duration of the transfer, this can be unpractical.

-Read the counter transfer status and use the number of bit left transfer to calculate a delay, since we know that we need about 60 µs per bit.

- Use the interrupts that can be generated at the end of a read or write cycle (Interrupt Enable Register at I/O + 0x70)

When in automatic acquisition the last data can be read at address I/O + $44, I/O + $46, etc…

The 24 bits are left aligned to give the possibilities to read only one location if 16 bits are sufficient.

The upper 16 bits will appears at address I/O + $46, etc…

Arbitration is provide to avoid a host read of data while a new update is in progress.

2.3.4.3.1 Bit Counter AD7711 #1, AD7711 #2

Position of the serial bit counter of each AD7711 is provided for host use.

BIT 7	BIT 6	BIT 5	BIT 04	BIT 03	BIT 02	BIT 01	BIT 00
			CNT#1_4	CNT#1_3	CNT#1_2	CNT#1_1	CNT#1_0

BIT15	BIT14	BIT13	BIT 12	BIT 11	BIT 10	BIT 09	BIT 08
			CNT#2_4	CNT#2_3	CNT#2_2	CNT#2_1	CNT#2_0

2.3.4.3.2 Bit Counter AD7711 #3, AD7711 #4

I/O + 0x72

Position of the serial bit counter of each AD7711 is provided for host use.

BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 00
			CNT#3_4	CNT#3_3	CNT#3_2	CNT#3_1	CNT#3_0

BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 09	BIT 08
			CNT#4_4	CNT#4_3	CNT#4_2	CNT#4_1	CNT#4_0

2.3.4.3.3 Bit Counter AD7711 #5, AD7711 #6

I/O + 0x74

Position of the serial bit counter of each AD7711 is provided for host use.

BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 00
			CNT#5_4	CNT#5_3	CNT#5_2	CNT#5_1	CNT#5_0

BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 09	BIT 08
			CNT#6_4	CNT#6_3	CNT#6_2	CNT#6_1	CNT#6_0

2.3.5 TRANSFER STATUS REGISTER

I/O + 0x76

The signal TFSx is “0” while a write transfer is taking place in the corresponding AD7711. The signal RFS is “0” during read data transfer.

BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 00
		TFS6	TFS5	TFS4	TFS3	TFS2	TFS1

BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 09	BIT 08
		RFS6	RFS5	RFS4	RFS3	RFS2	RFS1

2.3.6 CONTROL REGISTER #0

I/O + 0x78

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
IP_32MHZ_EN	ACQUIRE DATA AD7711		EN_IRQ0	CAL_REG	START CONVERSION ENABLE	HOST START PULSE ENABLE	A0 AD7711

IP_32MHZ_EN

When the bit #0 is set to “1”, the module runs at 32 MHz. Upon reset the value is “0”, to work with an IP clock of 8 MHz. Rev a run only at 8 Mhz.

ACQUIRE DATA AD7711

When set to “1” with bit # 0 also set to “1” the AD7711 will acquire data continuously and store the result into the DATA storage registers I/O + $44, I/O + $46, etc…

Result can be read any time.

EN_IRQ0

Need to be set to “1” to have INTREQ#0 active.

CAL_REG

If instead of acquiring the data in continuous mode, when this bit is set to “1”, the AD7711 will provide the calibration registers values. The AD7711 control register need to be programmed accordingly.

START CONVERSION ENABLE

When this bit is set to “1’’ continuous conversion of the voltage A/D converter is made using the internal clock as sample clock.

For example :

Program clock :

I/O + $00 = $0400

I/O + $02 = $0000

I/O + $78 > $04

HOST START PULSE ENABLE

When set to “1”, a write by the Host at the location I/O + $0C will start an acquisition to the 8 voltage analog channels .

START CONVERSION ENABLE SHOULD ALSO BE SET TO “1”.

A0 AD7711

A0_AD7711 = “0”. Access to the internal control register of the AD7711.

A0_AD7711 = “1”. Access to the Calibration registers or the data registers.

For a continuous acquisition by the AD7711 the signal “A0” must be high.

2.3.7 SYNCHRONIZATION PULSE

I/O + 0x7a

Writing to this address sends a temporary low signal to the /SYNC input of all the AD7711s. It resets the nodes of the digital filter. It allows the synchronization of the digital filters.

2.3.8 INTERRUPT STATUS REGISTER

I/O + 0x7c

A “0” in any of these locations, means that an interrupt request was generated. When an interrupt is pending, a write to this location with the correspondent bit set to “1” will reset the interrupt.

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT0
		TFS6	TFS5	TFS4	TFS3	TFS2	TFS1

BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
		RFS6	RFS5	RFS4	RFS3	RFS2	RFS1

2.3.9 INTERRUPT MASK

I/O + 0x7e

When set to “1” each bit will enable the corresponding line TFS or RFS to generate an interrupt at end of cycle

BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 00
		TFS6	TFS5	TFS4	TFS3	TFS2	TFS1

BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 09	BIT 08
		RFS6	RFS5	RFS4	RFS3	RFS2	RFS1

2.3.10 INTERRUPT VECTOR REGISTER

I/O + 0x0a

This location contains the value of the eight-bit interrupt vector sent during the interrupt acknowledge cycle.

BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 00
IVR7	IVR6	IVR5	IVR4	IVR3	IVR2	IVR1	IVR0

3 HARDWARE DETAILS

3.1 JUMPERS

The jumpers placement is depicted below.

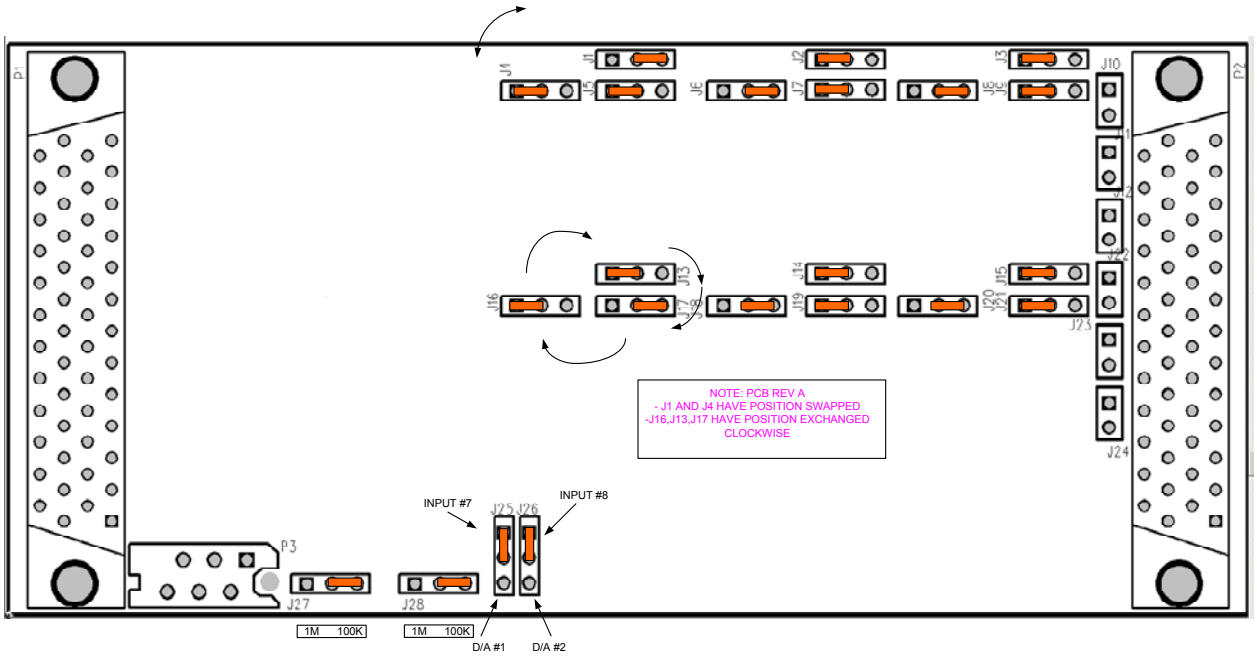


Figure 3.1: Jumpers Locations

3.1.1 CONNECTOR DESCRIPTIONS

3.1.2 IP EXTERNAL I/O CONNECTOR: P2

The signals are routed as follows.

Pin	Connection	Pin	Connection
1	IN_1	26	AGND
2	IN_2	27	AGND
3	IN_3	28	AGND
4	IN_4	29	AGND
5	IN_5	30	AGND
6	IN_6	31	AGND
7	IN_7	32	AGND
8	IN_8	33	AGND
9		34	
10	CURRENT_7A	35	CURRENT_8A
11	AGND_7A	36	AGND_8A
12	CURRENT_5A	37	CURRENT_6A
13	IN_THERM_5A+	38	IN_THERM_6A+
14	IN_THERM_5A-	39	IN_THERM_6A-
15	AGND_5A	40	AGND_6A
16		41	
17	CURRENT_2A	42	CURRENT_4A
18	IN_THERM_2A+	43	IN_THERM_4A+
19	IN_THERM_2A-	44	IN_THERM_4A-
20	AGND_2A	45	AGND_4A
21		46	
22	CURRENT_1A	47	CURRENT_3A
23	IN_THERM_1A+	48	IN_THERM_3A+
24	IN_THERM_1A-	49	IN_THERM_3A-
25	AGND_1A	50	AGND_3A

Table 4.1: IP external I/O connector

