

**CPCI6713-4 IP**

**CPCI DSP Intelligent IP Carrier**

**HARDWARE REFERENCE MANUAL**

**Revision 2.0.0**  
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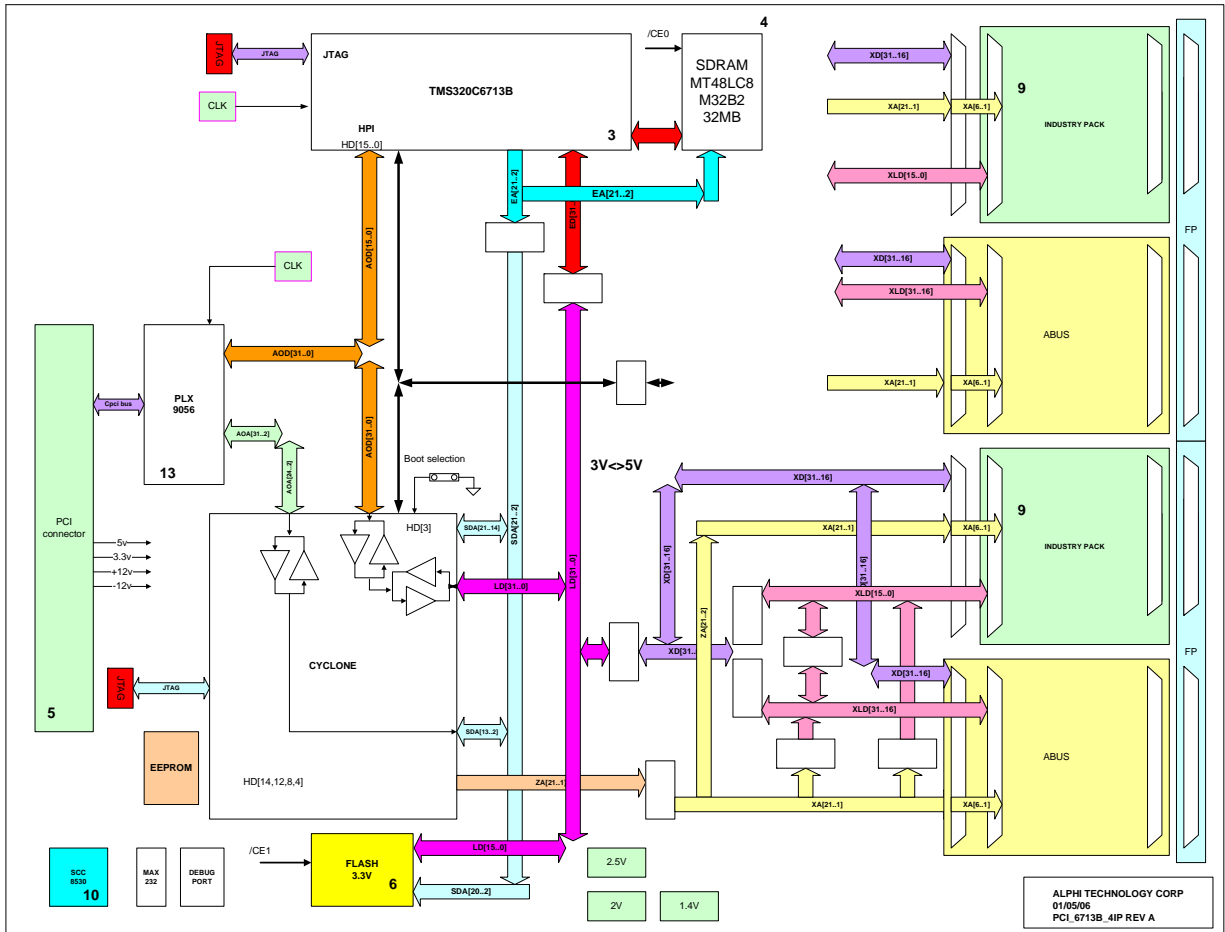
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# 1 BLOCK DIAGRAM



## 2 ARCHITECTURE

The main processor is a TMS320C6713B with a system clock up to 288MHZ.

Other board resources include:

- Up to 32Mbytes of SDRAM
- 512KB Flash memory for the bootstrap program
- RS232C controller
- Cyclone FPGA for decoding
- 4 IP slots to accommodate single / dual Industry Pack at 8 or 32 Mhz clock

### 2.1 THE 6713B BOOT PROCESS

The TMS320C6713/13B device has two boot modes: from the HPI or from external asynchronous FLASH EEPROM. On the TMS320C6713B, boot mode is determined during the device reset.

Refer to the TI application note spra512 for details on booting through the HPI.

When using the FLASH to boot, the first 1K of the FLASH are copied, starting to the local address 0x00000000 of the processor. After the end of the transfer, the CPU starts executing at the address 0. The small program thus loaded has the responsibility of doing at least a minimum configuration of 6713 registers and of copying a bigger program that will start executing and actually boot the board.

The board interface is configured as Big-Endian with the 8-bit data on the ED[31:24] side of the bus. HPI is always enabled

#### J 5

#### BOOT CONFIGURATION

No jumper

CE1 width 32-bit, HPI boot/Emulation boot

**jumper**

CE1 width 16-bit, Asynchronous external ROM boot with default timings

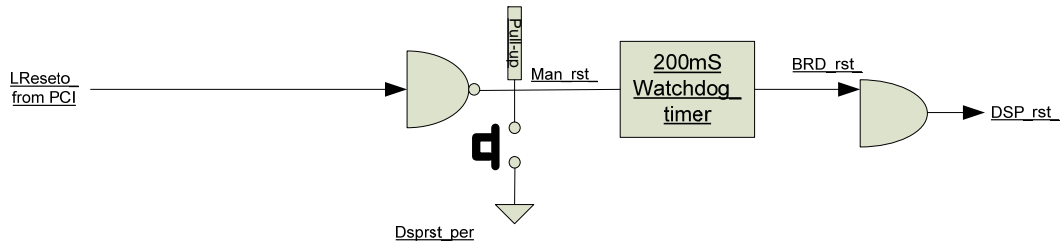
### 2.2 RESET SCHEME

The TMS6713B-4PACK board has multiple source of reset. Upon Power-on a watch-dog timer provide a 200ms minimum delay where the DSP is maintained on reset. This gives each programmable logic chip enough time to get its program loaded.

The board can be reset by:

- Power-on reset
- CPCI reset line /LRESET0 from PLX
- Push-button

All these methods use the watch-dog timer for delay.



### 3 6713 Local Peripherals

#### 3.1 6713 Internal registers

##### 3.1.1 EMIF programming

The board uses the 6713 EMIF module (External Memory Interface) to generate on-board timings.

Using the EMIF, the memory space is divided as:

MEMORY SPACE	SETTING	RESOURCE	SIZE	ADDRESS RANGE
CE0	0xffffbf33	SDRAM	8-32MB	0x80000000-0x81FFFFFF
CE1	0x12328620	ADD_ON + PERIPHERALS	4MB	0x90000000-0x903FFFFFF
CE2	0x12328610	IP MEMORY SPACE	4MB	0xA0000000-0xA31FFFFFF
CE3	0x12328610	FLASH (16-bit wide)	4MB	0xB0000000-0xB03FFFFFF

The default EMIF configuration in accordance with the PLL settings has been selected to give the maximum performance without sacrificing signal integrity. We recommend not changing it, as an incorrect setting will prevent the board from functioning properly.

Default EMIF configuration:

REGISTER	ADDRESS	SETTING
EMIF_GCTL	0x01800000	0x00000078
EMIF_CE0	0x01800008	0xffffbf33
EMIF_CE1	0x01800004	0x12328620
EMIF_CE2	0x01800010	0x12328610
EMIF_CE3	0x01800014	0x12328610
EMIF_SDRAMCTL	0x01800018	0x46216000
EMIF_SDRAMTIM	0x0180001C	0x00000618
EMIF_SDRAMEXT	0x01800020	0x00054529

### 3.1.2 PLL programming

The outside 48MHZ clock provided to the DSP is multiplied by the programmable internal PLL (x12) generating a 576 MHZ internal clock. This clock is then divided by two to provide SYSCLK or CLKOUT2 (288 MHZ).

The outside bus timings are generated by the TMS320C6713B EMIF using CLKOUT3 (the 576 MHZ clock divided by 6 by the PLL # 2) which is a 96 MHZ clock.

We strongly recommend using the default timings.

```
/*-----*/
/* C6713 PLL SUPPORT */
/*-----*/
#define PLL_BASE_ADDR      0x01b7c000
#define PLL_PID            ( PLL_BASE_ADDR + 0x000 )
#define PLL_CSR            ( PLL_BASE_ADDR + 0x100 )
#define PLL_MULT           ( PLL_BASE_ADDR + 0x110 )
#define PLL_DIV0           ( PLL_BASE_ADDR + 0x114 )
#define PLL_DIV1           ( PLL_BASE_ADDR + 0x118 )
#define PLL_DIV2           ( PLL_BASE_ADDR + 0x11C )
#define PLL_DIV3           ( PLL_BASE_ADDR + 0x120 )
#define PLL_OSCDIV1       ( PLL_BASE_ADDR + 0x124 )

#define CSR_PLEN           0x00000001
#define CSR_PLLPWRDN      0x00000002
#define CSR_PLLRST        0x00000008
#define CSR_PLLSTABLE     0x00000040
#define DIV_ENABLE        0x00008000

/*-----*/
/* init_pll() */
/* PLL Initialization */
/*-----*/
void init_pll()
{
    /*-----*/
    /* When PLEN is off DSP is running with CLKIN clock */
    /* source, currently 50MHz or 20ns clk rate. */
    /*-----*/
    *(int *)PLL_CSR &= ~CSR_PLEN;

    /* Reset the pll. PLL takes 125ns to reset. */
    *(int *)PLL_CSR |= CSR_PLLRST;

    /*-----*/
    /* PLLOUT = CLKIN/(DIV0+1) * PLLM */
    /* 450 = 50/1 * 9 */
    /*-----*/
    *(int *)PLL_DIV0 = DIV_ENABLE + 0;
    *(int *)PLL_MULT = 12;
    *(int *)PLL_OSCDIV1 = DIV_ENABLE + 4;

    /*-----*/
    /* Program in reverse order. */
    /* DSP requires that periheral clocks be less then */
    /* 1/2 the CPU clock at all times. */
    /*-----*/
    *(int *)PLL_DIV3 = DIV_ENABLE + 5; // 96 MHz EMIF
    *(int *)PLL_DIV2 = DIV_ENABLE + 3;
    *(int *)PLL_DIV1 = DIV_ENABLE + 1;
    *(int *)PLL_CSR &= ~CSR_PLLRST;

    /*-----*/
    /* Now enable pll path and we are off and running at */
    /* 300MHz with 100 MHz SDRAM. */
    /*-----*/
    *(int *)PLL_CSR |= CSR_PLEN;
}
```



### 3.2 CE0 space

The SDRAM is mapped in the CE0 space. Depending on your board options, up to 32 megabytes are available (4 megabytes is standard). The SDRAM is connected to the 6713B bus. The data and address buses are isolated to the local bus by buffers.

### 3.3 CE1 space

CE1 space is share between the boot flash, all peripherals including the ADD\_ON module.

PERIPHERALS	SIZE	ADDRESS RANGE
FLASH	2MB	0x90000000 - 0x901F FFFF
PLX_REG	1KB	0x902F E000 - 0x902F E3FF
SCC8530	1KB	0x902F E400 - 0x902F E7FF
CYCLONE REG	1KB	0x902F E800 - 0x902F EBFF

#### 3.3.1 FLASH EPROM

A 256Kx16 Flash memory [M29F400DB](#) is visible at the base address of CE1 (0x0x90000000) space for use during the boot process. It is also visible in CE3 (0xB0000000). The address space CE1 is 32-bit wide once the board has booted, so when accessing the FLASH, only the lower 16 bits of each 32-bit word contains actual data.

By contrast, the CE3 space is 16-bit wide, matching the FLASH actual geometry and the data is continuous.

#### 3.3.2 Locals Registers

The cyclone logic has a set of locals registers used to set-up some local parameters or to communicate with the PLX bus.

##### 3.3.2.1 DSP\_CNTL0\_ADR 0x902F E800

ED7	ED6	ED5	ED4	ED3	ED2	ED1	ED0
		XRESET	NMIEN	x	FLASH_PAGE	!/LED_O[1]	!/LED_O[0]

/LED\_O[1..0]: This register controls 2 LEDs. The reset position is for the LEDs to be "off". A "1" in the position corresponding to the LED will set it "on".

FLASH\_PAGE: Currently unused, should be 0.

NMIEN: TMS320C6713B allows receiving the NMI interrupt from multiple sources. The default is 0: "disabled".

XRESET: A "1" will put the extended bus in a reset mode until it is cleared. The default is "no reset".

##### 3.3.2.2 DSP\_STAT0\_ADR 0x902F E804

ED7	ED6	ED5	ED4	ED3	ED2	ED1	ED0
-----	-----	-----	-----	-----	-----	-----	-----

EVENT_LTCH	LINTO_LTCH	DSPNMI	RY_BY_FLASH	8530_IRQ	/LINTO	USERO
EVENT_LTCH	Status of the latched line Ext_event line from PLX9056					
LINTO_LTCH	Status of the latched line linto# from PLX9056					
DSPNMI:	Status of the CPCI-generated bit to activate an NMI interrupt to the processor					
RY_BY_FLASH	Status of the RY_BY pin from flash memory for use in its programming.					
8530_IRQ	Status of interrupt from SCC8530: when the value is "0", the interrupt is active.					
/LINTO	Status of interrupt line activated by the CPCI bus through the PLX 9056.					
USERO	Status of USERO line activated by the CPCI bus through the PLX 9056.					

**3.3.2.3 DSP\_CNTL1\_ADR 0x902F E808**

ED7	ED6	ED5	ED4	ED3	ED2	ED1	ED0
0	INT_8530_EN		LINTO_DIR				

LINTO\_DIR A "1" remove the direct connection of LINTO interrupt to the EXT\_NMI interrupt.

INT\_8530\_EN When set to "1" enables the 8530 interrupt as a source of the XINT\_INT6 - interrupt.

**3.3.2.4 DSP\_STAT1\_ADR 0x902F E80C**

ED7	ED6	ED5	ED4	ED3	ED2	ED1	ED0
		EXT_EVENTB					

EXT\_EVENTB Status of the DIRECT line Ext\_event line from PLX9056

**3.3.2.5 DSP\_CNTL2\_ADR 0x902F E810**

ED7	ED6	ED5	ED4	ED3	ED2	ED1	ED0
D_DSP7	D_DSP6	D_DSP5	D_DSP4	D_DSP3	D_DSP2	D_DSP1	D_DSP0

This register can be used as an inter-processor communication register with the PLX 9056.

**3.3.2.6 DSP\_STAT2\_ADR 0x902F E814**

ED7	ED6	ED5	ED4	ED3	ED2	ED1	ED0
P_CNT7	P_CNT6	P_CNT5	P_CNT4	P_CNT3	P_CNT2	P_CNT1	P_CNT0

This register can be used as an inter-processor communication register with the PLX 9056. Its value reflects what was written in the CPCI\_CNTRL1 register.

**3.3.2.7 DSP\_IPINT\_ADR 0x902F E820-E85C**

The TMS320C6713B supports 16 prioritized interrupts. In the present configuration, 5 interrupts are used by external hardware. Each interrupt can be programmed for edge/level and polarity. A set of multiplexer allocated the different source of interrupt to these 5 interrupts. See Interrupt registers details in the paragraph 3.3.3.

**3.3.2.8 DSP\_LINTI\_INTI 0x902F E840**

When DSP writes at this location, an interrupt is send to the HOST through the line /LINTI. The multiplexer must be set to "0". It is set to "0" upon reset.

**3.3.2.9 DSP\_LINTI\_RSTI 0x902F E844**

When the interrupt /LINTI is asserted, either the DSP or the CPCI must write to this register. CPCI\_LINTI\_RST located at Base + 0x10. The interrupt is also cleared the board reset.

**3.3.2.10 DSP\_CYC\_REV\_ADR 0x902F E860**

Unique 8 bits identifiers factory programmed within the Cyclone FPGA

ED7	ED6	ED5	ED4	ED3	ED2	ED1	ED0
0	0	0	0	0	0	0	1

**3.3.2.10.1 DSP\_PCB\_REV\_ADR[] 0x902F E864**

Unique 8 bits identifiers factory programmed within the Cyclone FPGA

ED7	ED6	ED5	ED4	ED3	ED2	ED1	ED0
0	0	0	0	0	0	0	1

**3.3.2.10.2 DSP\_PLX\_REV\_ADR[] 0x902F E868**

Unique 8 bits identifiers factory programmed within the Cyclone FPGA

ED7	ED6	ED5	ED4	ED3	ED2	ED1	ED0
1	0	1	0	0	1	0	1

**3.3.2.10.3 DSP\_DSP\_REV\_ADR[] 0x902F E86C**

Unique 8 bits identifiers factory programmed within the Cyclone FPGA

ED7	ED6	ED5	ED4	ED3	ED2	ED1	ED0
1	0	1	0	1	0	1	0

### 3.3.3 Interrupt Registers

0xB010 0080- B010 009C

#### 3.3.3.1 DSP SOURCE OF INTERRUPT

The sole source of interrupts to the DSP are :

- The IP modules
- The serial port 8530
- The Host through the PLX 9056
- External event signal

External interrupt	Name source	Function
XINT[4]	IP INTERRUPTS	
XINT[5]	IP INTERRUPTS	
XINT[6]	/LINTO /INT85/EXT_EVENT	HOST through PLX /SCC8530/EXTERNAL SIGNAL
XINT[7]	IP INTERRUPTS	
NMI	/LINTO	HOST through PLX

**NOTE: THE INTERRUPT NEEDS TO BE PROGRAMMED FOR NEGATIVE EDGE DETECTION AT TMS320C6713B LEVEL**

#### 3.3.3.2 INTERRUPT TO HOST

The LINTI # line is the sole source for the local hardware to interrupt the HOST.

Multiplexer allows to enable one or more of these source to drive the LINTI# line.

- The IP modules
- The serial port 8530
- External event signal

### 3.3.4 PLX 9056 Registers

Base address: 0x902FFE000

The TMS320C6713B can access the PLX configurations registers at the following addresses.

NAME	CPCI AD	LOCAL	FUNCTION
CPCIIDR	00h	00h	CPCI Configuration ID
CPCICR	04h	04h	CPCI Command
CPCISR	06h	06h	CPCI Status
CPCIREV	08h	08h	CPCI Revision ID
CPCICCR	09-0Bh	09-0Bh	CPCI Class Code
CPCICLSR	0Ch	0Ch	CPCI Cache Line Size
CPCILTR	0Dh	0Dh	CPCI Bus Latency Timer
CPCIHTR	0Eh	0Eh	CPCI Header Type
CPCIBISTR	0Fh	0Fh	CPCI Built-In Self-Test (BIST)
CPCIBAR0	10h	10h	CPCI Base Address for Memory Accesses to Local, Runtime, DMA, and Messaging Queue Registers
CPCIBAR1	14h	14h	CPCI Base Address for I/O Accesses to Local, Runtime, DMA, and Messaging Queue Registers
CPCIBAR2	18h	18h	CPCI Base Addr. for Accesses to Local Address Space 0
CPCIBAR3	1Ch	1Ch	CPCI Base Addr. for Accesses to Local Address Space 1
CPCIBAR4	20h	20h	CPCI Base Address
CPCIBAR5	24h	24h	CPCI Base Address
CPCICIS	28h	28h	CPCI Cardbus Information Structure Pointer
CPCISVID	2Ch	2Ch	CPCI Subsystem Vendor ID
CPCISID	2Eh	2Eh	CPCI Subsystem ID
CPCIERBAR	30h	30h	CPCI Base Address for Local Expansion ROM
CAP_PTR	34h	34h	New Capability Pointer
CPCIILR	3Ch	3Ch	CPCI Interrupt Line
CPCIIPR	3Dh	3Dh	CPCI Interrupt Pin
CPCIMGR	3Eh	3Eh	CPCI Minimum Grant
CPCIMLR3	3Fh	3Fh	CPCI Maximum Latency.
PMCAPID	40h	180h	Power Management Capability ID .
PMNEXT	41h	181h	Power Management Next Capability Pointer
PMC	42h	182h	Power Management Capabilities .
PMCSR	44h	184h	Power Management Control/Status
PMCSR_BSE	46h	186h	PMCSR Bridge Support Extensions
PMDATA	47h	187h	Power Management Data
HS_CNTL	48h	188h	Hot Swap Control
HS_NEXT	49h	189h	Hot Swap Next Capability Pointer .
HS_CSR	4Ah	18Ah	Hot Swap Control/Status .
PVPDID	4Ch	18Ch	CPCI Vital Product Identification .
PVPD_NEXT	4Dh	18Dh	CPCI Vital Product Data Next Capability Pointer
PVPDAD	4Eh	18Eh	CPCI Vital Product Data Address
PVPDATA	50h	190h	CPCI VPD Data .
LAS0RR	00h	80h	Direct Slave Local Address Space 0 Range
LAS0BA	04h	84h	Direct Slave Local Address Space 0 Local Base Address (Remap
MARBR	08h or ACh	88h or 12Ch	Mode/DMA Arbitration

NAME	CPCI AD	LOCAL	FUNCTION
BIGEND	0Ch	8Ch	Big/Little Endean Descriptor.
LMISC1	0Dh	8Dh	Local Miscellaneous Control
PROT_AREA	0Eh	8Eh	Serial EEPROM Write-Protected Address Boundary
LMISC2	0Fh	8Fh	Local Miscellaneous Control 2
EROMRR	10h	90h	Direct Slave Expansion ROM Range
EROMBA	14h	94h	Direct Slave Expansion ROM Local Base Address Re BREQo Control
LBRD0	18h	98h	Local Address Space 0/Expansion ROM Bus Region Descriptor
DMRR	1Ch	9Ch	Local Range for Direct Master-to-CPCI
DMLBAM	20h	A0h	Local Base Address for Direct Master-to-CPCI Memory
DMLBAI	24h	A4h	Local Base Address for Direct Master-to-CPCI I/O Configuration
DMPBAM	28h	A8h	CPCI Base Address (Remap for Direct Master-to-CPCI Memory)
DMCFGA	2Ch	Ach	CPCI Configuration Address for Direct Master-to-CPCI I/O Configuration
LAS1RR	F0h	170h	Direct Slave Local Address Space 1 Range
LAS1BA	F4h	174h	Direct Slave Local Address Space 1 Local Base Address (Remap
LBRD1	F8h	178h	Local Address Space 1 Bus Region Descriptor
DMDAC	FC	17Ch	Direct Master CPCI Dual Address Cycles Upper Address
CPCIARB	100h	1A0h	CPCI Arbiter Control
PABTADR	104h	1A4h	CPCI Abort Address
MBOX0	40h 78h	or C0h	Mailbox 0
MBOX1	44h 7Ch	or C4h	Mailbox 1
MBOX2	48h	8Ch	Mailbox 2
MBOX3	4Ch	CCh	Mailbox 3
MBOX4	50h	D0h	Mailbox 4
MBOX5	54h	D4h	Mailbox 5
MBOX6	58h	D8h	Mailbox 6
MBOX7	5Ch	DCh	Mailbox 7
P2LDBELL	60h	E0h	CPCI-to-Local Doorbell
L2PDBELL	64h	E4h	Local-to-CPCI Doorbell
INTCSR	68h	E8h	Interrupt Control/Status
CNTRL	6Ch	ECh	Serial EEPROM Control, CPCI Command Codes, User I/O Control, and Init Control
CPCIHIDR	70h	F0h	CPCI Hardwired Configuration ID
CPCIHREV	74h	F4h	sCPCI Hardwired Revision ID

NAME	CPCI AD	LOCAL	FUNCTION
DMAMODE0	80h	100h	DMA Channel 0 Mode
DMAPADR0	84h	104h	when DMAMODE0[20]=0
Or	88h	108h	when DMAMODE0[20]=1 DMA Channel 0 CPCI Address
DMALADR0	88h	108h	when DMAMODE0[20]=0
Or	8Ch	0Ch	when DMAMODE0[20]=1 DMA Channel 0 Local Address
DMASIZ0	8Ch	10Ch	when DMAMODE0[20]=0
Or	84h	4h	when DMAMODE0[20]=1 DMA Channel 0 Transfer Size Bytes
DMADPR0	90h	110h	DMA Channel 0 Descriptor Pointer
DMAMODE1	14h	114h	DMA Channel 1 Mode
DMAPADR1	98h	118h	when DMAMODE1[20]=0
Or	9Ch	11Ch	when DMAMODE1[20]=1 DMA Channel 1 CPCI Address
DMALADR1	9Ch	11Ch	when DMAMODE1[20]=0
Or	A0h	120h	when DMAMODE1[20]=1 DMA Channel 1 Local Address.
DMASIZ1	A0h	120h	when DMAMODE1[20]=0
Or	98h	118h	when DMAMODE1[20]=1 DMA Channel 1 Transfer Size Bytes
DMADPR1	A4h	124h	DMA Channel 1 Descriptor Pointer
DMACSR0	A8h	128h	DMA Channel 0 Command/Status
DMACSR1	A9h	129h	DMA Channel 1 Command/Status.
DMAARB	Ach	12Ch	DMA Arbitration
DMATHR	B0h	130h	DMA Threshold
DMADAC0	B4h	134h	DMA Channel 0 CPCI Dual Address Cycles Upper Address
DMADAC1	B8h	138h	DMA Channel 1 CPCI Dual Address Cycle Upper Address
OPQIS	30h	B0h	Outbound Post Queue Interrupt Status
OPQIM	34h	B4h	Outbound Post Queue Interrupt Mask.
IQP	40h		Inbound Queue Port.
OQP	44h		Outbound Queue Port
MQCR	C0h	140h	Messaging Queue Configuration
QBAR	C4h	144h	Queue Base Address
IFHPR	C8h	148h	Inbound Free Head Pointer
IFTPR	CCh	14Ch	Inbound Free Tail Pointer
IPHPR	D0h	150h	Inbound Post Head Pointer
IPTPR	D4h	154h	Inbound Post Tail Pointer
OFHPR	D8h	158h	Outbound Free Head Pointer
OFTPR	DCh	15Ch	Outbound Free Tail Pointer
OPHPR	E0h	160h	Outbound Post Head Pointer
OPTPR	E4h	164h	Outbound Post Tail Pointer
QSR	E8h	168h	Queue Status/Control

Detailed information can be found into the PLX 9056 data sheet.

### 3.3.5 RS-232C Port

Base address: 0x902FFE400  
Port A Control Register: 0x902FFE408  
Port A Data Register: 0x902FFE40C

The board uses the port A of a SCC85C230 to provide a serial interface. It use a 7.372800 MHz local clock oscillator. The port B has no outside connection.  
The interrupt from the serial controller is routed to the Cyclone to be shared with others interrupts source.

### 3.4 CE2 space

Base address :0xA0000000

The CE2 space is dedicated to the IP memory space. Total available addressing size will be 4 Mbytes if the space is defined as 32 bit wide access or 2 Mbytes if the CE2 space is defined as 16 bits access. The DSP 6713B shift the address accordingly.  
Presently the space is defined as 16 bit access. Each Industry Pack module will then share 512k bytes of memory. To be able to access the full possibilities of the IP memory space (8 Mbytes) a paging register is used.

RESOURCE	ADDRESS RANGE 16 BITS	ADDRESS RANGE 32 BITS
IPA MEMORY SPACE	A000 0000- A007 FFFF	A000 0000- A00F FFFF
IPB MEMORY SPACE	A008 0000- A00F FFFF	A010 0000- A01F FFFF
IPC MEMORY SPACE	A010 0000- A017 FFFF	A020 0000- A02F FFFF
IPD MEMORY SPACE	A018 0000- A01F FFFF	A030 0000- A03F FFFF

### 3.5 CE3 space

Base address :0xB0000000

The CE3 is shared between the boot FLASH as a 16-bit space and the Industry Pack IO space. This allows to for instance running a program stored into it, or in general to access the data continuously. By contrast when accessing the same FLASH at the address 0x90000000, only 2 bytes are valid in each 4 bytes.

RESOURCE	ADDRESS RANGE
Boot Flash	B000 0000- B00F FFFF
IP Control/Status Registers	B010 0000- B010 07FF
IPA SPACE (ID,IO,INT,DMA)	B010 0800- B010 09FF
IPB SPACE (ID,IO,INT,DMA)	B010 0A00- B010 0BFF
IPC SPACE (ID,IO,INT,DMA)	B010 0C00- B010 0DFF
IPD SPACE (ID,IO,INT,DMA)	B010 0E00- B010 0FFF



## 4 CPCI-Slave Address Map

### 4.1 PLX Address Map

### 4.2 Local Resources

There are 4 base address regions available on the PLX CPCI9056. The **CPCI-6713B\_4PACK** uses all 4 regions.

- BAR0:
- BAR1:
- BAR2:
- BAR3:

RESOURCE	PLX REGION	SPACE	ADDRESS RANGE	SIZE	LOCAL ADDRESS 16 bits	LOCAL ADDRESS 32 bits
PLX registers	BAR0	AS0	0x000- 0x1FF	32	\$902F E000	
IP_MEMORY	BAR2	AS2	0x00 0000- 0x3F FFFF	16	\$A000 0000- \$A01F FFFF	\$9030 0000- \$903F FFFF
Cyclone registers	BAR2	AS15	0x40 0000- 0x40 FFFF	16	\$902FE800	
Not Used	BAR2	AS15	0x41 0000- 0x41 FFFF	16		
DSP HPI registers Not Used	BAR2	AS15	0x42 0000- 0x42 FFFF	16		
IP Local registers	BAR2	AS 15	0x43 0000- 0x43 07FF	16	\$B010 0000	
IP_IO_SPACE	BAR2	AS 2- AS13	0x43 0800- 0x43 FFFF	16	\$B010 0800- \$B010 0FFF	\$9010 0800- \$9010 0FFF
IP_MEMORY A_B	BAR3	AS 1	0x0000 0000- 0x000F FFFF	32		\$9030 0000- \$9037 FFFF
IP_MEMORY C_D	BAR3	AS 1	0x0010 0000- 0x001F FFFF	32		\$9038 0000- \$903F FFFF
IP_IO SPACE	BAR3	AS 1	0x0020 0000- 0x003F FFFF	32		\$9010 0800- \$9010 0FFF

#### 4.2.1 Cyclone Registers

The HOST can access several registers located inside the CYCLONE FPGA.

These registers are used mainly to monitor the behavior of the board or to control and/or generate interrupt to the DSP. Details are provided above.

#### 4.2.1.1 CPCI\_CNTL0

Base + 0x0

ED7	ED6	ED5	ED4	ED3	ED2	ED1	ED0
DSPNMI	USERI_O	HINTEN	0	0		DSPRST	0

*DSPNMI*

A “1” generates an NMI interrupt to the TMS320C6713B. NMIEN bit must be selected.

*HINTEN*

Host interrupt enable. This bit, when set to “1”, allows the LINT1 signal to generate an interrupt on the CPCI. The default is “disabled”

*DSPRST*

When set to “1” by CPCI will maintain the TMS320C6713B on reset mode. It needs to be set back to “0” to remove the DSP reset.

#### 4.2.1.2 CPCI\_STAT0

Base + 0x4

ED7	ED6	ED5	ED4	ED3	ED2	ED1	ED0
0	N/A_	0	/LINTI			/LED_1_	/LED_0_

*/LINTI*

Status of the interrupt request line LINTI to the CPCI bus. When this bit is “0”, an interrupt is requested. HINTEN must be enabled for this line to actually generate an interrupt on the CPCI bus.

*DSP\_HINT*

Status of TMS320C6713B generated HPI interrupt

*/LED\_0*

Status of the LEDs controlled by the DSP. At reset, the LEDS are “off”. A “1” will turn the corresponding LED “on”.

*/LED\_1*

Status of the LEDs controlled by the DSP. At reset, the LEDS are “off”. A “1” will turn the corresponding LED “on”.

#### 4.2.1.3 CPCI\_CNTL1

Base + 0x8

ED7	ED6	ED5	ED4	ED3	ED2	ED1	ED0
P_CNT7	P_CNT6	P_CNT5	P_CNT4	P_CNT3	P_CNT2	P_CNT1	P_CNT0

The value written by the host in the CPCI\_CNTL1 register can be read by the DSP in the DSP\_STAT2 register.

#### 4.2.1.4 CPCI\_STAT1

Base + 0xC

ED7	ED6	ED5	ED4	ED3	ED2	ED1	ED0
D_DSP7	D_DSP6	D_DSP5	D_DSP4	D_DSP3	D_DSP2	D_DSP1	D_DSP0

The value written in the *DSP\_CNTL2* register by the DSP can be read by the host in this register.

#### 4.2.1.5 CPCI\_LINTI\_RST

Base + 0x10

A write at this address by the host will de-assert the line */LINTI* that has generated an interrupt on the CPCI bus.

#### 4.2.1.6 CPCI\_DSP\_INT

Base + 0x14

Not used

#### 4.2.1.7 CPCI\_CNTL2

Base + 0x18

This 32 bits registers is available on the CPCI side only for manufacturing test.

Not used

### 4.2.2 DSP HPI Registers

The HOST through the PLX 9056 can access to all the resource of the board through the Host Port Interface bus or H.P.I. of the DSP. It is a 16 bit bus with only four (4) registers locations. As the TMS320C6713B is a 32bit machine, every access consists of two consecutive 16 bit half words. The two DSP signals *HCNTL1* and *HCNTL0* that select the type of access are automatically generated by the board logic from the address used.

BAR3 offset	HCNTL1	HCNTL0	Description
0x20000	0	0	Host reads from or writes to the HPI control register (HPIC).
0x20004	0	1	Host reads from or writes to the HPI address register (HPIA).
0x20008	1	0	Host reads from or writes to the HPI data register (HPID) in <i>auto increment</i> mode. The HPI address register (HPIA) is post incremented by a word address ( four bytes addresses)
0x2000C	1	1	Host reads from or writes to the HPI data register (HPID) in <i>fixed</i> address mode. The HPI address register (HPIA) is not affected.

```
typedef struct hpi_t {
    long ctrl;
    long addr;
    long data;
    long autoinc;
} hpi_t;
hpi_t *hpi;

ULONG readHPI(ULONG addr)
{
    int i = 10000;

    hpi->addr = addr;
    hpi->ctrl = 0x00110011;
    while ((hpi->ctrl & 8)&& (i--)) ; // wait for ready
    if (i == 0) printf("\nTimeout accessing the HPI and waiting for ready\n");
    return hpi->data;
}

void writeHPI(ULONG addr, ULONG data)
{
    int i = 10000;
```

```

hpi->addr = addr & 0xfffffc; // force a 32 bit boundary
hpi->data = data;
hpi->ctrl = 0x00110011;
while ((hpi->ctrl & 8)&& (i--)) ; // wait for ready
if (i == 0) printf("\nTimeout accessing the HPI and waiting for ready\n");
}

```

## 5 MAIN BOARD CONNECTORS

### 5.1 Ps mode

Pin	Signal name	Description
1	DCLK	Clock Signal
2	GND	Ground
3	CONF_DONE	Configuration done
4	VCC	Power supply
5	nCONFIG	Configuration control
6	NC	No connect
7	nSTATUS	Configuration status
8	NC	No connect
9	DATA0	Data to Device
10	GND	Ground

### 5.2 Cyclone

#### 5.2.1 USB Byteblaster

The two Cyclones can be programmed using the ByteBlaster.  
Connector P1 is used for the I/O CYCLONE.  
Connector P2 is used for the DSP CYCLONE.

J2 Pin	Signal
Pin 1	DCLK
Pin2	GND
Pin3	DONE
Pin4	+3.3V
Pin5	nCONFIG
Pin6	nCE
Pin7	Data0
Pin8	IO nCSO
Pin9	IO ASDO
Pin10	GND

**Table 5-1 ByteBlaster pod**

The ByteBlaster programs the serial EEPROM EPCS1 or EPCS4, then the Programmed data are transferred to the CYCLONE using Asynchronous Serial Mode.

## 6 Industry Pack

### 6.1 Board Control / Status Registers

The following locations are the Control / Status registers for the IP MODULES. Most of the registers are accessible to both the DSP and the HOST.

HOST Address BAR2:	DSP LOCAL Address	Data	R/W	Description
0X00430XXX				IP BUS
	0XB0100004	D03-D00	R/W	IP memory page selection
	0XB0100008	N/A	WS	HOST Interrupt Acknowledge
	0XB0100010	D07-D00	R/W	IP Control/Status Register
	0XB0100014	D03-D00	R/W	Strobe Edge selection
	0XB0100020	N/A	WS	Next DMA End A
	0XB0100024	N/A	WS	Next DMA End B
	0XB0100028	N/A	WS	Next DMA End C
	0XB010002C	N/A	WS	Next DMA End D
	0XB0100030	N/A	WS	Clear BERR
	0XB0100038	N/A	WS	Software Strobe for manual clocking by DSP
	0XB0100040	D07-D00	R/W	Source selection for IPSTROBE_A and IPSTROBE_B
	0XB0100044	D07-D00	R/W	Source selection for IPSTROBE_C and IPSTROBE_D
	0XB0100048	D07-D00	R/W	Source selection for TINP_0 and TINP_1
	0XB0100060	N/A	WS	Clear Strobe
	0XB0100080	D07-D00	R/W	DSP Interrupt Enable Control register 0
	0XB0100084	D07-D00	R/W	DSP Interrupt Enable Control register 1
	0XB0100088	D07-D00	R/W	DSP Interrupt Enable Control register 2
	0XB010008C	D07-D00	W	IP RESET
	0XB0100090	D07-D00	R/W	DSP Interrupt Status register 0
	0XB0100094	D07-D00	R/W	DSP Interrupt Status register 1
	0XB0100098	D07-D00	R/W	DSP Interrupt Status register 2
	0XB010009C	D07-D00	R/W	DSP Interrupt Status register 0
	0XB01000A0	D07-D00	R/W	HOST Interrupt Enable Control register 0
	0XB01000A4	D07-D00	R/W	HOST Interrupt Enable Control register 1
	0XB01000A8	D07-D00	R/W	HOST Interrupt Enable Control register 2
	0XB01000B0	D07-D00	R/W	HOST Interrupt Status register 0
	0XB01000B4	D07-D00	R/W	HOST Interrupt Status register 1
	0XB01000B8	D07-D00	R/W	HOST Interrupt Status register 2

**Table 6.2: Control / Status Registers**

### 6.1.1 IP Memory Page selection

DSP Address: 0Xb0100004, Bits 03-00  
 CPCI Address: BAR2:0x0430004, Bits 07-00  
 Mode of Access: Read/Write

The limited space available for the IP memory by the DSP require to use a paging mode to access the full 8 Mbytes.

IP MEMORY ACCESS TYPE	PAGE SIZE BY IP	ADDRESS	CONDITION	BIT 03	BIT 02	BIT 01	BIT 00
DSP 16 BITS	512K	\$A010 0000-\$A01F FFFF		XADR22	XADR21	XADR20	XADR19
DSP 32BITS	1 M	\$9030 0000-\$903F FFFF	SPLIT_MEM_DSP = "0"	XADR22	XADR21	XADR20	LA19
	2M		SPLIT_MEM_DSP = "1"	XADR22	XADR21	LA20	LA19
PLX 16 BITS	1M	\$0000 0000-\$001F FFFF		XADR22	XADR21	XADR20	AOA19
PLX 32 BITS	1M	\$0000 0000-\$001F FFFF	SPLIT_MEM_PLX = "0"	XADR22	XADR21	XADR20	AOA19
	2M	\$0000 0000-\$001F FFFF	SPLIT_MEM_PLX = "1"	XADR22	XADR21	AOA20	AOA19

### 6.1.2 HOST Interrupt Acknowledge

DSP Address: 0Xb0100008, Bits 03-00  
 CPCI Address: Not Accessible  
 Mode of Access: Write Strobe

The DSP can write to this register to turn off the HOST interrupt generated by LINTI. It is intended for use by the HOST device driver.

### 6.1.3 IP Control Register

DSP Address: 0Xb0100010, Bits 07-00  
 CPCI Address: BAR2:0x0430010, Bits 07-00  
 Mode of Access: Read/Write  
 Reset By: CPCI Hardware Reset, Software Reset, Watchdog Reset

This register allows for setting the modes of access to the IPs.

BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 00
	IP C-D CLOCK		IP A-B CLOCK	SPLIT_MEM_DSP	MEM_32 CD_DSP	SPLIT_MEM_PLX	MEM_32CD_PLX

#### 6.1.3.1 MEM\_32CD\_PLX

This bit, when low (0), will the space allocated to the 32-bit interface IP\_MEMORY being exclusively for IP A\_B . When high (1), IP modules C\_D will be selected. Bit # 1 SPLIT\_MEM\_PLX must be set to "1".

### 6.1.3.2 SPLIT\_MEM\_PLX

This bit, when low (0), will allocated the 32-bit interface IP\_MEMORY space into two same size with address AOA[19] as switch.

### 6.1.3.3 MEM\_32CD\_DSP

This bit, when low (0), will the space allocated to the 32-bit interface IP\_MEMORY being exclusively for IP A\_B . When high (1), IP modules C\_D will be selected. Bit # 1 SPLIT\_MEM\_DSP must be set to "1".

See 32bit wide IP paragraph for more details

### 6.1.3.4 SPLIT\_MEM\_DSP

This bit, when low (0), will allocated the 32-bit interface IP\_MEMORY space into two same size with address LD[19] as switch.

See 32bit wide IP paragraph for more details

### 6.1.3.5 IP A-B CLOCK

This bit, when low (0), will clock IP module A and B at 8 MHz. When high (1), IP module A and B will be clocked at 32 MHz.

### 6.1.3.6 IP C-D CLOCK

This bit, when low (0), will clock IP module C and D at 8 MHz. When high (1), IP module C and D will be clocked at 32 MHz.

## 6.1.4 Strobe Edge selection

A "0" will enable a positive edge detection from the IPSTROBE signal.

A "1" will enable a negative edge detection from the IPSTROBE signal.

BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 00
				IP B STROBE	IP B STROBE	IP B STROBE	IP A STROBE

### 6.1.5 Next DMA End A,B,C,D

*DSP Address:* 0xb0100020,24,28,2C

*CPCI Address:* Not Accessible

*Mode of Access:* Write Strobe

According to the IP specification, the final DMA access of a transfer should occur with /IPDMAEND active low.

By writing to this location prior to the final IP DMA transfer, the IP DMA access will occur with /IPDMAEND active low. It is restored inactive high after the access.

If no significance to /IPDMAEND is required by the IP, then this protocol can be ignored.

### 6.1.6 Clear BERR

If an IP access times out due to an invalid access or some other problem, a status bit in IP Status Register is set. Writing to this location will clear those bits.

### 6.1.7 Software Strobe for manual clocking by DSP

### 6.1.8 DSP Interrupt Enable Control Register 0

DSP Address: 0Xb0100080  
CPCI Address: BAR2: 0x0430080  
Mode of Access: Read/Write

This register selects the interrupt source for the DSP\_INT4. The appropriate bit should be set (1) to allow that IP interrupt to trigger the DSP. When this bit is set, an interrupt will occur if an access to the corresponding IP resulted in a timeout. This would indicate a bad access on that IP.

BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 00
IP B, DMA1_ EN	IP B, DMA0_ EN	IP A, DMA1_ EN	IP A, DMA0_ EN	IP B, INT1 EN	IP B, INT0 EN	IP A, INT1 EN	IP A, INT0 EN

### 6.1.9 DSP Interrupt Enable Control Register 1

DSP Address: 0Xb0100084  
CPCI Address: BAR2: 0x0430084  
Mode of Access: Read/Write

This register selects the interrupt source for the DSP\_INT5. The appropriate bit should be set (1) to allow that IP interrupt to trigger the DSP. When this bit is set, an interrupt will occur if an access to the corresponding IP resulted in a timeout. This would indicate a bad access on that IP.

BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 00
IP D, DMA1_ EN	IP D, DMA0_ EN	IP C, DMA1_ EN	IP C, DMA0_ EN	IP D, INT1 EN	IP D, INT0 EN	IP C, INT1 EN	IP C, INT0 EN

### 6.1.10 DSP Interrupt Enable Control Register 2

DSP Address: 0Xb0100088  
CPCI Address: BAR2: 0x0430088  
Mode of Access: Read/Write

This register selects the interrupt source for the DSP\_INT6. The appropriate bit should be set (1) to allow that IP interrupt to trigger the DSP. When this bit is set, an interrupt will occur if an access to the corresponding IP resulted in a timeout. This would indicate a bad access on that IP.

BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 00
BERR D	BERR C	IP D STROBE	IP C STROBE	BERR B	BERR A	IP B STROBE	IP A STROBE

### 6.1.11 IP RESET

DSP Address: 0Xb010008C  
CPCI Address: BAR2: 0x043008C  
Mode of Access: Read Only

A write at this location will activated the IP reset line to "low" resetting the IP modules.



## 6.2 DSP Interrupt enable and source

Bit	Signal
0	Intreq_A0
1	Intreq_A1
2	Intreq_B0
3	Intreq_B1
4	IP_DMA_A0
5	IP_DMA_A1
6	IP_DMA_B0
7	IP_DMA_B1

DSP \$B0100080

DSP\_INT\_4

Bit	Signal
0	Intreq_C0
1	Intreq_C1
2	Intreq_D0
3	Intreq_D1
4	IP_DMA_C0
5	IP_DMA_C1
6	IP_DMA_D0
7	IP_DMA_D1

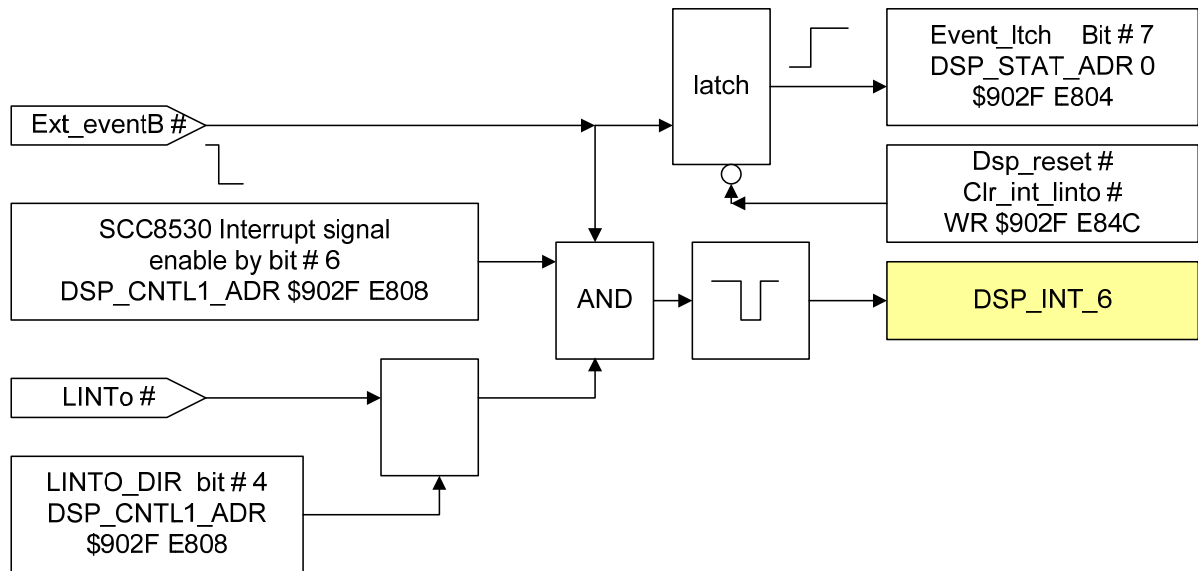
DSP \$B0100084

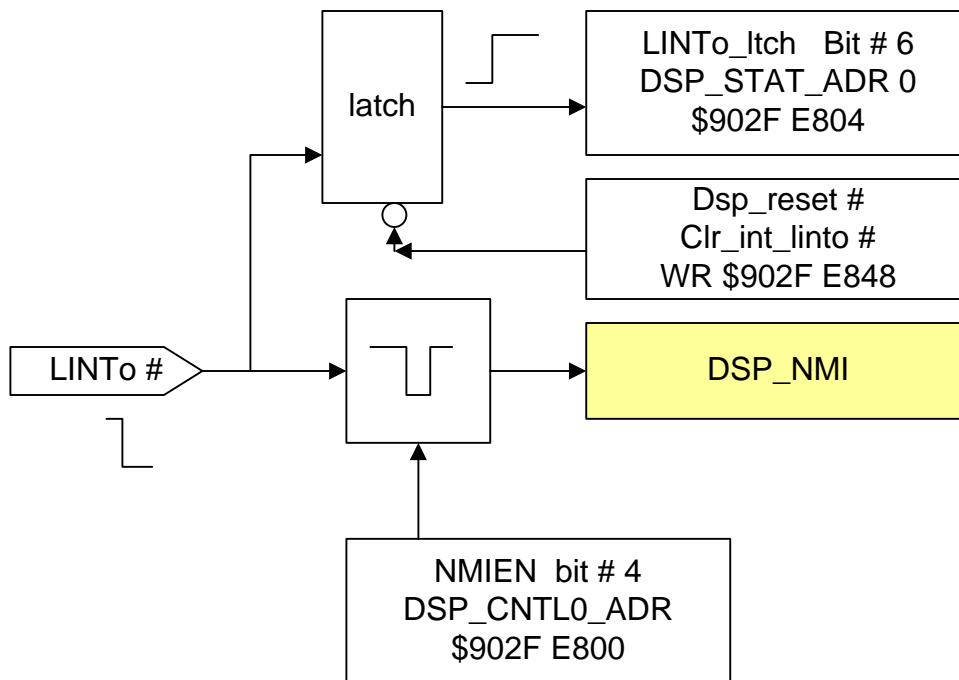
DSP\_INT\_5

Bit	Signal
0	IPSTROBE_A
1	IPSTROBE_B
2	Berr_A
3	Berr_B
4	IPSTROBE_C
5	IPSTROBE_D
6	Berr_C
7	Berr_D

DSP \$B0100088

DSP\_INT\_7





### 6.2.1 DSP Interrupt Status Register 0

DSP Address: 0Xb0100090  
 CPCI Address: BAR2: 0x0430090  
 Mode of Access: Read Only

This register allows the DSP interrupt routine for DSP\_INT4 to determine which of the IPs are causing an interrupt.

BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 00
IP B, DMA1	IP B, DMA0	IP A, DMA1	IP A, DMA0	IP B, INT1	IP B, INT0	IP A, INT1	IP A, INT0

When the applicable bit is low (0), the IP is asserting the /INT line.

The interrupt routine must ensure that all interrupts have been cleared prior to returning. Since the DSP interrupt must be pulsed, the logic only generates a pulse when the transition from no interrupts are asserted, to at least one interrupt is asserted.

### 6.2.2 DSP Interrupt Status Register 1

DSP Address: 0Xb0100094  
 CPCI Address: BAR2: 0x0430094  
 Mode of Access: Read Only

This register allows the DSP interrupt routine for DSP\_INT4 to determine which of the IPs are causing an interrupt.

BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 00
IP D, DMA1	IP D, DMA0	IP C, DMA1	IP C, DMA0	IP D, INT1	IP D, INT0	IP C, INT1	IP C, INT0

When the applicable bit is low (0), the IP is asserting the /INT line.

The interrupt routine must ensure that all interrupts have been cleared prior to returning. Since the DSP interrupt must be pulsed, the logic only generates a pulse when the transition from no interrupts are asserted, to at least one interrupt is asserted.

### 6.2.3 DSP Interrupt Status Register 2

DSP Address: 0Xb0100098  
 CPCI Address: BAR2: 0x0430098  
 Mode of Access: Read Only

This register allows the DSP interrupt routine for DSP\_INT4 to determine which of the source's are causing an interrupt.

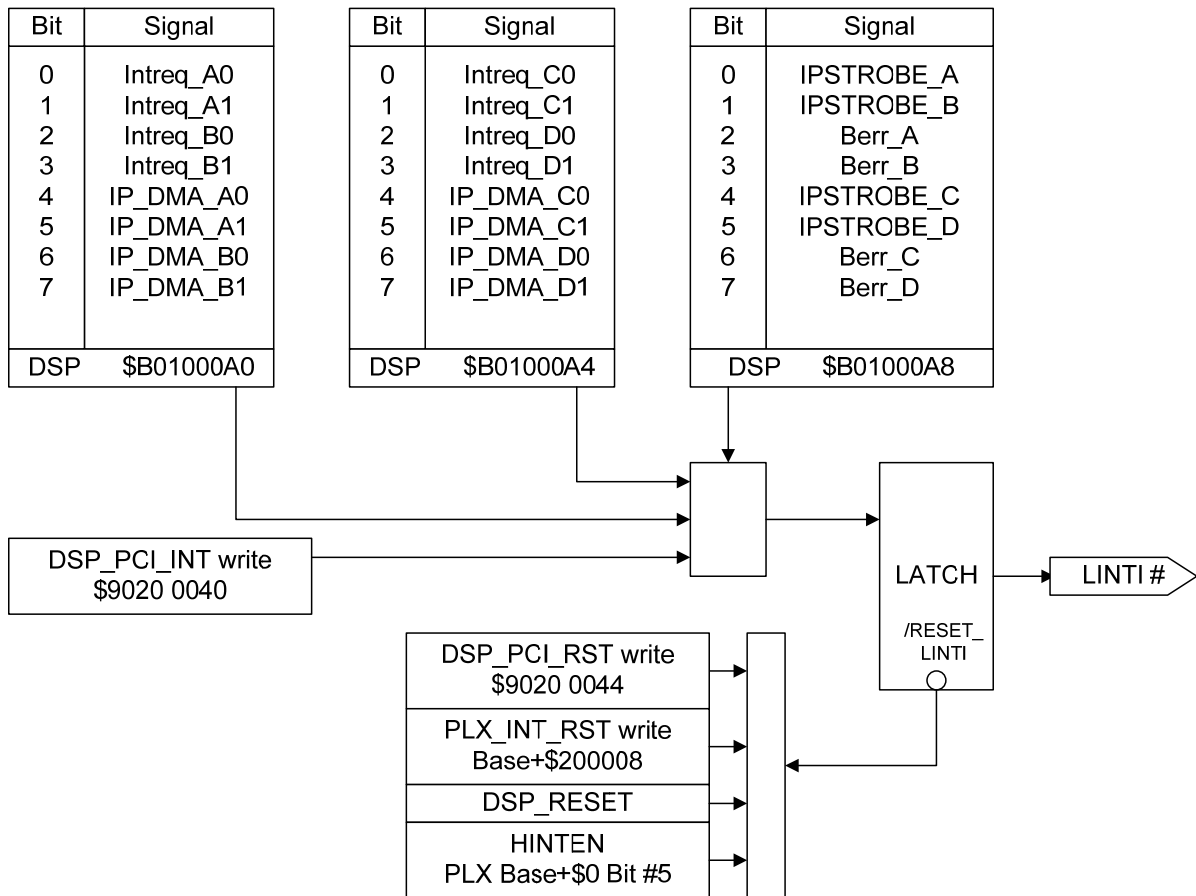
BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 00
BERR D	BERR C	STROBE D	STROBE C	BERR B	BERR A	STROBE B	STROBE A

When the applicable bit is low (0), the IP is asserting the /INT line.

The interrupt routine must ensure that all interrupts have been cleared prior to returning. Since the DSP interrupt must be pulsed, the logic only generates a pulse when the transition from no interrupts are asserted, to at least one interrupt is asserted.

This bit is cleared by writing to Clear BERR/STROBE.

### 6.3 HOST Interrupt Enable



#### 6.3.1 HOST Interrupt Enable Control Register 0

DSP Address: 0Xb01000A0  
 CPCI Address: BAR2: 0x04300A0  
 Mode of Access: Read/Write

The sole external source line use to interrupt the HOST is LINTI #.

Each of the IP interrupt lines or DMA request lines can be selected to generate an interrupt to the HOST.

Also a DSP to HOST strobe pulse can generate an interrupt to the HOST.

This register selects the interrupt source for the LINTI #. The appropriate bit should be set (1) to allow that IP interrupt to trigger the HOST.

When this bit is set, an interrupt will occur if an access to the corresponding IP resulted in a timeout. This would indicate a bad access on that IP.

BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 00
IP B, DMA1_ EN	IP B, DMA0_ EN	IP A, DMA1_ EN	IP A, DMA0_ EN	IP B, INT1 EN	IP B, INT0 EN	IP A, INT1 EN	IP A, INT0 EN

### 6.3.2 HOST Interrupt Enable Control Register 1

DSP Address: 0Xb01000A4

CPCI Address: BAR2: 0x04300A4

Mode of Access: Read/Write

This register selects the interrupt source for the the LINTI #. The appropriate bit should be set (1) to allow that IP interrupt to trigger the DSP.

When this bit is set, an interrupt will occur if an access to the corresponding IP resulted in a timeout. This would indicate a bad access on that IP.

BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 00
IP D, DMA1_ EN	IP D, DMA0_ EN	IP C, DMA1_ EN	IP C, DMA0_ EN	IP D, INT1 EN	IP D, INT0 EN	IP C, INT1 EN	IP C, INT0 EN

### 6.3.3 HOST Interrupt Enable Control Register 2

DSP Address: 0Xb01000A8

CPCI Address: BAR2: 0x04300A8

Mode of Access: Read/Write

This register selects the interrupt source for the the LINTI #. The appropriate bit should be set (1) to allow that IP interrupt to trigger the DSP.

When this bit is set, an interrupt will occur if an access to the corresponding IP resulted in a timeout. This would indicate a bad access on that IP.

BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 00
BERR D	BERR C	IP D STROBE	IP C STROBE	BERR B	BERR A	IP B STROBE	IP A STROBE

### 6.3.4 HOST Interrupt Status Register 0

DSP Address: 0Xb01000B0

CPCI Address: BAR2: 0x0430B0

Mode of Access: Read Only

This register allows the DSP interrupt routine for the LINTI # to determine which of the IPs are causing an interrupt.

BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 00
IP B, DMA1	IP B, DMA0	IP A, DMA1	IP A, DMA0	IP B, INT1	IP B, INT0	IP A, INT1	IP A, INT0

When the applicable bit is low (0), the IP is asserting the /INT line.

The interrupt routine must ensure that all interrupts have been cleared prior to returning. Since the DSP interrupt must be pulsed, the logic only generates a pulse when the transition from no interrupts are asserted, to at least one interrupt is asserted.

### 6.3.5 HOST Interrupt Status Register 1

DSP Address: 0Xb01000B4

CPCI Address: BAR2: 0x04300B4

Mode of Access: Read Only

This register allows the DSP interrupt routine for the LINTI # to determine which of the IPs are causing an interrupt.

BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 00
IP D, DMA1	IP D, DMA0	IP C, DMA1	IP C, DMA0	IP D, INT1	IP D, INT0	IP C, INT1	IP C, INT0

When the applicable bit is low (0), the IP is asserting the /INT line.

The interrupt routine must ensure that all interrupts have been cleared prior to returning. Since the DSP interrupt must be pulsed, the logic only generates a pulse when the transition from no interrupts are asserted, to at least one interrupt is asserted.

### 6.3.6 HOST Interrupt Status Register 2

DSP Address: 0Xb01000B8

CPCI Address: BAR2: 0x04300B8

Mode of Access: Read Only

This register allows the DSP interrupt routine for the LINTI # to determine which of the source's are causing an interrupt.

BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 00
BERR D	BERR C	STROBE D	STROBE C	BERR B	BERR A	STROBE B	STROBE A

When the applicable bit is low (0), the IP is asserting the /INT line.

The interrupt routine must ensure that all interrupts have been cleared prior to returning. Since the DSP interrupt must be pulsed, the logic only generates a pulse when the transition from no interrupts are asserted, to at least one interrupt is asserted.

This bit is cleared by writing to Clear BERR/STROBE.

## 6.4 IP module address map

HOST Address BAR2:	DSP Address	Data	R/W	Description
0X00430800	0XB0100800	D07-D00	R/W	IP A IDSPACE 16 bit
0X00430880	0XB0100880	D07-D00	R	IP A INTO/1 Acknowledge
0X00430900	0XB0100900	D15-D00	R/W	IP A IOSPACE 16 bit
0X00430980	0XB0100980	D15-D00	R/W	IP A IOSPACE 16 bit DMA
	0XA0000000	D15-D00	R/W	IP MEM A
0X00430A00	0XB0100A00	D07-D00	R/W	IP B IDSPACE 16 bit
0X00430A80	0XB0100A80	D07-D00	R	IP B INTO/1 Acknowledge
0X00430B00	0XB0100B00	D15-D00	R/W	IP B IOSPACE 16 bit
0X00430B80	0XB0100B80	D15-D00	R/W	IP B IOSPACE 16 bit DMA
	0XA0080000	D15-D00	R/W	IP MEM B
0X00430C00	0XB0100C00	D07-D00	R/W	IP C IDSPACE 16 bit
0X00430C80	0XB0100C80	D07-D00	R	IP C INTO/1 Acknowledge
0X00430D00	0XB0100D00	D15-D00	R/W	IP C IOSPACE 16 bit
0X00430D80	0XB0100D80	D15-D00	R/W	IP C IOSPACE 16 bit DMA
	0XA0100000	D15-D00	R/W	IP MEM C
0X00430E00	0XB0100E00	D07-D00	R/W	IP D IDSPACE 16 bit
0X00430E80	0XB0100E80	D07-D00	R	IP D INTO/1 Acknowledge
0X00430F00	0XB0100F00	D15-D00	R/W	IP D IOSPACE 16 bit
0X00430F80	0XB0100F80	D15-D00	R/W	IP D IOSPACE 16 bit DMA
	0XA0180000	D15-D00	R/W	IP MEM D
	0X90200800	D07-D00	R/W	IP A/B IOSPACE 32 bit
	0X90200900	D07-D00	R/W	IP A/B IOSPACE 32 bit DMA
	0X90200A00	D07-D00	R/W	IP C/D IOSPACE 32 bit
	0X90200B00	D07-D00	R/W	IP C/D IOSPACE 32 bit DMA

**Table 6.3: IP SPACE Registers**

#### **6.4.1 IP A 16-Bit ID Access**

*DSP Address:* 0Xb0100800 – 0Xb010087f, Bits 15-00

*CPCI Address:* BAR2: 0x0430000– 0x043007f

*Mode of Access:* Read / Write

Access to these locations generates a valid IP ID SPACE cycles to IP A.

#### **6.4.2 IP A Interrupt Acknowledge**

*DSP Address:* 0Xb0100880 – 0Xb010087f, Bits 15-00

*CPCI Address:* Not Accessible

*Mode of Access:* Read / Write

Reading from this location generates a valid IP Interrupt Acknowledge cycle to IP A.

0Xb0100880 issues an acknowledge to IP INT0, and 0Xb0100884 issues an acknowledge to IP INT1.

Note that this is not required by the carrier, and is only supported for those IP modules requiring it.

#### **6.4.3 IP A 16-Bit IO Access**

*DSP Address:* 0Xb0100900 – 0Xb010097f

*CPCI Address:* BAR2: 0x0430100– 0x043017f

*Mode of Access:* Read / Write

Access to these locations generates a valid IP IO SPACE cycles to IP A.

#### **6.4.4 IP A 16-Bit IO Access DMA**

*DSP Address:* 0Xb0100980 – 0Xb01009ff

*CPCI Address:* BAR2: 0x0430100– 0x043017f

*Mode of Access:* Read / Write

Access to these locations generates a valid IP IO SPACE cycles to IP A.

#### **6.4.5 IP B 16-Bit ID Access**

*DSP Address:* 0Xb0100a00 – 0Xb0100a7f

*CPCI Address:* BAR2: 0x0430200– 0x043027f

*Mode of Access:* Read / Write

Access to these locations generates a valid IP ID SPACE cycles to IP B.

#### **6.4.6 IP B Interrupt Acknowledge**

*DSP Address:* 0Xb0100A80 – 0Xb0100A7f, Bits 15-00

*CPCI Address:* Not Accessible

*Mode of Access:* Read / Write

Reading from this location generates a valid IP Interrupt Acknowledge cycle to IP A.

0Xb0100980 issues an acknowledge to IP INT0, and 0Xb0100984 issues an acknowledge to IP INT1.

Note that this is not required by the carrier, and is only supported for those IP modules requiring it.

#### **6.4.7 IP B 16-Bit IO Access**

*DSP Address:* 0Xb0100b00 – 0Xb0100b7f

*CPCI Address:* BAR2: 0x0430300– 0x043037f

*Mode of Access:* Read / Write

Access to these locations generates a valid IP IO SPACE cycles to IP B.

#### **6.4.8 IP B 16-Bit IO Access DMA**

*DSP Address:* 0Xb0100b80 – 0Xb0100bff

*CPCI Address:* BAR2: 0x0430300– 0x043037f

*Mode of Access:* Read / Write

Access to these locations generates a valid IP IO SPACE cycles to IP B.

#### **6.4.9 IP C 16-Bit ID Access**

*DSP Address:* 0Xb0100c00 – 0Xb0100c7f  
*CPCI Address:* BAR2: 0x0430400– 0x043047f  
*Mode of Access:* Read / Write

Access to these locations generates a valid IP ID SPACE cycles to IP C.

#### **6.4.10 IP C Interrupt Acknowledge**

*DSP Address:* 0Xb0100C80 – 0Xb0100C7f, Bits 15-00  
*CPCI Address:* Not Accessible  
*Mode of Access:* Read / Write

Reading from this location generates a valid IP Interrupt Acknowledge cycle to IP A.

0Xb0100C80 issues an acknowledge to IP INT0, and 0Xb0100C84 issues an acknowledge to IP INT1.

Note that this is not required by the carrier, and is only supported for those IP modules requiring it.

#### **6.4.11 IP C 16-Bit IO Access**

*DSP Address:* 0Xb0100d00 – 0Xb0100d7f  
*CPCI Address:* BAR2: 0x0430400– 0x043047f  
*Mode of Access:* Read / Write

Access to these locations generates a valid IP IO SPACE cycles to IP C.

#### **6.4.12 IP C 16-Bit IO Access DMA**

*DSP Address:* 0Xb0100d80 – 0Xb0100dff  
*CPCI Address:* BAR2: 0x0430400– 0x043047f  
*Mode of Access:* Read / Write

Access to these locations generates a valid IP IO SPACE cycles to IP C.

#### **6.4.13 IP D 16-Bit ID Access**

*DSP Address:* 0Xb0100e00 – 0Xb0100e7f  
*CPCI Address:* BAR2: 0x0430600– 0x043067f  
*Mode of Access:* Read / Write

Access to these locations generates a valid IP ID SPACE cycles to IP D.

#### **6.4.14 IP D Interrupt Acknowledge**

*DSP Address:* 0Xb0100E80 – 0Xb0100E7f, Bits 15-00  
*CPCI Address:* Not Accessible  
*Mode of Access:* Read / Write

Reading from this location generates a valid IP Interrupt Acknowledge cycle to IP A.

0Xb0100E80 issues an acknowledge to IP INT0, and 0Xb0100E84 issues an acknowledge to IP INT1.

Note that this is not required by the carrier, and is only supported for those IP modules requiring it.

#### **6.4.15 IP D 16-Bit IO Access**

*DSP Address:* 0Xb0100f00 – 0Xb0100f7f  
*CPCI Address:* BAR2: 0x0430700– 0x043077f  
*Mode of Access:* Read / Write

Access to these locations generates a valid IP IO SPACE cycles to IP D.

#### **6.4.16 IP D 16-Bit IO Access DMA**

*DSP Address:* 0Xb0100f80 – 0Xb0100fff  
*CPCI Address:* BAR2: 0x0430700– 0x043077f  
*Mode of Access:* Read / Write

Access to these locations generates a valid IP IO SPACE cycles to IP D.



#### 6.4.17 IP MEM BANK SELECTION

Space addressing limitations of the TMS320C6713B, request an smaller allocation of memory than the IPO specification allowed( 8 Mbytes). .

To allow access to larger MEM area, the board implements a paging mechanism. By setting these bits to the appropriate value, MEM spaces of up to 8 megabytes can be used.

DSP Address: 0Xb0100004  
CPCI Address: BAR2: 0x0430004  
Mode of Access: Read / Write  
Reset By: CPCI Hardware Reset, Software Reset,  
Watchdog Reset

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MEM_SLT # 7	MEM_SLT # 6	MEM_SLT # 5	MEM_SLT # 4	ADDR #22	ADDR #21	ADDR #20	ADDR #19

#### 6.4.18 16 bits wide IP

##### 6.4.19 IP A 16-Bit MEM Access

DSP Address: 0xa0000000 – 0xa007ffff  
CPCI Address: BAR2: 0x000000– 0x0fffff  
Mode of Access: Read / Write  
Access to these locations generates a valid IP MEM SPACE cycles to IP A.

##### 6.4.20 IP B 16-Bit MEM Access

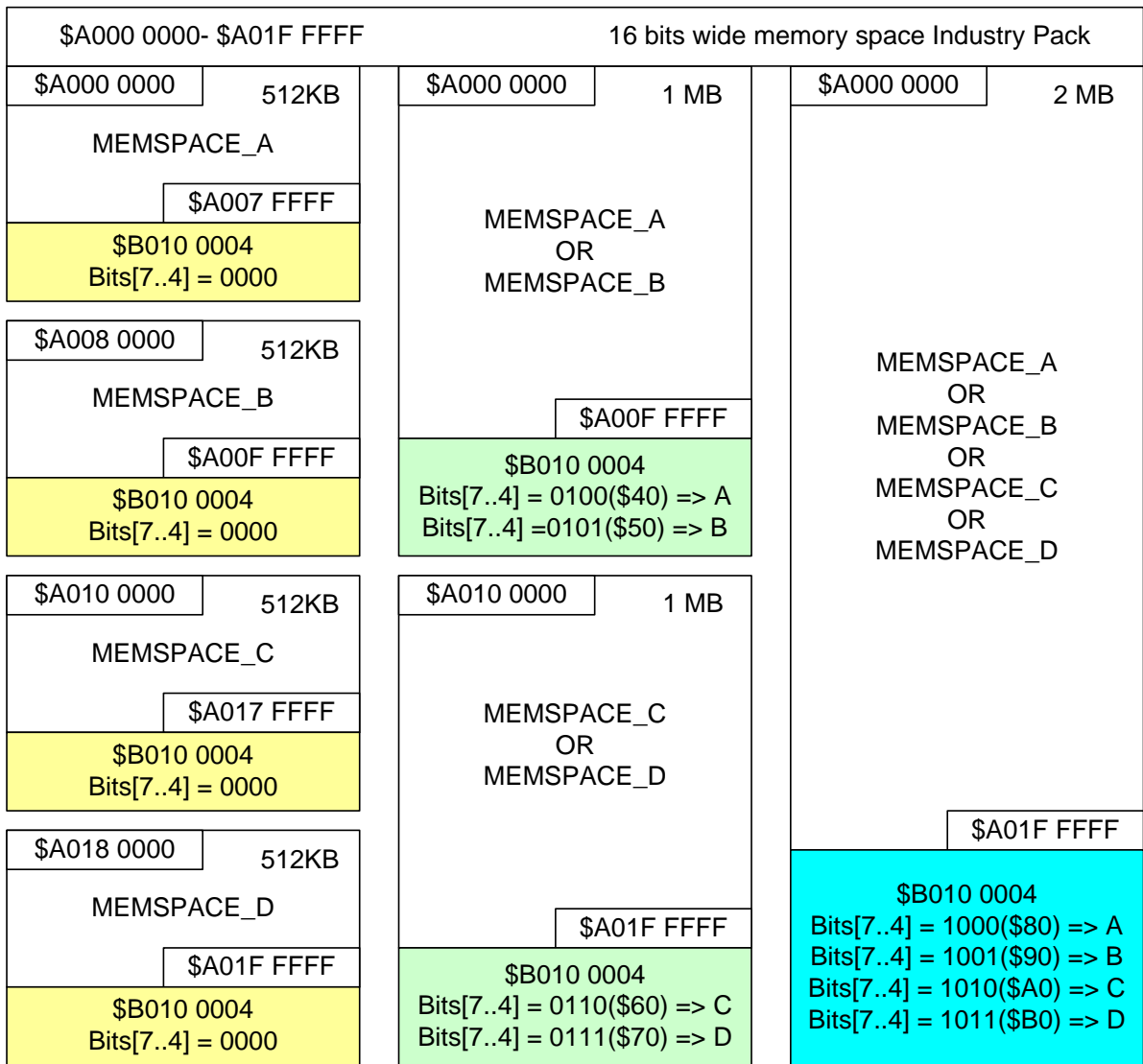
DSP Address: 0xa0080000 – 0xa00fffff  
CPCI Address: BAR2: 0x100000– 0x1fffff  
Mode of Access: Read / Write  
Access to these locations generates a valid IP MEM SPACE cycles to IP B.

##### 6.4.21 IP C 16-Bit MEM Access

DSP Address: 0xa0100000 – 0xa017ffff  
CPCI Address: BAR2: 0x200000– 0x2fffff  
Mode of Access: Read / Write  
Access to these locations generates a valid IP MEM SPACE cycles to IP C.

##### 6.4.22 IP D 16-Bit MEM Access

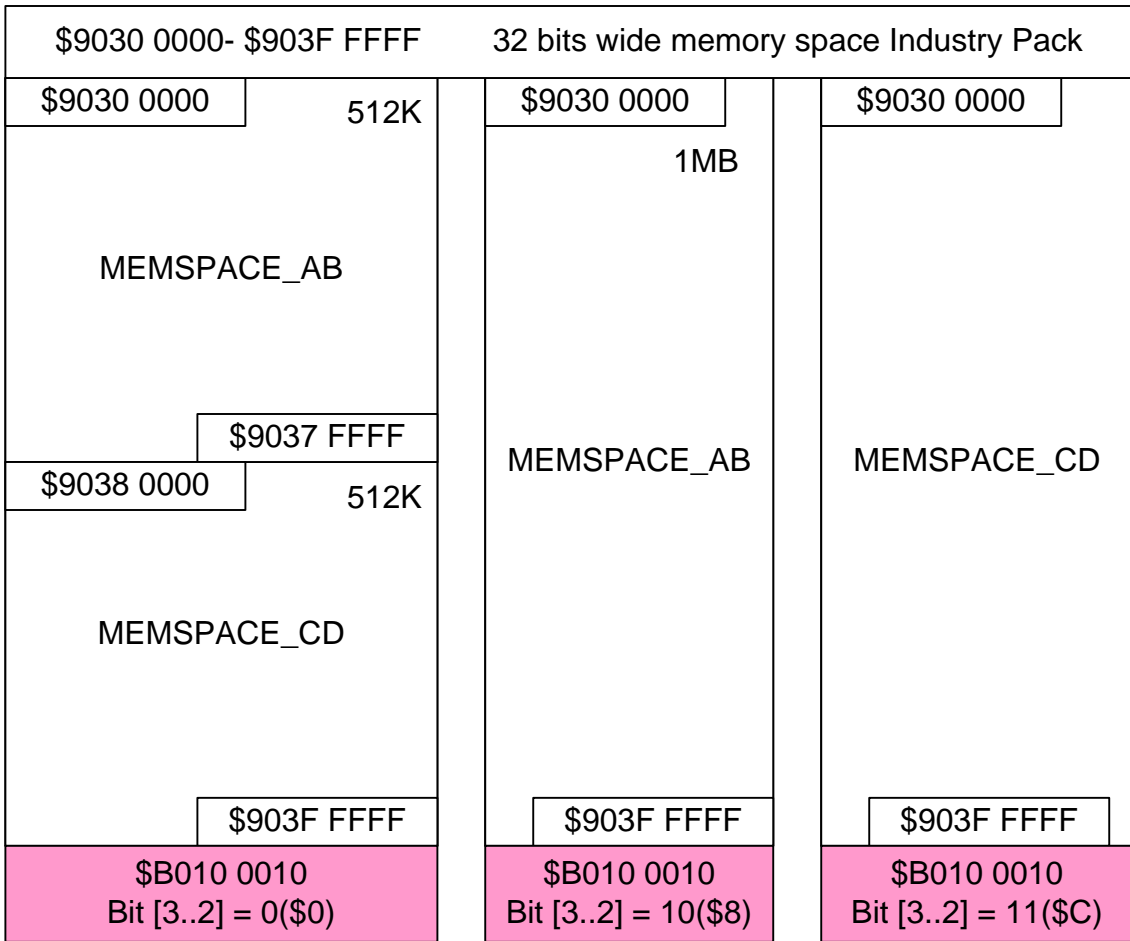
DSP Address: 0xa0180000 – 0xa01fffff  
CPCI Address: BAR2: 0x300000– 0x3fffff  
Mode of Access: Read / Write  
Access to these locations generates a valid IP MEM SPACE cycles to IP D.

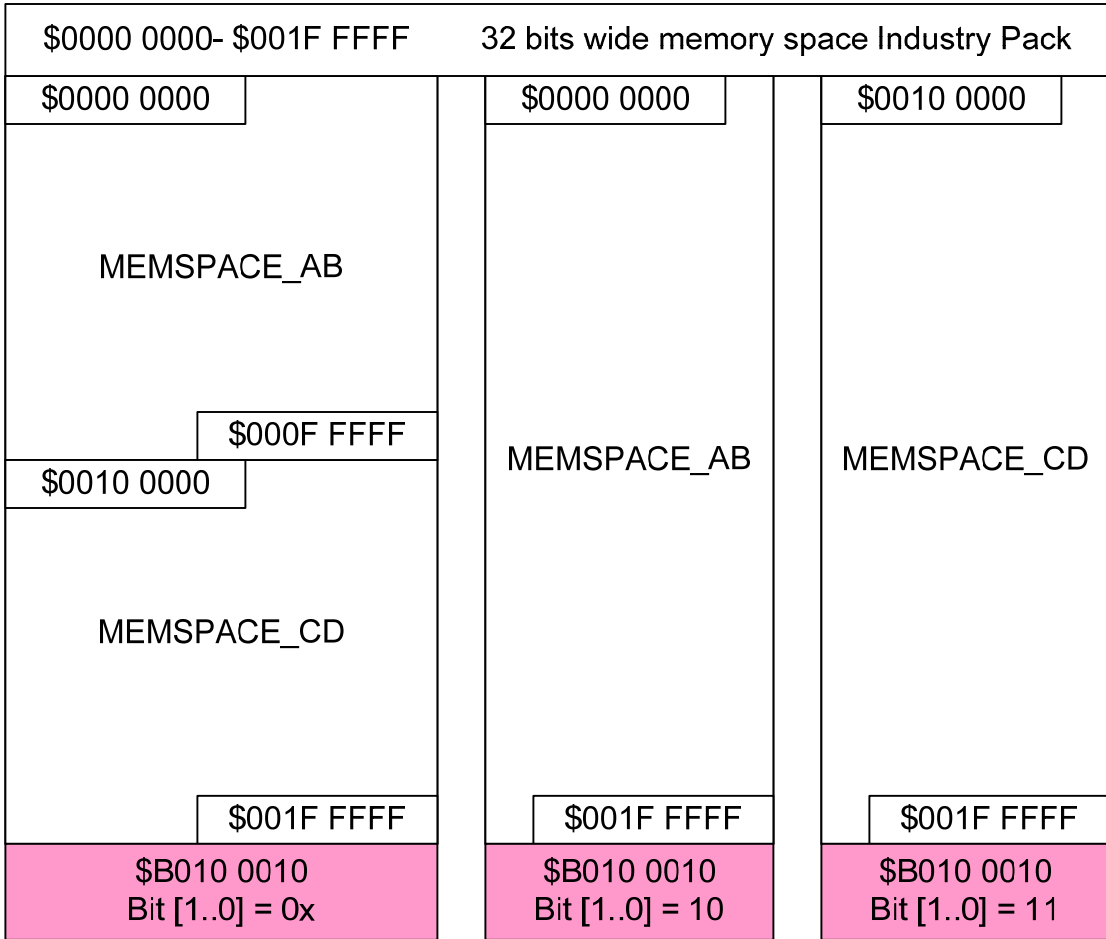


#### 6.4.23 32 bits wide IP

DSP Address: 0Xb0100010  
 CPCI Address: BAR2: 0x0430010  
 Mode of Access: Read / Write  
 Reset By: CPCI Hardware Reset, Software Reset,  
 Watchdog Reset

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	IPC-D 32 MHZ		IPA-B 32 MHZ	SPLIT_ MEM_DSP	MEM_32 CD_DSP	SPLIT_ MEM_ PLX	MEM_ 32CD_ PLX





#### 6.4.24 Software Strobe for manual clocking by DSP

DSP Address: 0xb0100038  
CPCI Address: Not Accessible  
Mode of Access: Write Strobe

A write to this location can potentially trigger a conversion or other event if selected in the **Clock / INT Configuration Registers**.

#### 6.4.25 Clock / INT Configuration Registers

DSP Address: 0xb0100040 – 0xb010005c, Bits 07 – 00  
CPCI Address: Not Accessible  
Mode of Access: Mixed  
Reset By CPCI Hardware Reset, Software Reset,  
Watchdog Reset

These registers control the External trigger and IPstrobe signals (4) from the IP module signal routing inside the card, as well as allow for the control and monitoring of the EXT trigger line. All of the registers are read/write, except for the EXT monitoring bits, which are read only.

A 4 pin connector J3 provide the following signal to/from the external environment.

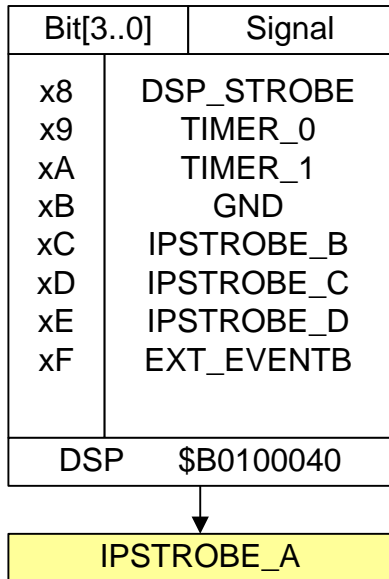
J2	Signal	Type
Pin 1	External Event	Input (negative pulse)
Pin 2	Buffered DSP timer #0	Output
Pin 3	Buffered Strobe Out	Output
Pin 4	GND	Ground

Each of the IPSTROBE can be selected as the destination or the source for the others IPSTROBE, External trigger or DSP Software Strobe.  
 The IPSTROBE selected as output must have then Bit # 3 IPSTROBE EN must be high (1). If the IP generates IPSTROBE, then Bit # 3 should be low (0).

**IPSTROBE\_A**

*DSP Address:* 0xb0100040 – Bits 00 – 03  
*CPCI Address:* Not Accessible  
*Mode of Access:* Mixed  
*Reset By* CPCI Hardware Reset, Software Reset, Watchdog Reset

Bit # 3 is set to “1” to enable the IPSTROBE as Output.



**Table 6.4: Source for IPSTROBE A**

**IPSTROBE\_B**

*DSP Address:* 0xb0100040 – Bits 07 – 04  
*CPCI Address:* Not Accessible  
*Mode of Access:* Mixed  
*Reset By* CPCI Hardware Reset, Software Reset, Watchdog Reset

Bit # 7 is set to “1” to enable the IPSTROBE as Output.

Bit[7..4]	Signal
8x	DSP_STROBE
9x	TIMER_0
Ax	TIMER_1
Bx	IPSTROBE_A
Cx	GND
Dx	IPSTROBE_C
Ex	IPSTROBE_D
Fx	EXT_EVENTB
DSP	\$B0100040

↓

IPSTROBE_B
------------

**Table 6.5: Source for IPSTROBE B**

## IPSTROBE\_C

DSP Address: *0xb0100044 – Bits 00 – 03*  
CPCI Address: *Not Accessible*  
Mode of Access: *Mixed*  
Reset By: *CPCI Hardware Reset, Software Reset,  
Watchdog Reset*

Bit # 3 is set to “1” to enable the IPSTROBE as Output.

Bit[3..0]	Signal
x8	DSP_STROBE
x9	TIMER_0
xA	TIMER_1
xB	IPSTROBE_A
xC	IPSTROBE_B
xD	GND
xE	IPSTROBE_D
xF	EXT_EVENTB

DSP    \$B0100044

↓

IPSTROBE\_C

**Table 6.6: Source for IPSTROBE C**

## IPSTROBE\_D

DSP Address: *0xb0100044 – Bits 07 –043*  
CPCI Address: *Not Accessible*  
Mode of Access: *Mixed*  
Reset By: *CPCI Hardware Reset, Software Reset,  
Watchdog Reset*

Bit # 7 is set to “1” to enable the IPSTROBE as Output.



Bit[7..4]	Signal
8x	DSP_STROBE
9x	TIMER_0
Ax	TIMER_1
Bx	IPSTROBE_A
Cx	IPSTROBE_B
Dx	IPSTROBE_C
Ex	GND
Fx	EXT_EVENTB
DSP	\$B0100044

↓

IPSTROBE_D
------------

**Table 6.7: Source for IPSTROBE D**

### 6.4.25.1 DSP Tinutp #0 Input Source

The DSP TMS320C6713B has two input lines used for timer #0 or different interrupts.

DSP Address: *0xb0100048 – Bits 00 – 03*  
CPCI Address: *Not Accessible*  
Mode of Access: *Mixed*  
Reset By: *CPCI Hardware Reset, Software Reset, Watchdog Reset*

Bit[3..0]	Signal
8	IPSTROBE_A
9	IPSTROBE_B
A	IPSTROBE_C
B	IPSTROBE_D
C	EXT_EVENTB

DSP	\$B0100048
-----	------------

↓

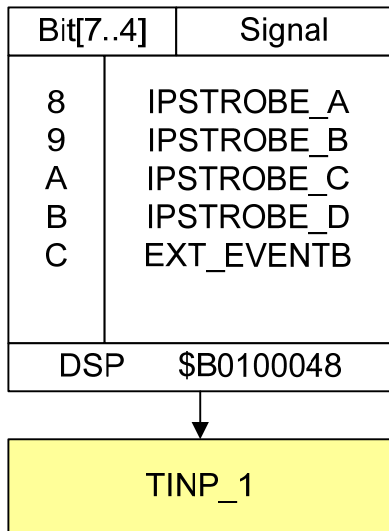
TINP_0
--------

**Table 6.8: Source for Tinutp # 0**

### 6.4.25.2 DSP Tinutp # 1 Input Source

The DSP TMS320C6713B has two input lines that can be source for timer #0 and timer#1 or different interrupts.

DSP Address: 0xb0100044 – Bits 07 – 04  
 CPCI Address: Not Accessible  
 Mode of Access: Mixed  
 Reset By: CPCI Hardware Reset, Software Reset,  
 Watchdog Reset

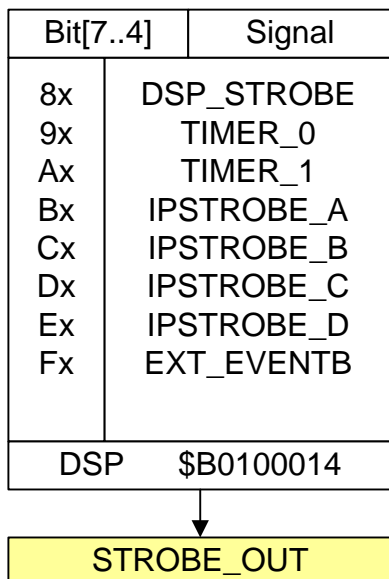


**Table 6.9: Source for Tinput # 1**

#### 6.4.25.3 EXT STROBE Direct Output J4

DSP Address: 0xb0100014, Bits 07 – 04  
 CPCI Address: Not Accessible  
 Mode of Access: Read/Write  
 Reset By: CPCI Hardware Reset, Software Reset,  
 Watchdog Reset

The EXT Trigger can be driven to a specific logic state for gating or other applications.



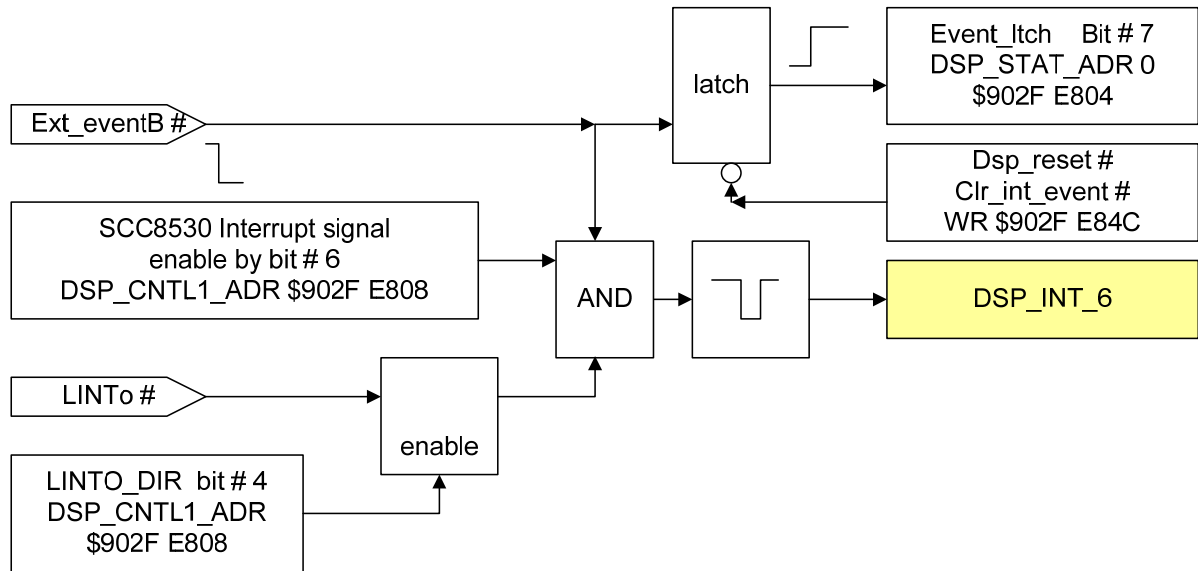
### 6.4.25.4 EXT\_EVENTB and LINTO # Monitor

The LINTO # direct signal status can be know at:

DSP\_STAT0\_ADR               \$902F E804               bit #1

The EXT\_EVENTB signal direct signal status can be know at:

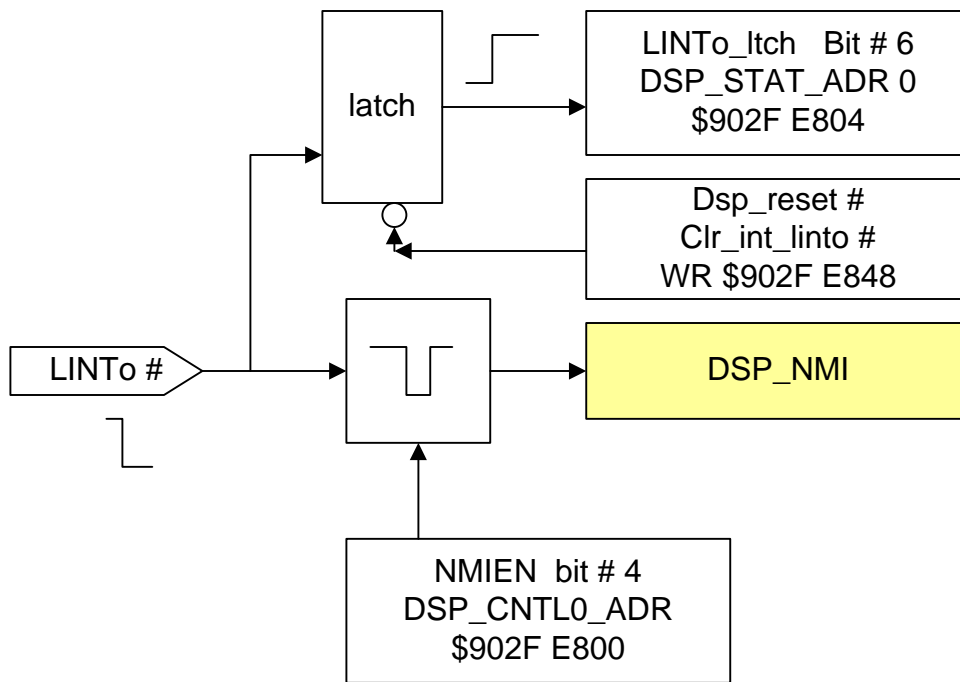
DSP\_STAT1\_ADR               \$902F E80C               bit #5



BIT #	Source	ADDRESS	RESET
1	EXT_EVENTB	\$902F E80C	
0	LINTO #	\$902F E804	

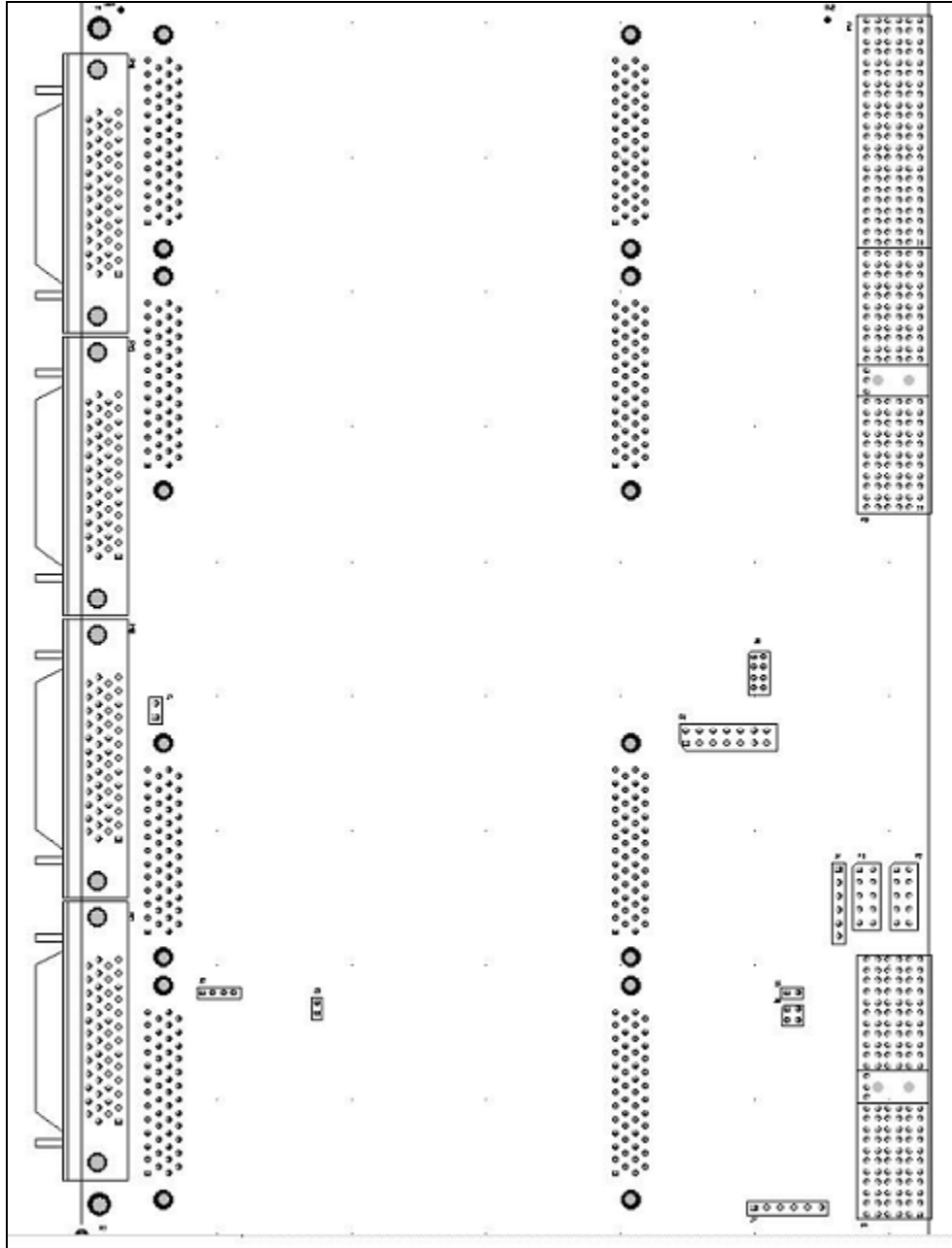
\$902F E848  
\$902F E84C

These bits reflect the current state of the EXT Trigger line.



## 6.5 Connectors, Jumpers, and LEDs

6.6 The jumper and connector placement is depicted below.



**Figure 6.1: Jumper and Connector Locations**

## 7 Jumper Descriptions

JUMPER	FACTORY SETTING	DESCRIPTION
J1	None	When shorted, provides DSP and board reset.
J2	None	Trigger Select
J3	1-2	Factory use. Always connect 1-2.
J4	None	Factory use. Never connect.
J5	1-2	DSP Boot Mode: CE1 width 16-bit, Asynchronous external ROM boot with default timings.
J6	connector for the FPGA programming	Factory use. Never connect.
J7	connector for the PLX JTAG	Factory use. Never connect.
J8	None	User select with read Back Register

**Table 7.10 Jumper Descriptions**

### 7.1 CONNECTIONS

### 7.2 Connector Descriptions

JUMPER	DESCRIPTION
P1	CPCI Connector
P2	RS-232 Port
P3	FPGA Programming (Factory Use)
P4	JTAG DSP
P5	IP A Bus
P6	IP B Bus
P7,17	I/O IP A
P8,18	I/O IP B
P9	Rear I/O IP A and IP B
P10	IP C Bus
P11	IP D Bus
P12,15	I/O IP C
P13,16	I/O IP D
P14	Rear I/O IP C and IP D

**Table 0.11 Connectors Descriptions**

#### 7.2.1.1 Serial Port (P2)

This 10 pin header allows a special cable with RS232 drivers and a 9 pin D connector to implement the serial port for debugging purposes.

An external cable is available.

W6	10 Pin connector for the serial cable	PIN 1 RS-232 RTS PIN 2 RS-232 TX PIN 3 RS-232 RX PIN 4 RS-232 CTS PIN 5 GND PIN 6 GND PIN 7 NC PIN 8 NC PIN 9 NC PIN 10 NC
----	---------------------------------------	---

**Table 0.12 Serial Connectors Descriptions**

#### 7.2.1.2 Emulator Connector (P4)

This connector is used to connect the emulator to the C6713B DSP.



### 7.2.1.3 Factory Use (P3)

This connector is used at the factory for programming the FPGA.

### 7.2.1.4 32 Bit CPCI Bus (P1)

This connector plugs into the backplane and provides the standard CPCI signals for all CPCI systems.

### 7.2.1.1 Rear I/O CPCI Bus (P9 and P14)

This connector plugs into the backplane and provides the rear I/O signal to the backplane.

## IP I/O CONNECTORS (P17, P18, P15, P16)

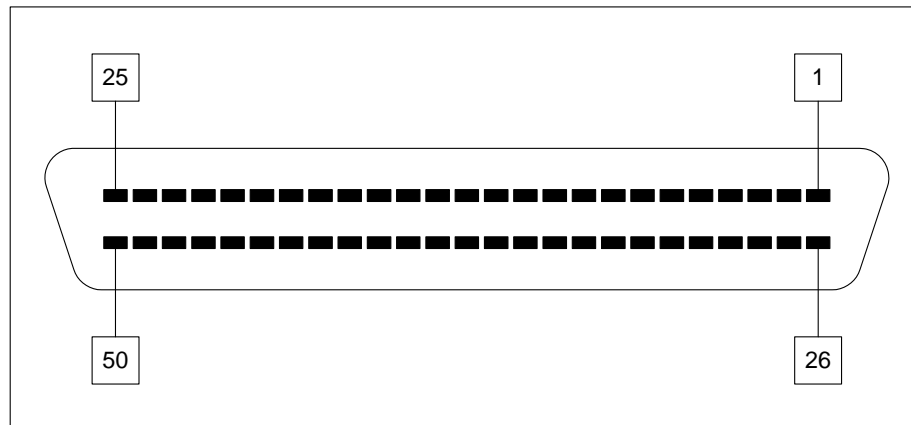
Connector	I/O for
P17	IP_A
P18	IP_B
P15	IP_C
P16	IP_D

A 50 pin subminiature D shelled connector is used to route the analog signals to the card. ALPHI Technology can supply transition modules and cable assemblies to meet any special requirements. Contact the factory for additional information.

Connectors are manufactured by AMP.

Use	Model
On PC Board	787190-5
Suggested Plug	749111-4

**Table 0.13: I/O Connector Model Numbers**



**Figure 0.2: External I/O Connector**

IP I/O Line	Backplane and Pin
IP_A:1	J4:11
IP_A:2	J4:36
IP_A:3	J4:61
IP_A:4	J4:86
IP_A:5	J4:111
IP_A:6	J4:10
IP_A:7	J4:35
IP_A:8	J4:60
IP_A:9	J4:85
IP_A:10	J4:110
IP_A:11	J4:9
IP_A:12	J4:34
IP_A:13	J4:59
IP_A:14	J4:84
IP_A:15	J4:109
IP_A:16	J4:8
IP_A:17	J4:33
IP_A:18	J4:58
IP_A:19	J4:83
IP_A:20	J4:108
IP_A:21	J4:7
IP_A:22	J4:32
IP_A:23	J4:57
IP_A:24	J4:82
IP_A:25	J4:107
IP_A:26	J4:6
IP_A:27	J4:31
IP_A:28	J4:56
IP_A:29	J4:81
IP_A:30	J4:106
IP_A:31	J4:5
IP_A:32	J4:30
IP_A:33	J4:55
IP_A:34	J4:80
IP_A:35	J4:105
IP_A:36	J4:4
IP_A:37	J4:29
IP_A:38	J4:54
IP_A:39	J4:79
IP_A:40	J4:104
IP_A:41	J4:3
IP_A:42	J4:28
IP_A:43	J4:53
IP_A:44	J4:78
IP_A:45	J4:103
IP_A:46	J4:2
IP_A:47	J4:27
IP_A:48	J4:52
IP_A:49	J4:77
IP_A:50	J4:102

IP I/O Line	Backplane and Pin
IP_B:1	J4:25
IP_B:2	J4:50
IP_B:3	J4:75
IP_B:4	J4:100
IP_B:5	J4:125
IP_B:6	J4:24
IP_B:7	J4:49
IP_B:8	J4:74
IP_B:9	J4:99
IP_B:10	J4:124
IP_B:11	J4:23
IP_B:12	J4:48
IP_B:13	J4:73
IP_B:14	J4:98
IP_B:15	J4:123
IP_B:16	J4:22
IP_B:17	J4:47
IP_B:18	J4:72
IP_B:19	J4:97
IP_B:20	J4:122
IP_B:21	J4:21
IP_B:22	J4:46
IP_B:23	J4:71
IP_B:24	J4:96
IP_B:25	J4:121
IP_B:26	J4:20
IP_B:27	J4:45
IP_B:28	J4:70
IP_B:29	J4:95
IP_B:30	J4:120
IP_B:31	J4:19
IP_B:32	J4:44
IP_B:33	J4:69
IP_B:34	J4:94
IP_B:35	J4:119
IP_B:36	J4:18
IP_B:37	J4:43
IP_B:38	J4:68
IP_B:39	J4:93
IP_B:40	J4:118
IP_B:41	J4:17
IP_B:42	J4:42
IP_B:43	J4:67
IP_B:44	J4:92
IP_B:45	J4:117
IP_B:46	J4:16
IP_B:47	J4:41
IP_B:48	J4:66
IP_B:49	J4:91
IP_B:50	J4:116

IP I/O Line	Backplane and Pin
IP_C:1	J5:11
IP_C:2	J5:33
IP_C:3	J5:55
IP_C:4	J5:77
IP_C:5	J5:99
IP_C:6	J5:10
IP_C:7	J5:32
IP_C:8	J5:54
IP_C:9	J5:76
IP_C:10	J5:98
IP_C:11	J5:9
IP_C:12	J5:31
IP_C:13	J5:53
IP_C:14	J5:75
IP_C:15	J5:97
IP_C:16	J5:8
IP_C:17	J5:30
IP_C:18	J5:52
IP_C:19	J5:74
IP_C:20	J5:96
IP_C:21	J5:7
IP_C:22	J5:29
IP_C:23	J5:51
IP_C:24	J5:73
IP_C:25	J5:95
IP_C:26	J5:6
IP_C:27	J5:28
IP_C:28	J5:50
IP_C:29	J5:72
IP_C:30	J5:94
IP_C:31	J5:5
IP_C:32	J5:27
IP_C:33	J5:49
IP_C:34	J5:71
IP_C:35	J5:93
IP_C:36	J5:4
IP_C:37	J5:26
IP_C:38	J5:48
IP_C:39	J5:70
IP_C:40	J5:92
IP_C:41	J5:3
IP_C:42	J5:25
IP_C:43	J5:47
IP_C:44	J5:69
IP_C:45	J5:91
IP_C:46	J5:2
IP_C:47	J5:24
IP_C:48	J5:46
IP_C:49	J5:68
IP_C:50	J5:90

IP I/O Line	Backplane and Pin
IP_D:1	J5:22
IP_D:2	J5:44
IP_D:3	J5:66
IP_D:4	J5:88
IP_D:5	J5:110
IP_D:6	J5:21
IP_D:7	J5:43
IP_D:8	J5:65
IP_D:9	J5:87
IP_D:10	J5:109
IP_D:11	J5:20
IP_D:12	J5:42
IP_D:13	J5:64
IP_D:14	J5:86
IP_D:15	J5:108
IP_D:16	J5:19
IP_D:17	J5:41
IP_D:18	J5:63
IP_D:19	J5:85
IP_D:20	J5:107
IP_D:21	J5:18
IP_D:22	J5:40
IP_D:23	J5:62
IP_D:24	J5:84
IP_D:25	J5:106
IP_D:26	J5:17
IP_D:27	J5:39
IP_D:28	J5:61
IP_D:29	J5:83
IP_D:30	J5:105
IP_D:31	J5:16
IP_D:32	J5:38
IP_D:33	J5:60
IP_D:34	J5:82
IP_D:35	J5:104
IP_D:36	J5:15
IP_D:37	J5:37
IP_D:38	J5:59
IP_D:39	J5:81
IP_D:40	J5:103
IP_D:41	J5:14
IP_D:42	J5:36
IP_D:43	J5:58
IP_D:44	J5:80
IP_D:45	J5:102
IP_D:46	J5:13
IP_D:47	J5:35
IP_D:48	J5:57
IP_D:49	J5:79
IP_D:50	J5:101