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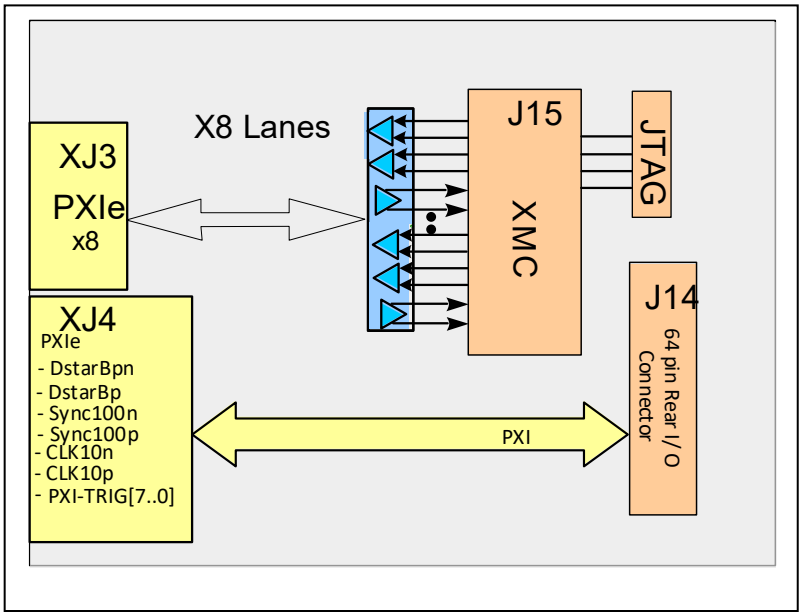
PXIe-XMC-IO

PXIe Module

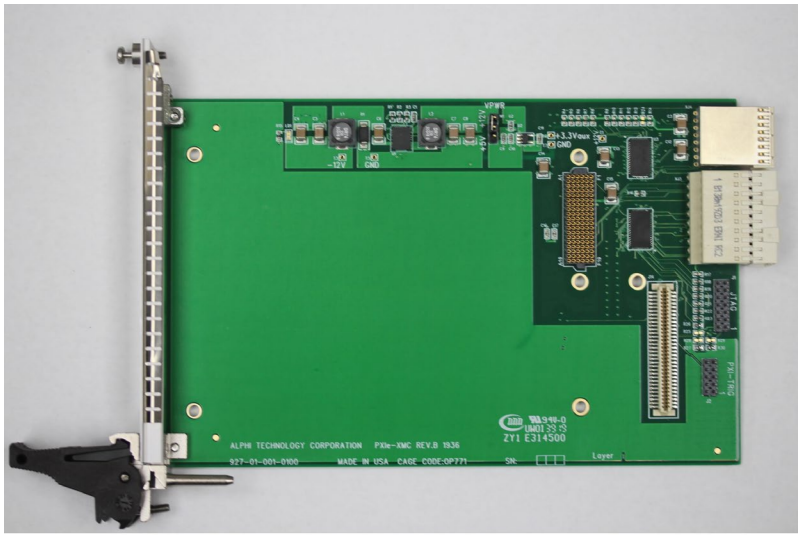
PXIexpress to XMC Non Intelligent Carrier with I/O Interface to Rear I/O

Features

- 3U PXIe form factor
- Single XMC carrier slot
- XMC Complies with ANSI/VITA 42.0-2008
- PXI Express x8 Lanes
- X8 Lanes Gen 1 Capable
- Connect User I/O from XMC to Clock and Trigger lane on XJ4
- On board XMC JTAG connector
- FPGA I/O bank control to PXI interface including Trigger and Clock



Block Diagram Overview



The PXIe-XMC-IO carrier allows a standard XMC module to be used in a PXI Express slot.

The carrier card interfaces an XMC mezzanine module to a PXI Express bus in a PXIe Chassis computer system. The PXIe bus adapter board allows a PXIe (PXIe bus master) to control and communicate with the hosted XMC module. It acts as an adapter to route signals between the system's PXIe bus and the XMC module connector. The I/O signals from the XMC are routed to the rear I/O and used to provide additional Ports controlled by the XMC. The added I/O ports are electrically controlled by the XMC module. The PXIe and PXI signals are routed to the FPGA via the user I/O J14 on the XMC.

Ordering Information	
PXIe-XMC-IO	PXIe to XMC Carrier with I/O

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