

Summary

- Altera FPGA
- 48 I/O lines, available by groups of 8
- Direct read back via the 74FCT652
- Pre-loadable outputs with strobe line for sync
- Change of state with interrupt generation
- Pattern match with 8 bit pre-load & interrupt
- 48 I/O lines, available by groups of 8
- 2 interrupts
- 2 optional timers
- User programmable with via Altera tools.
- Programmable via IP bus or bit/byte blaster
- Local serial Eprom
- Optional clock osc.
- 8/32 Mhz IP clock support
- Vita 4 compliant



BI-DIRECTIONAL TTL I/O WITH ALTERA FLEX FPGA



IP-ALTEA IO

Features

- Altera FPGA 10K20
- 48 user I/O lines
- Single wide Industry Pack
- TTL Outputs
- Optional User clock oscillator

Memory

- Internal

I/O Level

- TTL I/O

Programmable via

- Bit / Byte Blaster
- Serial Eprom
- IP Bus
- Multiple example

IP interface

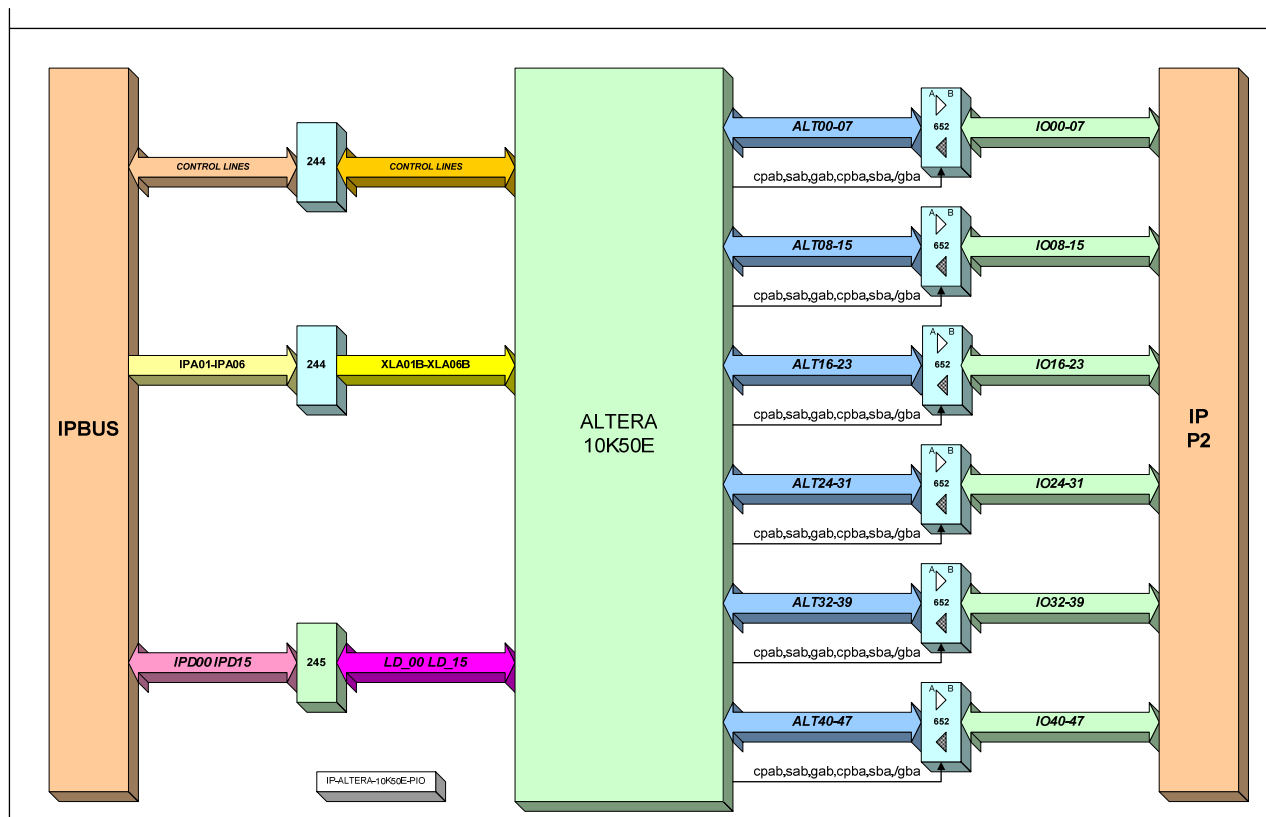
- 8/32 Mhz clock
- 16 bit data
- Interrupts
- DMA

Operating: Environmental

- Operating temperature
 Commercial: 0 to +55 °C
 Optional: -25°C to +80°C
- Non-operating: -40°C to 85 °C
- Airflow requirement: .5 CFM
- Humidity: 5 to 90% (non-cond.)
- Altitude: 0 to 10'000 ft

Mechanical: Environmental

- Size: Vita 4 Type 1 IP
 1.8" x 3.9"
- Power: 1 watt
- Vibration: 0.5G RMS
 20-2000 Hz rand
- Shock: 20 G, 11 ms, ½ sine
- Weight: tbd
- MTBF: >250000 hours



Functional Block Diagram

Ordering Information

Part Number : IP-Altera-IO

ALTERA 10K20 bi-directional ttl IO Industry Pack module

Optional Accessories

Part Number : TB-50-HDR
 Part Number : CBL-50-HDR

50 pin terminal block and 1meter flat ribbon cable
 50 pin,1meter flat ribbon cable, IDC header connector

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