# PCI-BCRTM

## MIL-STD-1553
## BCRTM
## PCI Module

### REFERENCE MANUAL

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## GENERAL DESCRIPTION

## INTRODUCTION

The PCI-BCRTM module provides Bus Controller (BC), Remote Terminal (RT) and Bus Monitor (BM) dual-redundant operations on the MIL-STD-1553 bus. The PCI form factor provide easy installation.

The ***PCI-BCRTM*** is installed with the following resources:

- UTMC BCRTM 1553 based processor unit
- 64K x 16 bit dual ported SRAM
- Supports Bus Controller, Remote Terminal and Bus Monitor mode
- RT address and operational modes are program or jumper selectable
- 1553 bus long or short stub jumper option with onboard transformers
- PCI VIO signaling

## FUNCTIONAL DESCRIPTION

A functional block diagram of the PCI module is depicted below in Figure 1.
The PCI-BCRTM is designed around the UTMC BCRTM CHIP, that can performs the 1553 bus operations without interaction with the host CPU once the UT1553B BCRTM

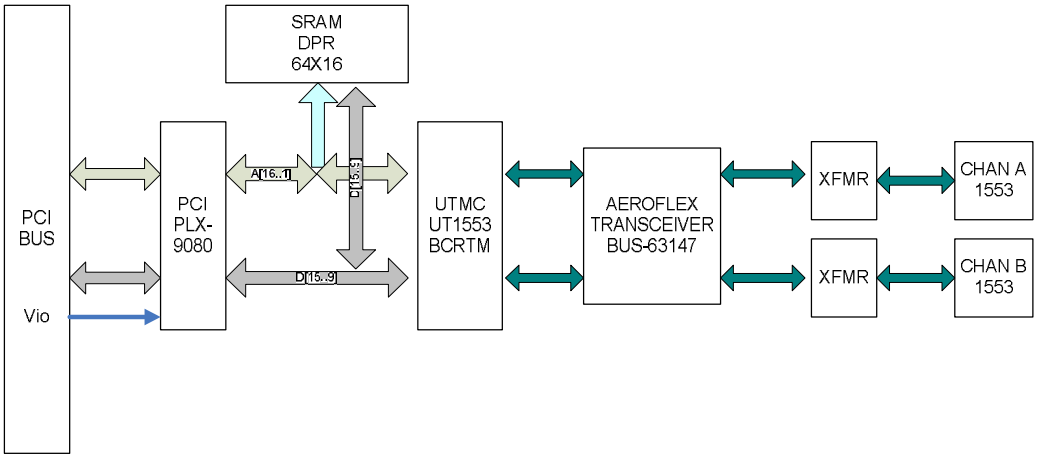


**Figure 1 PCI-BCRTM**

## REFERENCE MATERIALS LIST

The reader should refer to the UTMC Webb site for the complete BCRTM registers.

Manual and Data Sheet:
http://www.ams.aeroflex.com/ProductFiles/DataSheets/1553/bcrtm.pdf

**WWW Home Page :**
http://ams.aeroflex.com/

Technical Questions - Please Contact info-ams@aeroflex.com

The reader should refer to the PCI Local Bus Specification for a detailed explanation of the PCI bus architecture and timing requirements. This specification is available from the following source:

**PCI Special Interest Group**
**PO Box 14070**
**Portland, OR 97214**
**Tel: (800) 433-5177**
**Tel: (503) 797-4207**
**Fax: (503) 234-6762**

The reader is also referred to the PLX-9080 PCI Controller data book:

**PLX TECHNOLOGY**
**6195 Lusk Boulevard**
**San Diego, CA 92121-2793**
**Tel: (800) 755-2622**

# HOST (PCI) SIDE

### Interface to HOST (PCI)

All PCI devices contain a set of registers in Configuration Space which allow for determining the manufacturer and model of the device, determining the resources necessary for the correct operation of the device, and other configuration information. Configuration space is decoded on a per slot / device basis via a mechanism described in the PCI specification.

All PCI devices can be relocated in physical memory by means of several Base Address Registers. These registers contain the high address bits, which must be matched for any access to the card to be successful. Part of the protocol of programming the Base Address Registers allows for the transfer of information regarding the size of the regions. The actual Base Address Registers are located in Configuration Space.

Normally, configuring the card is performed by the system controller and some form of firmware or BIOS. Unfortunately, determining Base Addresses and other configuration information in Configuration Space is operating system dependent. One of the primary functions of the device driver under Windows NT is to map these resources to the user application. The card is actually accessed through the decoded base address registers.

### PCI Configuration Space

| | |
|---|---|
| *PCI Address:* | *CONFIG:0x00 – 0x3C* |
| *Mode of Access:* | *Read/Write* |
| *Reset By* | *PCI Hardware Reset* |

The card has the following registers available to PCI Configuration Space. They are implemented in the PLX chip. The registers are also accessible from the DSP Local bus.

| Offset Into PCI CFG | 31 – 24 | 23 – 16 | 15 – 8 | 7 – 0 |
|---|---|---|---|---|
| 0x00 | Device ID | | Vendor ID | |
| 0x04 | Status | | Command | |
| 0x08 | Class Code | | | Revision ID |
| 0x0C | BIST | Header Type | PCI Latency Timer | Cache Line Size |

| | | | | |
|---|---|---|---|---|
| 0x10 | PCI Base Address 0<br>(Memory Access to PLX Registers) | | | |
| 0x14 | PCI Base Address 1<br>(I/O Access to PLX Registers) | | | |
| 0x18 | PCI Base Address 2<br>(Memory Access to DSP SRAM and card registers) | | | |
| 0x1C | PCI Base Address 3<br>(Not Used for this card) | | | |
| 0x20 | Unused PCI Base Address 4 | | | |
| 0x24 | Unused PCI Base Address 5 | | | |
| 0x28 | Cardbus CIS Pointer (Not Supported) | | | |
| 0x2C | Subsystem ID | | Subsystem Vendor ID | |
| 0x30 | PCI Base Address for Expansion ROM | | | |
| 0x34 | Reserved | | | |
| 0x38 | Reserved | | | |
| 0x3C | Max Latency | Min Grant | Interrupt Pin | Interrupt Line |
| 0x80 | RT Jumper status- READ ONLY | | | |
| 0x82 | Int. Status- READ ONLY | | | |

**Table 1.0 : PCI Configuration Space**

The card presents the following initial configuration values to the PCI system, based on the values stored in the NVRAM device read by the PLX PCI9080 interface chip.

| Register | Value (Meaning) |
|---|---|
| Vendor ID | 0x13C5 (ALPHI Technology) |
| Device ID | 0x0409 (PCI-BCRTM) |
| Revision ID | 0x00 |
| Class Code | 0xff0000 (Device does not fit into defined class codes) |
| Interrupt Line | 0xff |
| Interrupt Pin | A |
| Multifunction Device | No |
| Build In Self Test | No |
| Latency Timer | 0x00 |
| Minimum Grant | 0x00 |
| Maximum Latency | 0x00 |
| Base Address 0 Size | 0x256 Bytes Allocated |
| Base Address 1 Size | 0x256 Bytes Allocated |
| Base Address 2 Size | 0x256 Bytes Allocated |
| Base Address 3 Size | 0x256 KBytes Allocated |
| Expansion ROM Size | None |

**Table 1.1: PCI-BCRTM Configuration Register Default Values**

**PCI Base Address Regions**

| HOST Address | WIDTH USED | Description | TYPE |
|---|---|---|---|
| BAR0 | 64 BYTES<br>0X0h– 3Fh | PLX Operation Registers | MEM |
| BAR1 | 256 BYTES | NOT USED | I/O |
| BAR2 | 256 BYTES<br>0X0h– 7Fh | Ch 1 BCRTM I/O Space<br>16 bit wide | MEM |
| BAR3 | 128 KBYTE<br>0X0h– 1FFFFh | Ch 1 BCRTM DUAL PORTED SRAM<br>16 bit wide | MEM |

**Table 2 PCI-BCRTM**

**INTERRUPTS:**

The BCRTM uses two (2) interrupt lines. These interrupts are Ored to the INTA pin on the PCI bus.

The source of each interrupt is listed below:

| INTERRUPT name | Description |
|---|---|
| Standard Interrupt Level. (STDINTL) | This is a level interrupt. It is asserted when one or more events enabled in either the Standard Interrupt Enable Register, RT Descriptor, or BC Command Block occur. Resetting the Standard Interrupt bit in the High-Priority Interrupt Status/Reset Register clears the interrupt. |
| High Priority Interrupt. (HPINT) | The High-Priority Interrupt level is asserted upon occurrence of events enabled in the High Priority Interrupt Enable Register. The corresponding bit(s) in the High- |

| | |
|---|---|
| | Priority Interrupt Status/Reset Register reset HPINT. |

**Table 3**

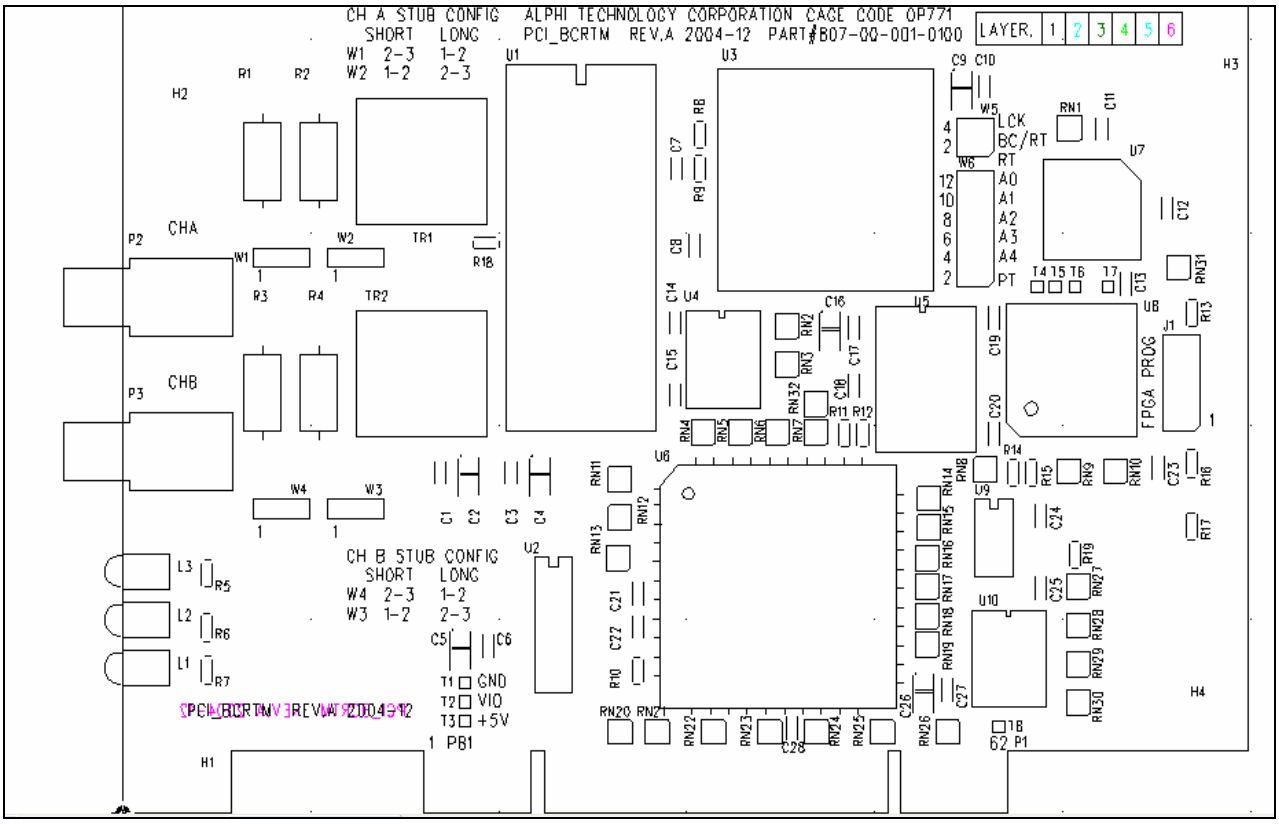


**Figure 2: JUMPER LOCATION DIAGRAM**

| JUMPER | FACTORY SETTING | DESCRIPTION |
|---|---|---|
| W1 | 2-3 | Long Stub/Short Stub Output channel 1A - ( Short Stub ) |
| W2 | 1-2 | Long Stub/Short Stub Output channel 1A + ( Short Stub ) |
| W3 | 1-2 | Long Stub/Short Stub Output channel 1B + ( Short Stub ) |
| W4 | 2-3 | Long Stub/Short Stub Output channel 1B - ( Short Stub ) |
| W5 | None | BCRTL and LOCK for BCRTM |
| W6 | None | 1553 bus RT address and parity selection |
| J1 | None | Altera programming plug |

**Table 4**

**W5 BCRTL and LOCK for BCRTM:**

| Signal | Jumper set | Description |
|---|---|---|
| BC/RT | 1-2 | **ON**: RT Enable **OFF**: BC Enable |
| LOCK | 3-4 | **ON**: LOCK Disable **OFF**: LOCK Enable |

**W6 RT Address Selection:**

| Signal | Jumper set | Description |
|---|---|---|
| RTPT | 1-2 | RT Address Parity |
| RTA4 | 3-4 | RT Address Bit 4 |
| RTA3 | 5-6 | RT Address Bit 3 |
| RTA2 | 7-8 | RT Address Bit 2 |
| RTA1 | 9-10 | RT Address Bit 1 |
| RTA0 | 11-12 | RT Address Bit 0 |

**Table 5: RT address and parity selection**

**Local Registers**

W6 RT Jumper Status Register $80

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| LOCK | BCRTMSEL | RTPT | RTA4 | RTA3 | RTA2 | RTA1 | RTA0 |

W8 BCRTM INT status lines $82

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| x | x | x | | VCC | AEN | HPINT | STD INTL |

**Master resetBCRTM $8A**

A write at this address will generate a 800nS reset pulse. It has the same effect as the PLX RESET 0 line.

**BCRTM Registers**

**#0 BC/RT CONTROL REGISTER**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| UNUSED | RT31 | SA31 | BCTO | EXTOVR | BC/RT | RTYALTB | BUSBEN |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CHNSELBUSAEN | RTYCNY | RTYCNT | RTYBCME | RTYTO | RTYME | RTYBSY | STN |

**#1 BC/RT STATUS REGISTER**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| MEMWIN | RTACT | DYNBUS | RTFLAG | SRQ | BUSY | BIT | RESET |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| BC/RT | BUS A/B | SSFAIL | UNUSED | UNUSED | UNUSED | UNUSED | CMBKPG |

**#2 (BC) CURRENT COMMAND BLOCK REGISTER**

**(RT) RT DESCRIPTOR SPACE ADDRESS REGISTER**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| A15 | A14 | A13 | A12 | A11 | A10 | A9 | A8 |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |

**#3 POLLING COMPARE REGISTER**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| X | X | X | X | X | MSGERR | INST | SRQ |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SWBT12 | SWBT13 | SWBT14 | BRDCST | BUSY | SS FLAG | DBC | TF |

### #4 BIT WORD REGISTER

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| CHNBFAIL | CHNAFAIL | D13 | D12 | D11 | D10 | D9 | D8 |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

### #5 CURRENT COMMAND REISTER

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

### #6 INTERRUPT LOG LIST POINTER REGISTER

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| A15 | A14 | A13 | A12 | A11 | A10 | A9 | A8 |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |

### #7 BCRTM HIGH PRIORITY INTERRUPT ENABLE REGISTER

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| UNUSED | UNUSED | UNUSED | UNUSED | UNUSED | UNUSED | UNUSED | DATOVR |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ILLCMD | DYNBUS | SSFAIL | ENDBIT | BITFAIL | EOL | MSGERR | STDINT |

### #8 BCRTM HIGH PRIORITY INTERRUPT STATUS RESET REGISTER

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| UNUSED | UNUSED | UNUSED | UNUSED | UNUSED | UNUSED | UNUSED | DATOVR |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| ILLCMD | DYNBUS | SSFAIL | ENDBIT | BITFAIL | EOL | MSGERR | STDINT |

### #9 STANDARD INTERRUPT ENABLE REGISTER

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| UNUSED | UNUSED | UNUSED | UNUSED | UNUSED | UNUSED | UNUSED | UNUSED |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| UNUSED | UNUSED | ILLBCMD | ILLCMD | POLMTCH | RTYFAIL | MSGERR | CMDBLK |

### #10 REMOTE TERMINAL ADDRESS REGISTER

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| INSTR | BUSY2 | SS FLAG | DBC | RT FLAG | SRQ | BUSY 1 | BC/RT |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| LOCK | PARERR | RTAPAR | RTA4 | RTA3 | RTA2 | RTA1 | RTA0 |

### #11 BUILT IN TEST START REGISTER

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | X |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | X |

### #12 PROGRAMED RESET REGISTER

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | X |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | X |

### #13 REMOTER TERMINAL RESET REGISTER

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | X |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | X |

### #14 BUS MONITOR CONTROL REGISTER

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| BMS | MAT | MDT | X | X | X | X | X |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | X |

### #15 RESERVED

### #16 MONITOR SELECTED REMOTE TERMINAL ADDRESS

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| TA15 | TA14 | TA13 | TA12 | TA11 | TA10 | TA9 | TA8 |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| TA7 | TA6 | TA5 | TA4 | TA3 | TA2 | TA1 | TA0 |

### #17 MONITOR SELECTED REMOTE TERMINAL ADDRESS

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|
| TA31 | TA30 | TA29 | TA28 | TA27 | TA26 | TA25 | TA24 |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| TA23 | TA22 | TA21 | TA20 | TA19 | TA18 | TA17 | TA16 |

## CONNECTION HARDWARE FOR 1553 BUS

The following hardware is available from:

**Trompeter Electronics, Inc.**
**31186 La Baya Drive**
**P.O. Box 5069**
**Westlake Village, CA**
**91362-4047**

**Phone: (818) 707-2020**
**Fax : (818) 706-1040**

**PL155-29** Mating plug for P2 and P3 (1553 Channels A and B)
**TWC-78-1** Cable meets 1553B requirements, 78 Ohm impedance

 

**TNGM1-1-78** 78 Ohm terminator
**BN153** Tee connector

ALPHI Technology stocks the above connectors and other cabling options. We can also build complete cable assemblies to meet your requirements.

 