

1. GENERAL DESCRIPTION

1.1 INTRODUCTION

The **IP-AD48-16** is a 16 bit single width IP module designed for high speed burst A/D data acquisition in 16 bits. The primary features of the **IP-AD48-16** are:

- Forty eight channels of simultaneous 16 bit A/D acquisition, operating at a maximum rate of 250 kHz.
- Inputs are software programmable +/- 10V (default) or +/-5v single ended.
- Up to 64K of samples stored divided among active A/D converters in onboard FIFO memory.
- Sampling clock selected from one of the following sources: Internal divider (TCLK0), IPSTROBE, external clock and Host.
- Trigger event selected from one of the following sources: Write to IP register, IPSTROBE, and external trigger.
- Burst acquisition or continuous streaming acquisition is also possible.
- IP bus operates at 32 MHz.

1.2 IDSPACE

Up to 32 bytes of registered data provide information about the module to the User. Word address access is used. The lower byte contains data related to the type of module, revision, etc...

ID space address	Description	Value
\$00	ASCII "I"	\$49
\$02	ASCII "P"	\$50
\$04	ASCII "A"	\$41
\$06	ASCII "H"	\$48
\$08	Manufacturer identification	\$11
\$0A	Module type	\$24
\$0C	Revision module	\$0A
\$0E	Reserved	\$00
\$10	Driver ID, low byte	\$00
\$12	Driver ID, high byte	\$00
\$14	Number of bytes used	\$0A
\$16	CRC	\$00
\$18-\$3E	User space	\$00

Table 1-1 IDSEL0 SPACE byte content

1.3 FUNCTIONAL DESCRIPTION

The IP_AD48_16 is designed around the A/D converter AD7656 from Analog Devices. It provide six independent ADC channels of simultaneous sampling A/D converter 16 bits with :

- True bipolar analog inputs with pin or software selectable range +/-10v or +/-5v
- 250 KSPS throughput rate.

The IP_AD48_16 is populated with eight(8) AD7656 .

Each input is has on the front a fast buffer amplifier LT1468/69.

A 64k X16 FIFO allow Burst mode or continuous sampling.

A data flow block diagram of the **IP-AD48-16** is presented in Figure 1-1.

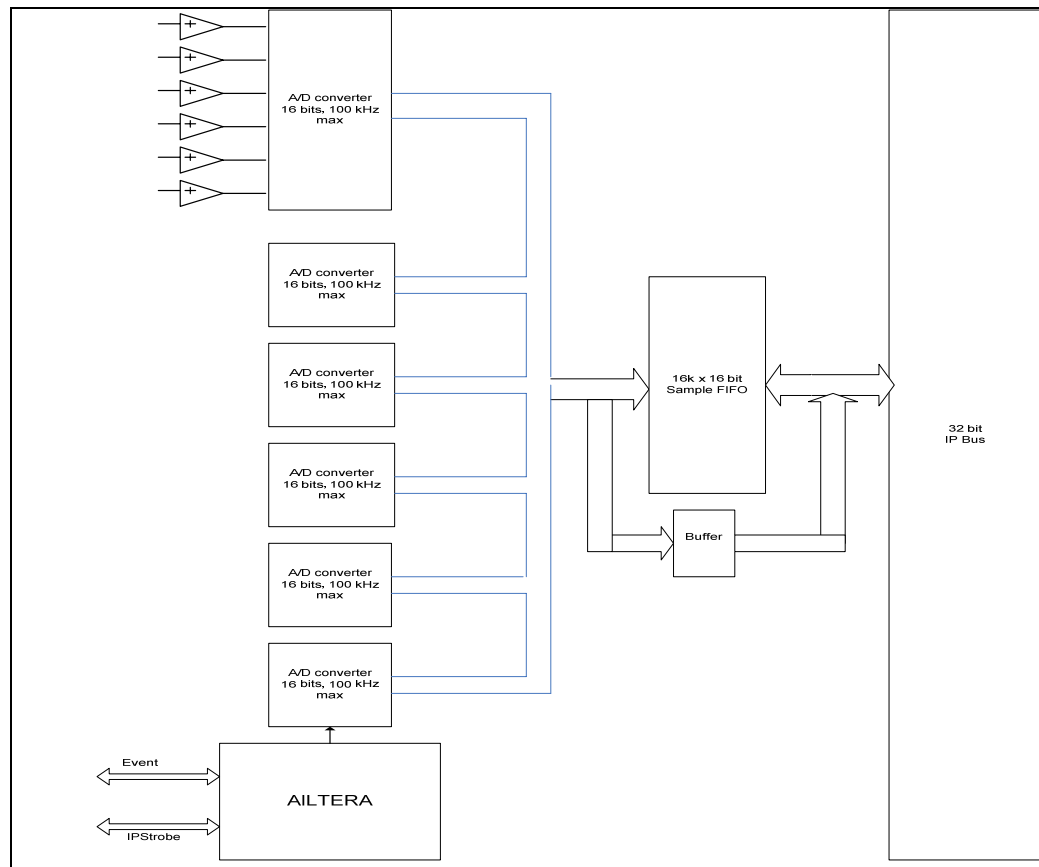


Figure 1.1: Data Flow Block Diagram

1.4 SOFTWARE SUPPORT

The **IP-AD48-16** board support package provide sample examples for :

- *Windows NT*
- *Windows 2000*
- *Labview*

2. THEORY OF OPERATION

2.1 ANALOG INPUTS

Forty eight Single Ended analog inputs are provided. By default, the inputs are high impedance +/- 10 volt .

There are eight A/D converters. The A/D converters operate continuously at the selected sampling rate.

2.1.1 DIRECT MODE

Direct read of the data from a A/D7656 is achieved by making six (6) consecutive read at the same base address of the selected A/D converter. The FIFO is by-passed. It is not storing any data at the end of conversion.

2.1.2 FIFO MODE

At the end of conversion a state machine will read the data of each selected A/D 7656 and store then into the FIFO. If all the A/D are selected 48 data will be written at each conversion. Up to 64K words are shared between the selected A/D 7656.

Each A/D can be disable providing more space for the active one.

FIFO pointers are used to monitor, stop or “throttle” the acquisition and inform the user by means of status or interrupt the progress of the acquired data.

3. INTERFACE TO THE IP CARRIER

The IP carrier controls this IP via a set of registers in IP IOSPACE. There is no memory on this IP.

3.1 REGISTERS

The I/O map access is displayed in 8 bit wide accesses except for the FIFO which is 16 bits wide, so all registers are at EVEN addresses . If using word access convert I/O map to even addresses.

IP-AD48-16 Address	Read/Write	Byte Access	Wait State @ 32MHz	Register
0x00	R/W	Lower	1	Internal Clock Divisor 0
0x02	R/W	Lower	1	Internal Clock Divisor 1
0x04	R/W	Lower	1	Internal Clock Divisor 2
0x06	R/W	Lower	1	A/D Mask
0x08				
0x0A	R/W	Lower	1	Input range selection
0x0C	W	Lower	1	Stop Acquisition
0x0E	R/W	Lower	1	Acquisition Control Register
0x10	R/W	Lower	1	Source Intreq1
0x12	W	Lower	1	Clear Intreq0 latch
0x14	R/W	Lower	1	Control register
0x16	R/W	Lower	1	FIFO Status register
0x18	W	Lower	1	FIFO reset
0x1A	R/W	Word	1	FIFO DATA/POINTER
0xxx	R/W	Lower	1	Source for Dmreq#0 / Dma_end#
0x26	WS	Lower	1	Host start acquisition
0x28	R/W	Lower	1	Interrupt Vector register
0x2E	R/W	Lower	1	Hardware/software range selection
0x40	R	Word	2	A/D DATA #1 (Input 1-6)
0x42	R	Word	2	A/D DATA #2 (Input 7-12)
0x44	R	Word	2	A/D DATA #3 (Input 13-18)
0x46	R	Word	2	A/D DATA #4 (Input 19-24)
0x48	R	Word	2	A/D DATA #5 (Input 25-30)
0x4A	R	Word	2	A/D DATA #6 (Input 31-36)
0x4C	R	Word	2	A/D DATA #7 (Input 37-42)
0x4E	R	Word	2	A/D DATA #8 (Input 43-48)
0x50	R/W	Lower B	1	A/D stand-by mode
0x60	W	Upper		Write A/D reg. address

Table 3.1: IO Registers

3.1.1 INTERNAL CLOCK DIVISOR

Base I/O + \$[4,2,0]

These three 8 bit registers combine to form one 24 bit register which serves as a divisor on the IP clock when internal sampling clock is selected. Note this IP only runs at 32 MHz.

$$SamplingRate = \frac{IPClockFrequency}{N + 1}$$

EXAMPLE

- At 32 MHz to set the Internal Clock at 200uS do the following.
- \$00 - Internal clock, write \$0 (any data within the appropriate range)
- \$02 - Internal clock, write \$0
- \$04 - Internal clock, write \$0

3.1.2 A/D MASK

Base I/O + \$06

Upon reset all the eight A/D converter are active. User can disable one or more A/D by setting the correspondent associated bit to “1”.It allow to use only the necessary A/D. Also the A/D can be set in “stand-by” for reduce power. The active A/D converter can share more room into the FIFO.

BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 00
AD #8	AD #7	AD #6	AD #5	AD #4	AD #3	AD #2	AD #1

3.1.3 TRIGGER EVENT

Base I/O + \$08

A write to this register will cause the trigger to occur, regardless of the setting in the **Acquisition Control Register**.

3.1.4 INPUT RANGE SELECTION

Base I/O + \$0A

Upon reset all the eight A/D converter have an input range of +/-10V. User can select each A/D converter to have all it’s 6 channels to be +/-5V input by setting the correspondent bit to a “1”.

The selection works concurrently with the Hardware/Software register (Base I/O + \$2E).

BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 00
AD #8	AD #7	AD #6	AD #5	AD #4	AD #3	AD #2	AD #1

3.1.5 STOP ACQUISITION

Base I/O + \$0C

A write to this register will stop the data to be written into the FIFO. Can be use with slow sampling .

3.1.6 ACQUISITION CONTROL REGISTER

Base I/O + \$0E

This register is use to program multiples parameters as clock source , FIFO pointers utilization.

Bits 7-6	Bits 5-4	Bits 3-2	Bits 1-0
Sampling Clock Source	Not used	End Acquisition Source	Not used

End Acquisition Source

This two bit selects witch FIFO pointer will end DATA to be written into the FIFO.

By default FF is the selected pointer.

End Acquisition Source	Meaning
xx xx 00 xx	FIFO FF Flag
xx xx 01 xx	FIFO PAF Flag

Sampling Clock Source

These two bits are use to select the signal use as for the A/D sampling clock.

Sampling Clock Source	Meaning
00 xx xx xx	Internal Sampling Clock (IP Clock divided by Divisor) TCLK0
01 xx xx xx	IPSTROBE signal
10 xx xx xx	External Clock -Front panel connector
11 xx xx xx	Host strobe conversion start pulse. Base I/O + \$28

3.1.7 CONTROL REGISTER

Base I/O + \$14

This register is used to:

- Select the source to initiate an acquisition.
- Control the reset of the INTREQ#1
- Reset A/D converter registers

BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 00
INT1 Reset RDFIFO	Event Enable	Master	INT1 Reset EF	Partial FIFO reset	A/D Direct	Reset A/D	CONV Source

CONV SOURCE

This bit, when high (1), enables the Event input signal (from the front panel) to be the source to start storage of acquired data into the FIFO a host write at Start acquisition register (Base I/O + \$26) is used.

This suppose that the sample clock is already running. The A/D's are converting data but the result are not stored.

Pulse must be 64 nS minimum.

Reset A/D

When pulsed to "1" then "0" reset the internal A/D registers. "0" upon reset.

A/D DIRECT

This bit, when high (1), DISABLE THE STATE MACHINE , NOT ALLOWING ANY A/D DATA TO BE WRITTEN INTO THE FIFO. Reset by default.

Partial FIFO pointer reset

This bit when pulsed to "1" then "0" reset the two FIFO pointers (PAE and PAF) . The programmed values are maintained.

INT1 RESET EF

This bit, when high (1) reset the INTREQ1# when the FIFO status line EF goes low.

MASTER

This bit, when high (1), will make the IP module generating the sample clock out to the IPSTROBE pin and eventually to the EVENT line. Use for multiple module synchronization. Carrier must be able to connect the IPSTROBE of more than one module together.

It will appear on IP-STROBE (P1 pin 46) as an output.

EVENT ENABLE

This bit, when high (1) enables the external event signal to be an output, the strobe output signal been the source. Care must be made not to have conflicted signals.

INT 1 RESET RDFIFO

This bit, when high (1) reset the INTREQ1# when the FIFO status line EF goes low.

This bit, when high (1) reset the INTREQ1# with the first read to the FIFO DATA address.

3.1.8 FIFO STATUS / CONTROL REGISTER

Base I/O + \$16

This register allows for querying the current state of the FIFO flags .

BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 00
FF	PAF	PAE	EF	HF	GND	BUSYIN	FIFO REG
R	R	R	R				R/W

FF

This bit, when low (0), indicates that there are 64536 samples stored in the FIFO DATA_OUT. It is usually an indication that the acquisition is completed.

PAF

This bit, when low (0), indicates that there is a programmable number of samples stored in the FIFO DATA_OUT. It has no meaning for the acquisition modes discussed in this manual.

PAE

This bit, when low (0), indicates that there is less than a programmable number of samples stored in the FIFO DATA_OUT. When this bit goes high, it indicates that the pre-trigger sampling requirement has been met, and that it is now possible to trigger the acquisition. In continuous modes, this bit being high indicates that there are N samples ready to be read, where N-1 is the number programmed in the FIFO.

EF

This bit, when low (0), indicates that there are no samples stored in the FIFO DATA_OUT.

HF

This bit, when low (0), indicates that there are 32 268 samples stored in the FIFO

BUSYIN

Status of the busy line of all the A/D. When high the A/D converter are converting(~3 μ S) then goes low when conversion is finished.

FIFO REG

Read/write

This bit, when cleared to low (0), allow direct data write to the **FIFO DATA_OUT** address .to be placed into the FIFO for testing purposes.

Subsequent reads of **FIFO DATA_OUT** address allow testing of the FIFO behavior When the bit is set high (1), writes to and reads of the FIFO will access the FIFO programming registers.

3.1.9 FIFO RESET

Base I/O + \$18

A write to this location will generate a master reset to the FIFO.

FIFO pointers (PAE and PAF) will be set to \$7F or \$ xxx depending of the FIFO REG bit. See the FIFO data sheet for more information.

3.1.10 FIFO DATA_OUT

Base I/O + \$1A

If the **FIFO REG** bit is clear (0), and then a read of this location will respond with the oldest data samples in the FIFO. If the **FIFO REG** bit is set (1), then a read of this location will read the internal configuration registers of the FIFO (PAE and PAF).

Data is stored as 16 bit Words in 2's complement format. Only enabled channels will be found in the FIFO.

FIFO pointers are accessed in a circular mode. First access is for PAE then next access is PAF, same for a write.

3.1.11 HOST START ACQUISITION

Base I/O + \$1C

A host write to this register will start an acquisition immediately if the signal is selected as source of sample clock.

If another source is selected (ex: TCLK0) a host write will enable the result of the conversion that is already running to be store into the FIFO.

3.1.12 A/D DATA ADDRESS

Base I/O + (\$40 - \$4E)

Direct access to the A/D conversion can be made if the State machine is disable .

The state machine by default will store A/D data into the FIFO at the end of conversion

Base I/O + \$28. To read the data of the selected A/D, six consecutive read need to be made at the same address.

State machine is disable when bit #2 of the CONTROL register is set to “1”.

A/D #	ADDRESS BASE I/O +
1	\$40
2	\$42
3	\$44
4	\$46
5	\$48
6	\$4A
7	\$4C
8	\$4E

3.1.13 A/D STAND-BY

Base I/O + \$50

Upon reset all the eight A/D converters are in low power “stand-by” mode . User must enable one or more A/D by setting the correspondent associated bit to “1”.

BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 00
AD #8	AD #7	AD #6	AD #5	AD #4	AD #3	AD #2	AD #1

4. PROGRAMMATION

4.1 DIRECT MODE

Direct read of the data from a A/D7656 is achieved by making six (6) consecutive read at the same base address of the selected A/D converter. The FIFO is by-passed. It is not storing any data at the end of conversion.

Setting up and operating this type of acquisition is easy.

- Select the sample clock source by programming the **Acquisition Control Register** bit [7..6]. \$C0 for Host start register or \$00 for TCLK0 (internal timer)

- Program internal timer if it is the sample clock source. Sampling clock will have to be carefully selected in such a way that the selected A/D converter are read before the next conversion
- Disable the FIFO mode by setting bit #2 of the **Control Register** to “1”.
- Enable the desired A/D converter.
- Start the conversion using **Host Start Acquisition** pulse .
- Monitor the BUSYIN signal bit # 1 FIFO Status register.
- Read the A/D converter data. Each read at one A/D data location provide the first channel then the second, etc....

4.2 FIFO MODE

Setting up and operating this type of acquisition is easy.

- Select the sample clock source by programming the **Acquisition Control Register** bit [7..6]. \$C0 for Host start register or \$00 for TCLK0 (internal timer)
- Program internal timer if it is the sample clock source. Sampling clock will have to be carefully selected in such a way that the selected A/D converter are read before the next conversion
- Enable the desired A/D's converter.
- Program the PAF pointer register if you desire a number of samples using n A/D converter to stop the data written into the FIFO source by programming the **Acquisition Control Register** bit [1..0].
- Program PAF to be the source of the interrupt INTreq1# if using interrupt or monitor the FIFO status/control register for PAF.
- Start the conversion using **Host Start Acquisition** pulse .
- Monitor the PAF signal bit # 6 FIFO Status/Control register or wait for interrupt.
- Read the FIFO DATA OUT .

4.3 INTERRUPTS PROGRAMMATION

4.3.1 INTREQ0

Source

Sole source for Intreq#0 is the PAE FIFO pointer. It can be use to inform the user that acquisition has started in case of external event trigger.

Reset

A write at address Base I/O + \$12 will reset the Interrupt #0.

4.3.2 INTREQ1

Source

Base I/O + \$10

This register selects the signal source that will generate an interrupt Intreq1.

BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 00
Not used	Not used	Not used	EF	PAE	HF	PAF	FF

FF

This bit, when low (0), indicates that there are 65536 samples stored in the FIFO DATA_OUT.

By default it will stop data to be written into the FIFO.

PAF

This bit, when low (0), indicates that there is a programmable number of samples stored in the FIFO.

HF

This bit, when low (0), indicates that there is a 65536/2 samples number of samples stored in the FIFO.

PAE

This bit, when low (0), indicates that there is less than a programmable number of samples stored in the FIFO DATA_OUT In continuous modes, this bit being high indicates that there are N samples ready to be read, where N-1 is the number programmed in the FIFO.

EF

This bit, when low (0), indicates that there are no samples stored in the FIFO DATA_OUT.

Reset

The interrupt Intreq1 is latched. The latch is reset by:

- a read of the FIFO Control/Status register (Base I/O + \$16)
- EF signal active with bit #4 of control register set to "1">
- Read FIFO DATA OUT with bit #7 of control register set to "1".

Interrupt vector register

Base I/O + \$28

The AD48-16 module can provide a vector registers to the lower data byte upon an INTESELA# cycle.

4.3.3 DMA_REQ0

Source

Base I/O + \$10

This register selects the signal source that will generate a DMA request #0 and the signal source that will generate a DMA_END# signal

BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 00
PAE	HF	PAF	EF	PAE	HF	PAF	FF

FF

This bit, when low (0), indicates that there are 65536 samples stored in the FIFO DATA_OUT.

By default it will stop data to be written into the FIFO.

PAF

This bit, when low (0), indicates that there is a programmable number of samples stored in the FIFO.

HF

This bit, when low (0), indicates that there is a 65536/2 samples number of samples stored in the FIFO.

PAE

This bit, when low (0), indicates that there is less than a programmable number of samples stored in the FIFO DATA_OUT In continuous modes, this bit being high

indicates that there are N samples ready to be read, where N-1 is the number programmed in the FIFO.

EF

This bit, when low (0), indicates that there are no samples stored in the FIFO DATA_OUT.

4.4 A/D7856 REGISTERS PROGRAMMATION.

Base I/O + \$0A

4.4.1 DEFAULT MODE

By default upon reset the H/S SEL line are low. Hardware selection of the Input range is active and by default the Range signal line are "0" defining a +/-10V input.

The internal reference is selected because H/S SEL is low and the WR#/REFen_dis pin is HIGH.

On the AD48-16 the CONVST A, CONVST B, and CONVST C pins are connected together.

4.5 INPUT RANGE PROGRAMMATION

(Base I/O + \$60)

The H /S SEL pin determines the source of the combination of ADCs that are to be simultaneously sampled. When the H /S SEL pin is logic low, the combination of channels to be simultaneously sampled is determined by the CONVST A, CONVST B, and CONVST C pins.

Channels selected for simultaneous sampling is determined by the contents of the Control Register DB15 to Control Register DB13. In this mode, a write to the control register is necessary.

The control register is an 8-bit write-only register. Data is written to this register using the CS and WR pins and the DB[15:8] data pins .To select an ADC pair to be simultaneously sampled, set the corresponding data line high during the write operation (table 2.1)

The AD7656 control register allows individual ranges to be programmed on each ADC pair. DB12 to DB10 in the control register are used to program the range on each ADC pair.

The CONVST A signal is used to initiate a simultaneous conversion on the combination of channels selected via the control register. CONVSTA, CONVST B and CONVST C signals are tied together.

During the write operation, Data Bus Bit DB15 to Bit DB8 is bidirectional and become inputs to the control register when RD is logic high and CS and WR are logic low. The logic state on DB15 through DB8 is latched into the control register when WR goes logic high.

Therefore, in software selection CONVSTA, CONVSTB and CONVSTC should be low (this is the way that we have; they are all connected to GND). Also, the H_SEL pin of the 8-bits register should be set to 1.

After a reset occurs on the AD7656, the control register contains all zeros.

BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 09	BIT 08
VC	VB	VA	RNGC	RNGB	RNGA	REFEN	REFBUF

To program the first A/D, BIT[0] of the register should be set to 1 at BASE + \$2E ,then bits D[15..8] of A/D register should be set to their corresponding values as 16 bits at address(Base I/O + \$60) .

Note: The AD48-16 uses only the internal reference. In software mode the Internal Reference need to be enabled by setting bit # 9 to “1”.

Bit	Mnemonic	Comment
DB15	VC	This bit is used to select Analog Inputs V5 and V6 for the next conversion. When this bit = 1, V5 and V6 are simultaneously converted on the next CONVST A rising edge.
DB14	VB	This bit is used to select Analog Inputs V3 and V4 for the next conversion. When this bit = 1, V3 and V4 are simultaneously converted on the next CONVST A rising edge.
DB13	VA	This bit is used to select Analog Inputs V1 and V2 for the next conversion. When this bit = 1, V1 and V2 are simultaneously converted on the next CONVST A rising edge.
DB12	RNGC	This bit is used to select the analog input range for Analog Inputs V5 and V6. When this bit = 1, the $\pm 2 \times VREF$ mode is selected for the next conversion. When this bit = 0, the $\pm 4 \times VREF$ mode is selected for the next conversion.
DB11	RNGB	This bit is used to select the analog input range for Analog Inputs V3 and V4. When this bit = 1, the $\pm 2 \times VREF$ mode is selected for the next conversion. When this bit = 0, the $\pm 4 \times VREF$ mode is selected for the next conversion.
DB10	RNGA	This bit is used to select the analog input range for Analog Inputs V1 and V2. When this bit = 1, the $\pm 2 \times VREF$ mode is selected for the next conversion. When this bit = 0, the $\pm 4 \times VREF$ mode is selected for the next conversion.
DB9	REFEN	This bit is used to select the internal reference or an external reference. When this bit = 0, the external reference mode is selected. When this bit = 1, the internal reference is selected.
DB8	REFBUF	This bit is used to select between using the internal reference buffers and choosing to by pass these reference buffers. When this bit is 0, the internal reference buffers are enabled and decoupling is required on the REFCAP. When this bit is 1, the internal reference buffers are disabled and a buffered reference should be applied to the REFCAP pins.

Table 2.1: Control Register Bit Function Descriptions

5. HARDWARE DETAILS

5.1 JUMPERS

5.2 CONNECTORS

The connector placement is depicted below.

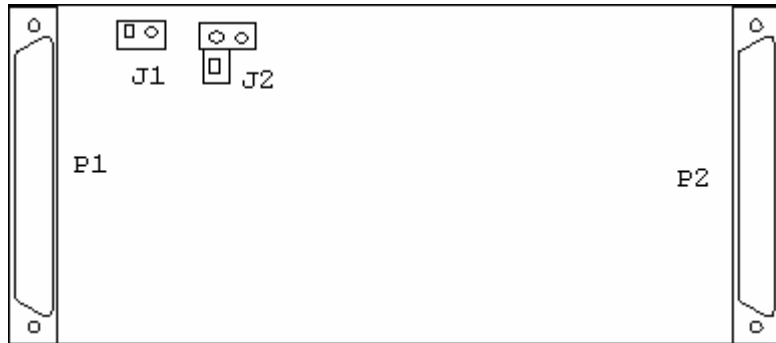


Figure 5.1: Connector Locations

4.3.1 CONNECTOR DESCRIPTIONS

IP External I/O Connector

JP2, a 49 pin subminiature connector used as External trigger when the (2-3) connection is made and used as Input CHAN 48 when connection (1-2) is made. At default, the (1-2) connection is made to get CHAN 48.

JP1 is inserted for factory use.

The signals are routed as follows.

Pin	Connection	Pin	Connection
1	IN_1	26	IN_2
2	IN_3	27	IN_4
3	IN_5	28	IN_6
4	IN_7	29	IN_8
5	IN_9	30	IN_10
6	IN_11	31	IN_12
7	IN_13	32	IN_14
8	IN_15	33	IN_16
9	IN_17	34	IN_18
10	IN_19	35	IN_20
11	IN_21	36	IN_22
12	IN_23	37	IN_24
13	IN_25	38	IN_26
14	IN_27	39	IN_28
15	IN_29	40	IN_30
16	IN_31	41	IN_32
17	IN_33	42	IN_34
18	IN_35	43	IN_36
19	IN_37	44	IN_38
20	IN_39	45	IN_40
21	IN_41	46	IN_42
22	IN_43	47	IN_44
23	IN_45	48	IN_46
24	IN_47	49	IN_48
25	GND	50	GND
1	IN_1	26	IN_2
2	IN_3	27	IN_4

Table 4.1: IP external I/O connector

The following figure shows the timing graph when using event as an Ext_CLK directly:

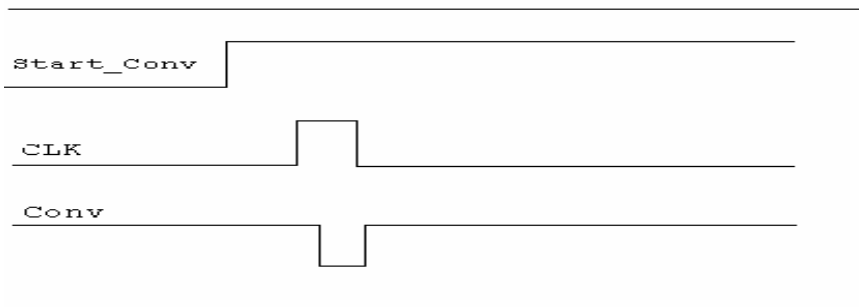


Figure 7.1: Event used as Ext_CLK

The following figure represents the timing waveform when event is connected as Ext_event.

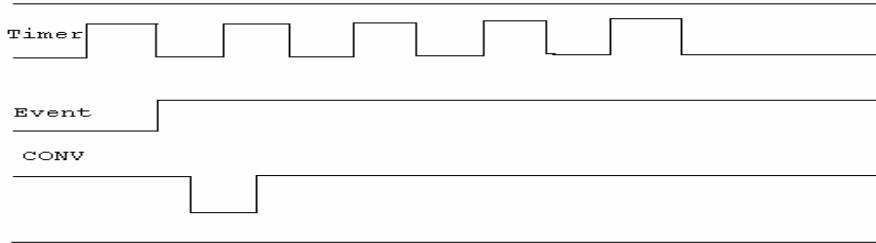


Figure 7.2: Event used as Ext_event

