IP-1553B
MIL-STD-1553

IndustryPack Module

REFERENCE MANUAL

693-13-000-4000

Revision 1.3
March 2001

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GENERAL DESCRIPTION

INTRODUCTION

The IP-SUMMIT module provides Bus Controller (BC), Remote Terminal (RT) and Bus Monitor (BM) dual-redundant operations on the MIL-STD-1553 bus. The IP form factor provide easy installation.

- UTMC Summit RISC based processor unit
- 64K x 16 bit dual ported SRAM
- One EEPROM (32 bytes) for identification
- Supports Bus Controller, Remote Terminal and Bus Monitor mode
- RT address and operational modes are program or jumper selectable
- 1553 bus long or short stub jumper option on transition module

FUNCTIONAL DESCRIPTION

A functional block diagram of the IP module is depicted below in Figure 1. The IP-SUMMIT is designed around the SUMMIT that is used to manage the 1553 BUS.

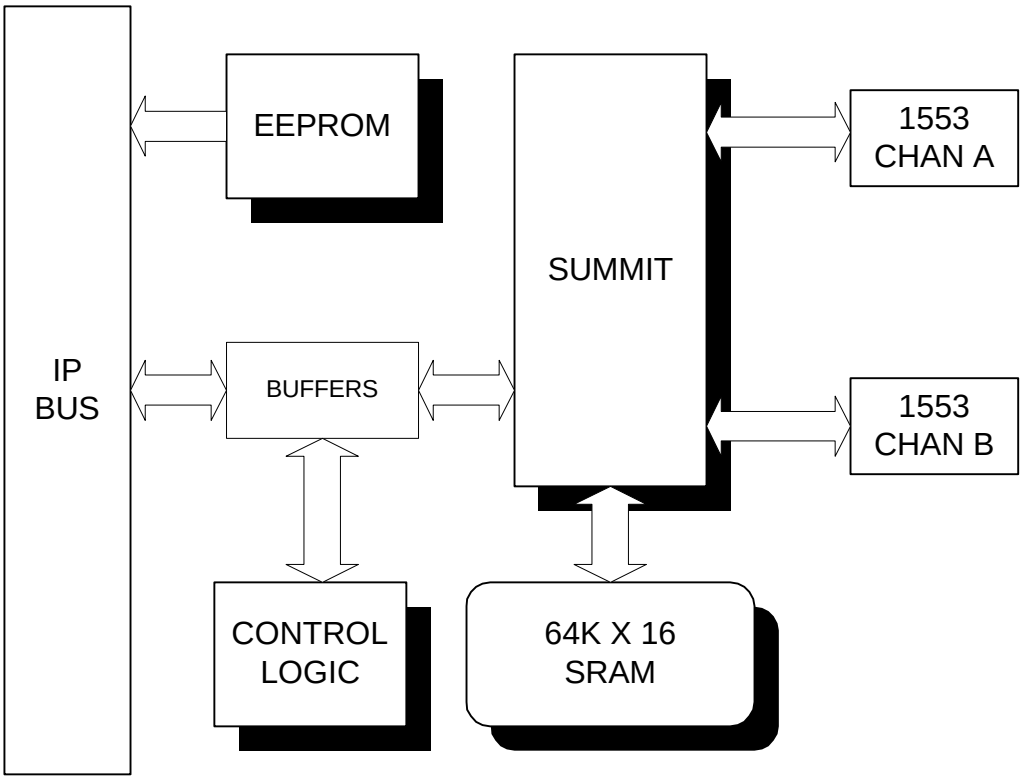

Figure 1

REFERENCE MATERIALS LIST

The reader should refer to the “SUMMIT” 1996 product handbook, from UTMC, that provides detailed descriptions about the SUMMIT registers.

UTMC
1575 Garden of the Gods Road
Colorado Springs, Colorado
80907-3486 USA

Marketing Department :
719-594-8166 or 800-722-1575

Technical Information :
719-594-8252

Literature Requests :
800-645-UTMC

WWW Home Page :
http://www.utmc.com

The reader is also referred to the IP Modules Draft Standard:

VITA standards Organization
10229 North Scottsdale Road, Suite B
Scottsdale AZ 85253
Voice : 602-951-8866
Fax : 602-951-0720

THEORY OF OPERATION

INTERNAL ORGANIZATION

The IP-SUMMIT facilitates host access to the :

- SUMMIT Registers
- Dual Port SRAM
- Identification EPROM
- Status register
- Interrupt Vector Register (IVR)

SUMMIT REGISTERS

REMOTE TERMINAL REGISTERS

Register Number	Name	Register Offset
0	Control Register	$00
1	Operational Status Register	$02
2	Current Command Register	$04
3	Interrupt Mask Register	$06
4	Pending Interrupt Register	$08
5	Interrupt Log List Pointer Register	$0A
6	BIT Word Register	$0C
7	Time-Tag Register	$0E
8	Remote Terminal Descriptor Pointer Register	$10
9	Status Word Bits Register	$12
10-15	Not Applicable	$14-$1E
16-31	Illegalization Registers	$20- $3E

Table 1

BUS CONTROLLER REGISTERS

Register Number	Name	Register Offset
0	Control Register	$00
1	Operational Status Register	$02
2	Current Command Block Register	$04
3	Interrupt Mask Register	$06
4	Pending Interrupt Register	$08
5	Interrupt Log List Pointer Register	$0A
6	BIT Word Register	$0C
7	Minor-Frame Timer	$0E
8	Command Block Pointer Register	$10
9	Not Applicable	$12
10	BC Command Block Initialization Count Register	$14
11-31	Not Applicable	$16- $3E

Table 2

MONITOR TERMINAL REGISTERS

Register Number	Name	Register Offset
0	Control Register	$00
1	Operational Status Register	$02
2	Current Command Block Register	$04
3	Interrupt Mask Register	$06
4	Pending Interrupt Register	$08
5	Interrupt Log List Pointer Register	$0A
6	BIT Word Register	$0C
7	Time-Tag Register	$0E
8-10	Not Applicable	$10-$14
11	Initial Monitor Command Block Pointer Register	$16
12	Initial Monitor Data Pointer Register	$18
13	Monitor Block Counter Register	$1A
14	Monitor Filter Register	$1C
15	Monitor Filter Register	$1E
16-31	Not Applicable	$20- $3E

Table 3

SHARED MEMORY SRAM

The IP-SUMMIT has a 64K x 16-bit Shared Memory. The base address of the SRAM is located in the IP Memory Space of the Host. Only 16-bit accesses are allowed. Arbitration between the Summit and the IP Bus is made by the local hardware. Summit access to the SRAM takes priority over any pending host access. Therefore, the host access will be held off until the summit access completes.

ID SPACE

The IP-SUMMIT conforms to the IP Bus Specification and has a 32 byte EEPROM that can be read to identify the IP module Manufacturer, type, revision,etc. The base address of the EEPROM is in the IP ID Space of the Host. The EEPROM is not protected against write. The Manufacturer ID identifies ALPHI as the manufacturer of the IP-SUMMIT module.

ID space address	Description	Value
$01	ASCII “I”	$49
$03	ASCII “P”	$50
$05	ASCII “A”	$41
$07	ASCII “C”	$43
$09	Manufacturer identification	$11
$0B	Module type	$00
$0D	Revision module	$43
$0F	Reserved	$00
$11	Driver ID,low byte	$00
$13	Driver ID,high byte	$00
$15	Number of bytes used	$0C
$17	CRC	
$19-$3F	User space	$XX

Table 4 IP-SUMMIT ID

IP INTERFACE

LOCAL MEMORY AND REGISTER MAP SUMMARY

IP MEM SPACE

NAME	OFFSET	DATA	R/W	COMMENTS
MEM SPACE	$0 - $1FFFF	D00-D15	R/W	Shared / Static RAM 64K x 16-bit (128Kbytes)

IP I/O SPACE

NAME	OFFSET	DATA	R/W	COMMENTS
SUMMIT REGISTERS	$00-$3F	D00-D15	R/W	SUMMIT Registers
INTERRUPT VECTOR	$40-$41	D00-D07	R/W	Interrupt Vector Registers
IP STATUS	$42-$43	D00-D07	R	Status Register

IP ID SPACE

NAME	OFFSET	DATA	R/W	COMMENTS
ID EEPROM	$00-$7F	D00-D07	R/W	IP EEPROM Identification

STATUS REGISTER

The IP STATUS register is used to determine the status of IP-SUMMIT jumper settings. The Status Register provides the following status bits:

Bit	Name	Function
0	MSEL0	Summit mode of Operation
1	MSEL1	
2	LOCK	Status of the Lock input Pin
3	READY	Status of the Ready Output Pin
4-7	NOT USED	

Table 5 Status register

SUMMIT MODE OF OPERATION

Mode select 0, in conjunction with Mode select 1 determines the Summit mode of operation. The table below describes these modes.

MSEL1	MSEL0	Mode Of Operation	W4:5-6	W4:7-8
0	0	Bus controller = SBC	ON	ON
0	1	Remote Terminal = SRT	ON	OFF
1	0	Monitor Terminal = SMT	OFF	ON
1	1	SMT/SRT	OFF	OFF

Table 6

LOCK

This read only bit reflects the inverted state of the LOCK input pin. The LOCK pin is latched on the rising edge of MRST. If the mode of operation must change, the user must perform a MRST.

READY

This read only bit reflects the inverted state of the output pin READY and is cleared on reset. This signal indicates the Summit has completed initialization or BIT, and regular execution may begin.

LOCAL INTERRUPT SOURCES

The SUMMIT has two (2) interrupt lines. These interrupts are Ored to the INTREQ0 pin on the IP bus. The Summit will provided the Interrupt Vector Register contents to the IP bus on D00-D07 during an interrupt acknowledge cycle.
Only Interrupt 0 on the IP Bus is used.

The source of each interrupt is listed below:

INTERRUPT name	Description
MSG_INT	Message interrupt.This pin is active for three clock cycles upon the occurrence of interrupt events which are enabled.
YF_INT	You failed Interrupt. This pin is active for three clock cycles upon the occurrence of interrupt events which are enabled.

Table 7

JUMPER LOCATION DIAGRAM

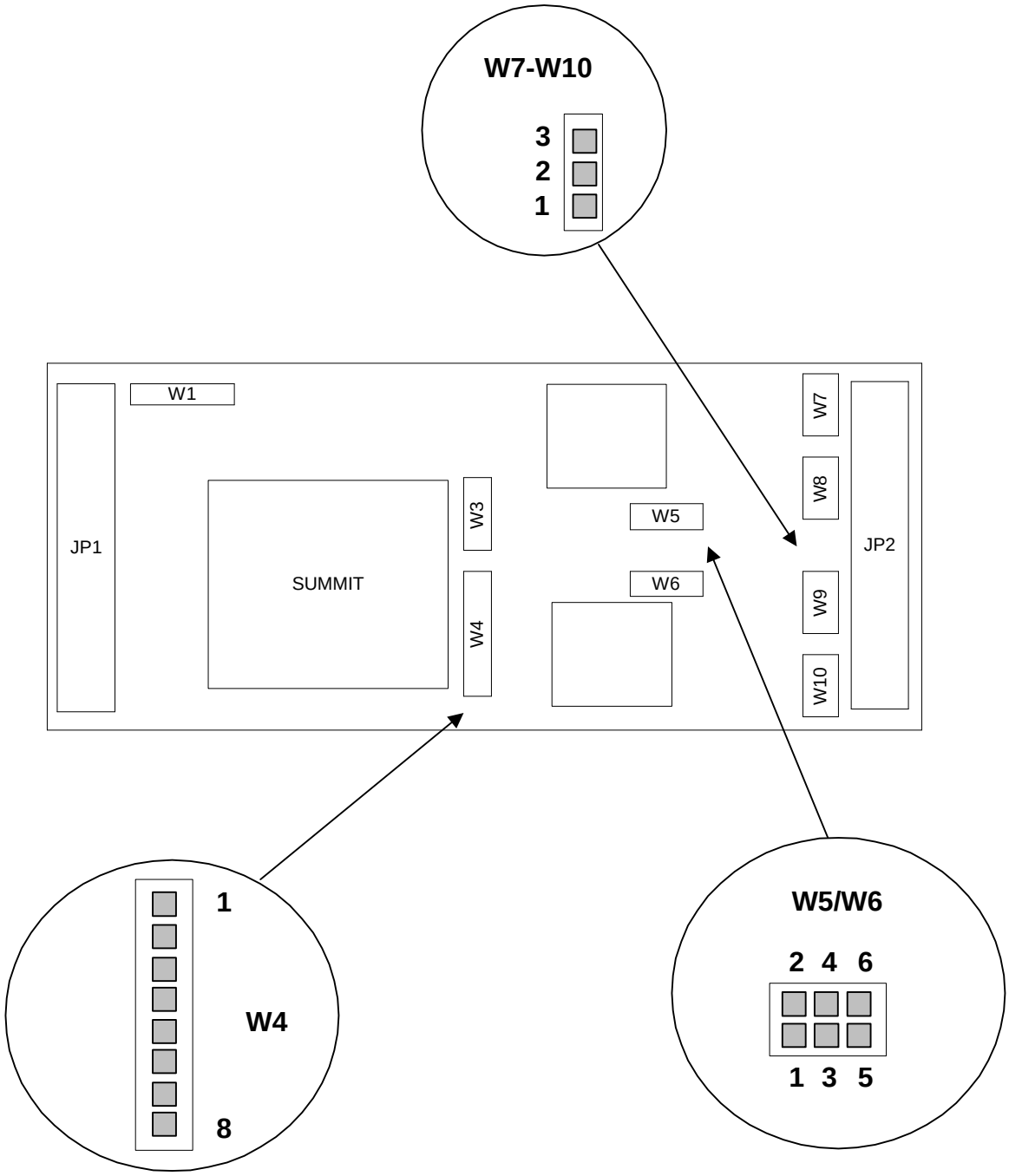

Figure 2

JUMPER	FACTORY SETTING	DESCRIPTION
W1	none	Lattice Ispl programation plug
W3	none	Summit JTAG test
W4	none	Mode of Operation of the SUMMIT
W5	none	Remote terminal address RTA0-RTA2
W6	none	Remote terminal address RTA3-RTPT
W7	2-3	Short Stub Output channel B -
W8	1-2	Short Stub Output channel B +
W9	2-3	Short Stub Output channel A -
W10	1-2	Short Stub Output channel A +

Table 8

W4 Mode of Operation Jumper Selection

Signal	Jumper set	Description
A/B* STD	1-2 ON OFF	 Military standard Mil_STD_1553B Military standard Mil_STD_1553A
LOCK	3-4 ON OFF	 Hardware configuration. This Pin when set active prevent Sotware change to both the RT address,A/B* STD and Mode select. Software configuration. Sotware change to both the RT address,A/B* STD and Mode select.
MSEL1	5-6 ON OFF	See Mode of Operation Table 6 Bit set to Logic “0” Bit set to Logic “1”
MSEL0	7-8 ON OFF	See Mode of Operation Table 6 Bit set to Logic “0” Bit set to Logic “1”

Table 9

W5 RT Address Selection

Signal	Jumper set	Description
RTA2	1-2 ON OFF	 RT Address BIT 2 set to Logic “0” RT Address BIT 2 set to Logic “1”
RTA1	1-2 ON OFF	 RT Address BIT 1 set to Logic “0” RT Address BIT 1 set to Logic “1”
RTA0	1-2 ON OFF	 RT Address BIT 0 set to Logic “0” RT Address BIT 0 set to Logic “1”

Table 10

W6 RT Address Selection

Signal	Jumper set	Description
RTPT	1-2 ON OFF	 RT Parity set to Logic “0” RT Parity set to Logic “1”
RTA4	1-2 ON OFF	 RT Address BIT 4 set to Logic “0” RT Address BIT 4 set to Logic “1”
RTA3	1-2 ON OFF	 RT Address BIT 3 set to Logic “0” RT Address BIT 3 set to Logic “1”

Table 11

W7 & W8 1553 Output Channel B Configuration

Signal	Jumper set W7	Jumper set W8	Description
CH B	1-2 ON 2-3 ON	2-3 ON 1-2 ON	Long Stub Output channel B Short Stub Output channel B

Table 12

W9 & W10 1553 Output Channel A Configuration

Signal	Jumper set W7	Jumper set W8	Description
CH A	1-2 ON	2-3 ON	Long Stub Output channel A
	2-3 ON	1-2 ON	Short Stub Output channel A

Table 13

SUMMIT I/O CONNECTIONS

I/O PIN	SIGNAL DESCRIPTION
1	GND
2	
3	GND
4	
5	GND
6	
7	GND
8	TIME-TAG CLK
9	GND
10	
11	GND
12	RTA4
13	GND
14	RTA3
15	GND
16	RTA2
17	GND
18	RTA1
19	GND
20	RTA0
21	GND
22	RTPT
23	GND
24	
25	

I/O PIN	SIGNAL DESCRIPTION
26	GND CHA
27	OUTCH A+
28	
29	OUTCH A-
30	
31	
32	
33	
34	
35	
36	
37	DMAG LED+
38	TERAC LED-
39	DMAG LED-
40	TERAC LED+
41	
42	
43	
44	
45	
46	
47	OUTCH B+
48	
49	OUTCH B-
50	GND CHB

IP-SUMMIT TRANSITION MODULE