# CPCI-SIP-PLX

## Slave 2- IndustryPack® Carrier for 3U *CompactPCI*™ systems

## REFERENCE MANUAL

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Part Number : 824-12-000-4000 

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# 1. GENERAL DESCRIPTION

## 1.1 INTRODUCTION

The CPCI-SIP-PLX is a 3U format CompactPCI (CPCI) bus IP carrier. The **CPCI-SIP-PLX** provides mechanical support and the electrical interfaces for two single width IP modules. Multiple **CPCI-SIP-PLX** boards may be installed in a single system. The primary features of the **CPCI-SIP-PLX** are as follows:

- Support for up to two IP modules
- 8 MHz or 32 MHz IP clock operation by IP.
- Direct I/O or Memory mapped access from CPCI bus via PLX 9080 PCI Chip
- Full interrupt support of host
- Front panel I/O connectors for all IP's
- Two PXI_TRIG[1..0] signals

## 1.2 FUNCTIONAL DESCRIPTION

A functional block diagram of the **CPCI-SIP-PLX** is presented below in Figure 1-1.

The jumper placement and the connector placement are depicted in Figure 1-2.

The **CPCI-SIP-PLX** operates as a slave that is managed by the host processor on the CPCI bus.

The **CPCI-SIP-PLX** is supported by ALPHI Technology under *Windows XP* by a **Board Support Package, which** is supplied with the card. Other documentation supplied with the card will describe this support in full detail.

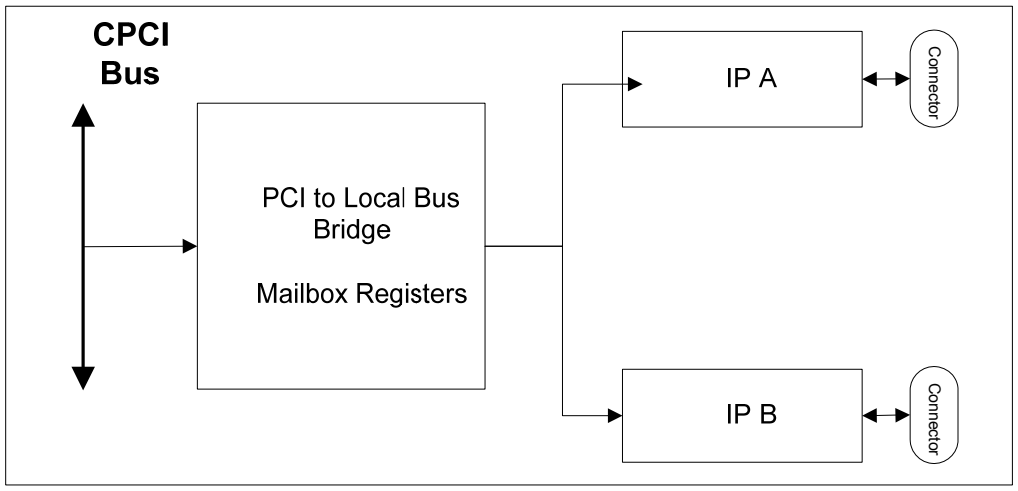


***Figure 1.1: Block Diagram***

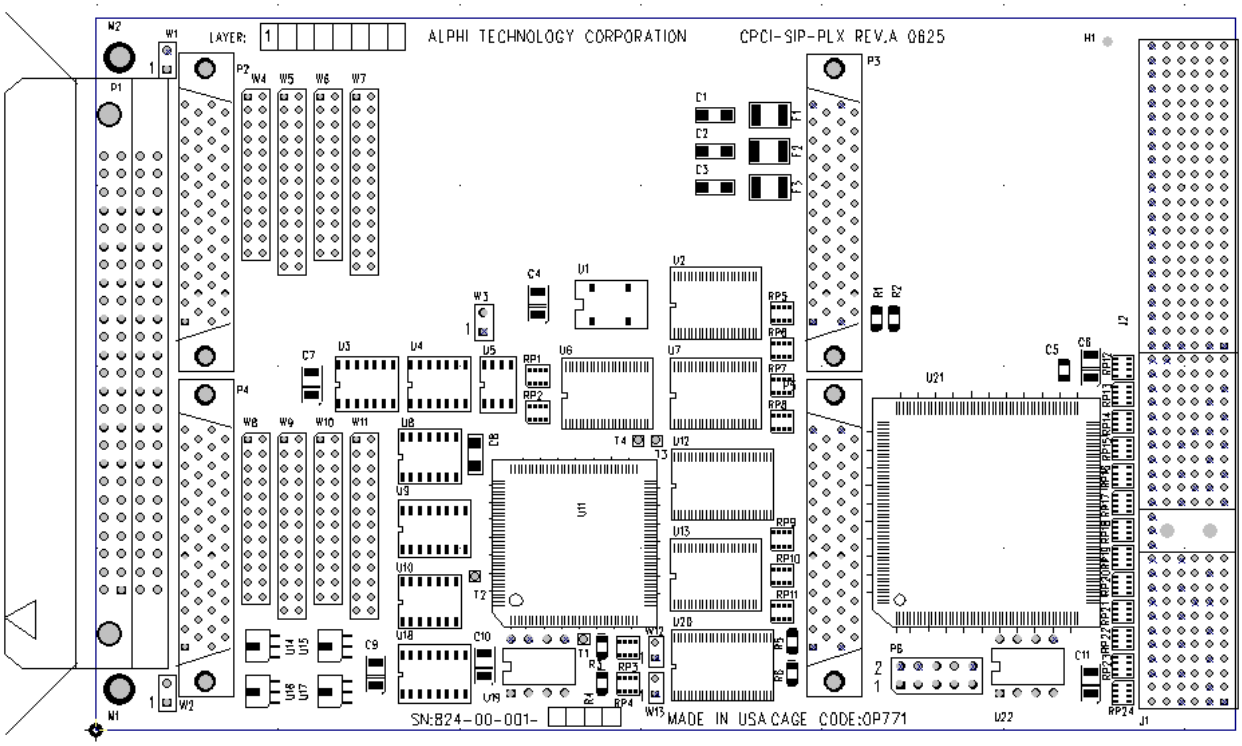


***Figure 1.2: Jumper and Connector Locations***

### 1.3 PXI_TRIG[1..0]

The two lines PXI_TRG[1..0] are located at the jumper W1 and W2.

W1 pin 1 = PXI_TRG[0], pin 2 = GND

W2 pin 1 = PXI_TRG[1], pin 2 = GND

HOST (CPCI) SIDE

## 1.4 CPCI CONFIGURATION REGISTERS

The card presents the following configuration values to the CPCI system, based on the values stored in the NVRAM device read by the PLX 9080 PCI interface chip.

| Register | Value (Meaning) |
|---|---|
| Vendor ID | 0x13c5 (ALPHI Technology) |
| Device ID | 0x0113 (CPCI-SIP-PLX) |
| Revision ID | 0x00 |
| Class Code | 0xff0000 (Device does not fit into defined class codes) |
| Interrupt Line | 0xff |
| Interrupt Pin | A |
| Multifunction Device | No |
| Build In Self Test | No |
| Latency Timer | 0x00 |
| Minimum Grant | 0x00 |
| Maximum Latency | 0x00 |
| Expansion ROM Size | None |

***Table 1.1: CPCI Configuration Registers***

## 1.5 CPCI BASE ADDRESS REGISTERS

The card requests base address regions from the CPCI system after RESET, based on the values stored in the NVRAM device read by the PLX 9080 PCI interface chip.

The decode addresses of these regions are assigned by the host processor. The **CPCI-SIP-PLX** uses 3 of the 4 PLX 9080 mapped base address registers. The PLX 9080 is normally programmed at the factory to request the following resource from the CPCI BIOS:

| BAR | From | To | Description | Type | SIZE |
|---|---|---|---|---|---|
| 0 | 0x00000000 | 0x00000003F | PLX PCI Operation Registers | I/O | 64 |
| 2 | 0x00000000 | 0x000007FF | IP ID and IO Region | I/O | 2 K |
| 3 | 0x00000000 | 0x00FFFFFF | IP Memory Region | MEM | 16M |

***Table 1.2: Base Address and Use***

## 1.6 CPCI OPERATION REGISTERS

The host processor communicates with the **CPCI-SIP-PLX** card via the PLX pass-through interface. After the base address register has been programmed by the CPCI configurator, incoming CPCI I/O or Memory cycles are used to access the registers of the PLX 9080 chip. The PCI Operation Registers of the PLX 9080 chip are depicted below:

| NAME | PCI Addr. | 31 – 24 | 23 – 16 | 15 – 8 | 7 – 0 |
|---|---|---|---|---|---|
| **PCIIDR** | 0x00 | Device ID | | Vendor ID | |
| **PCICR** | 0x04 | Status | | Command | |
| **PCISR** | 0x08 | Class Code | | | Revision ID |
| **PCIREV** | 0x0C | BIST | Header Type | PCI Latency Timer | Cache Line Size |
| **PCICCR** | 0x10 | PCI Base Address 0 (Memory Access to PLX Registers) | | | |
| **PCICLSR** | 0x14 | PCI Base Address 1 (I/O Access to PLX Registers) | | | |
| **PCILTR** | 0x18 | PCI Base Address 2 (Memory Access to DSP SRAM, IP IOSPACE, and other card registers) | | | |
| **PCIHTR** | 0x1C | PCI Base Address 3 (Memory Access to DPR) | | | |
| **PCIBISTR** | 0x20 | Unused PCI Base Address 4 | | | |
| **PCIBAR0** | 0x24 | Unused PCI Base Address 5 | | | |
| **PCIBAR1** | 0x28 | Cardbus CIS Pointer (Not Supported) | | | |
| **PCIBAR2** | 0x2C | Subsystem ID | | Subsystem Vendor ID | |
| **PCIBAR3** | 0x30 | PCI Base Address for Expansion ROM | | | |
| **PCIBAR4** | 0x34 | Reserved | | | |
| **PCIBAR5** | 0x38 | Reserved | | | |
| **PCICIS** | 0x3C | Max Latency | Min Grant | Interrupt Pin | Interrupt Line |

***Table 1.3: PCI Configuration Space***

## 2. LOCAL SIDE

### 2.1 I/O MAP

The local I/O space is shared between the IP space and the local registers.

Two (2Kbytes) are reserved by the board to access all the locals registers and IP registers.

The local bus is a 16-bits bus. PCI can be 8,16 OR 32-bits access.

The local registers are located within the I/O space of the IP_A from I/O +$C0 to $FF

| FROM | TO | R/W | REGION |
|---|---|---|---|
| 0x00 | 0x3F | R/W | IP_A ID Space |
| 0x80 | 0x81 | R | IP_A Interrupt Vector 0 |
| 0x82 | 0x83 | R | IP_A Interrupt Vector 1 |
| | | | |
| *0xC0* | *0xFF* | *R/W* | *Local status and control registers* |
| | | | |
| 0x100 | 0x17F | R/W | IP_A I/O Space |
| | | | |
| 0x200 | 0x23F | R/W | IP_B ID Space |
| 0x280 | 0x281 | R | IP_B Interrupt Vector 0 |
| 0x282 | 0x283 | R | IP_B Interrupt Vector 1 |
| 0x300 | 0x37F | R/W | IP_B I/O Space |
| | | | |

***Table 2.1: IP ID and I/O Regions***

## 2.2 IP MEMORY MAP

Each IP module can decode up to 8 Mbytes of Memory. A total of 16 Mbytes have been allocated by the PCI host. Access are 8/16 or 32-bits . As the local bus is 16 bus wide a 32 bit access will be two back to back access.

| PLX 9080 | FROM | TO | R/W | REGION |
|---|---|---|---|---|
| BAR3 | 0x00000000 | 0x007FFFFF | R/W | IP_A Memory Space |
| BAR3 | 0x00800000 | 0x00FFFFFF | R/W | IP_B Memory Space |

***Table 2.2: IP Memory Regions***

## 2.3 LOCAL REGISTERS

The CPCI_4SIP_plx has registers use to defined the functionality of each IP and to route and/or enable the different interrupts or strobes.

| BASE + $ | R/W | Bit used | Name | Function |
|---|---|---|---|---|
| 0x88 | W | xx | IP_GLOBAL_RESET | Global reset for all IP'. |
| 0xC0 | R/W | 7..0 | CTRL_0 | IP's clock speed |
| 0XC2 | R/W | 0 | IP ERROR signal | |
| 0xA0 | R/W | 7..0 | INT0_en Registers | Enable IP's interrupts to be source of LINTI # signal |
| 0xA2 | R/W | 3..0 | INT2_en Registers | Enable IP strobes from IP's to be source of LINTI # signal |
| 0xA2 | R/W | 7..4 | INT2_en Registers | Enable PXI_TRIG[1..0] lines to be source of LINTI # signal |
| 0xA6 | R/W | 3..0 | INT6_en Registers | Enable IP_DMA's request lines to be source of LINTI # signal |
| 0xA8 | W | xx | IP_A reset | A write generate an IP_reset to IP_A. |
| 0xA8 | R | 7..0 | IP's Interrupt status | Status of IP's interrupts. |
| 0xAA | W | xx | IP_B reset | A write generate an IP_reset to IP_B. |
| 0xAA | R | 7..0 | IP's Strobe / PXI lines status | Status of IP's strobe lines PXI_TRIG[1..0] lines |
| 0xAE | R | 7..0 | IP's DMA request status | Status of IP's DMA requests lines. |
| 0xD0 | R/W | 7..0 | IP's strobe | Control source signal for IP's strobe if selected as input. |
| 0xD6 | R/W | 7..0 | HOST_REG_[3..0] | Provide a TTL high or Low signal controlled by software to the PXI_TRIG[1..0] line if selected. |
| 0xD8 | R/W | 3..0 | PXI_TRIG[0] | PXI_TRIG[0] source signal selection |
| 0xD8 | R/W | 7..4 | PXI_TRIG[1] | PXI_TRIG[1] source signal selection |

***Table 2.3: Local registers***

xx : any data value

### 2.3.1 IP_Global _Reset

Base address of IP-A + $88

A write access(any data) at this location will provide assertion of the IP_RESET line of all the two IP's.

### 2.3.2 CTRL_0 register

Base address of IP-A + $C0

This register controls the IP clock speed for each IP.

| Bit | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|
| | NA | NA | IP_B clock | IP_A clock | | LINTI_en | | |

"0" = 8 MHZ IP clock (default)

"1" = 32 MHZ IP clock

When Bit # 2 is set to "1" Interrupt source can be routed to the PLX 9080 through the LINTI # line.

### 2.3.3 ERROR register

Base address of IP-A + $C2

If an IP module generate an ERROR signal, it is latched .

Bit # 0 of Base address of IP-A + $C2 reflect the status of the ERROR line. When "0" an ERROR signal has been detected and latched.

To reset the latch a write access need to be made at the address :

Base address of IP-A + $C2.

### 2.3.4 Source selection interrupts

#### 2.3.4.1 INT0_en Register

Base address of IP-A + $A0

This 8-bits register allows one or more IP's interrupt line to be the source signal for the unique PCI interrupt line LINTI #. A "1" to the associate bit enable the corresponding line.

Status of the interrupts is located at Base address of IP_A + $A8

| Bit | Register Name |
|---|---|
| Bit 0 | INTREQA0 |
| Bit 1 | INTREQA1 |
| Bit 2 | INTREQB0 |
| Bit 3 | INTREQB1 |
| Bit 4 | NA |
| Bit 5 | NA |
| Bit 6 | NA |
| Bit 7 | NA |

***Table 2.4: CPCI IP Interrupt enable REGISTER***

#### 2.3.4.2 INT2_en Registers

Base address of IP-A + $A2

This 8-bits register allows one or more IP's Strobe line or PXI_TRIG[1..0] (if defined as output) to be the source signal for the unique PCI interrupt line LINTI #. A "1" to the associate bit enable the corresponding line.

Status of the IP Strobe lines is located at Base address of IP_A + $AA

| Bit | Register Name |
|---|---|
| Bit 0 | IP_A STROBE |
| Bit 1 | IP_B STROBE |
| Bit 2 | Not used |
| Bit 3 | Not used |
| Bit 4 | BERR SIGNAL |
| Bit 5 | PXI_TRIG[0] |
| Bit 6 | PXI_TRIG[1] |
| Bit 7 | VCC(NOT USED) |

***Table 2.5: CPCI IP Strobe REGISTER***

#### 2.3.4.3 INT6_en Registers

Base address of IP-A + $A6

This 8-bits register allows one or more IP's DMA request line to be the source signal for the unique PCI interrupt line LINTI #. A "1" to the associate bit enable the corresponding line.

Status of the IP DMA request lines is located at Base address of IP_A + $AE

| Bit | Register Name |
|---|---|
| Bit 0 | DMARQA0 |
| Bit 1 | DMARQA1 |
| Bit 2 | DMARQB0 |
| Bit 3 | DMARQB1 |
| Bit 4 | NA |
| Bit 5 | NA |
| Bit 6 | NA |
| Bit 7 | NA |

***Table 2.6: CPCI IP DMA REGISTER***

### 2.3.5 IP_reset registers

Base address of IP-A + $A8-$AE

Each IP can be individually reset by a host write at address:

A global reset can also be generated by writing at address Base address of IP-A + $88

| BASE ADDRESS IP_A + | IP_Reset |
|---|---|
| $A8 | A |
| $AA | B |

### 2.3.6 IPSTROBE source register

Base address of IP-A + $D0

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| Not used | Not used | Gate_en_B | Gate_en_A | Not used | Not used | Gate_1 | Gate_0 |

**Gate_[3..0]**

Four bits multiplexer control lines as selection of IPSTROBE for one or more IP modules.

| Gate_[3..0] | Source to IPSTROBE |
|---|---|
| 0000 | IPSTROBE_A |
| 0001 | IPSTROBE_B |
| 0010 | IPSTROBE_C |
| 0011 | IPSTROBE_D |
| 0100 | HOST_REG[0] |
| 0101 | IPINT_A0 |
| 0110 | IPINT_A1 |
| 0111 | IPINT_B0 |
| 1000 | IPINT_B1 |
| 1001 | Not used |
| 1010 | Not used |
| 1011 | Not used |
| 1100 | Not used |
| 1101 | 8MHZ CLOCK |
| 1110 | PXI_TRIG[0] |
| 1111 | PXI_TRIG[1] |

**Gate_en_ [A, B, C, D]**

When set to a “1” the correspondent IPSTROBE line is enable as OUTPUT and will convey the source signal already selected by the lower bit[3..0] to INDUSTRY-PACK IPSTROBE module.

Base address of IP-A + $D6

This register use only the FOUR lower bits [3..0] that ,when controlled by the host, can been routed to the IPSTROBE's or the PXI_TRIG[1..0] lines.

Signal name is HOST_REG[3..0].

**PXI_SOURCE register**

Base address of IP-A + $D8

Two bi-directional lines are available to the user. Each line can be programmed as input (default) or output.

As INPUT the PXI_TRIG [1..0] line can be routed to the PCI interrupt line through the LINTI # signal or to the IPSTROBE line of each INDUSTRY-PACK module.

As OUTPUT the PXI_TRIG [1..0] can convey a synchronization signal which source can be an interrupt or an IPSTROBE signal from any INDUSTRY-PACK module.

Also a host can access these lines and generate a pulse or a level using HOST_REG[3..0] bits.

Each lower three bit of the half-byte is use as control lines of a 8 to 1 multiplexer to select the source of the signal that will be output to the PXI_TRIG[1..0]. When one of this three bit is ="1" the PXI_TRIG[] line is set as output and an external open drain buffer is enable.

A read-back of the register reflects on the bit #3 and bit #7 the status of the correspondent PXI_TRIG[1..0] lines.

| Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|
| PXI_TRIG[0] LINE STATUS (READ ONLY) | PXI_IO_02 | PXI_IO_01 | PXI_IO_00 |

| Bit 7 | Bit 6 | Bit 5 | Bit 4 |
|---|---|---|---|
| PXI_TRIG[1] LINE STATUS (READ ONLY) | PXI_IO_12 | PXI_IO_11 | PXI_IO_10 |

| PXI_IO_0[2..0] | Source to PXI_TRIG[0] |
|---|---|
| 000 | GND |
| 001 | HOST_REG[0] |
| 010 | IPSTROBE |
| 011 | IPINT_A0 |
| 100 | IPINT_B0 |
| 101 | Not used |
| 110 | Not used |
| 111 | HOST_REG[2] |

| PXI_IO_1[2..0] | Source to PXI_TRIG[1] |
|---|---|
| 000 | GND |
| 001 | HOST_REG[1] |
| 010 | IPSTROBE |
| 011 | IPINT_A0 |
| 100 | IPINT_B0 |
| 101 | Not used |
| 110 | Not used |
| 111 | HOST_REG[3] |

Note: When input the PXI_TRIG[1..0] line are clocked with the local 32Mhz clock.

Example: Generate the 8MHZ clock to the PXI_TRI[1..0] lines

-Set **IPSTROBE source register** I/O +$D0 to “0D”

-Set **PXI_SOURCE register** I/O +$D8 to “22”.

A read-back of the register reflects on the bit #3 and bit #7 the status of the correspondent PXI_TRIG[1..0] lines.

If the 8MHZ need to be convey to the IPSTROBE_A set **IPSTROBE source register** I/O +$D0 to “1D”

### 2.4 TIME-OUT

A Time-out counter will terminate any access to the local board after 3 µS.

# 3. IP DETAILS

## 3.1 IP MODULE ID SPACE

Each IP must support identification PROM. The CPCI-SIP-PLX decodes 64 bytes of ID space for each IP module. The ID PROM contains information about each the IP, which is defined in the Industry Pack Specification. The two IP ID's spaces can be accessed at fixed offsets from Base Address 1, as indicated in Table 2.5. The information required for the most common IP PROM format is shown below:

| OFFSET | DESCRIPTION | VALUE |
|---|---|---|
| 0x00 | ASCII "I" | 0x49 |
| 0x02 | ASCII "P" | 0x50 |
| 0x04 | ASCII "A" | 0x41 |
| 0x06 | ASCII "C" | 0x43 |
| 0x08 | Manufacturer ID | |
| 0x0A | Model No | |
| 0x0C | Revision | |
| 0x0E | Reserved | 0x00 |
| 0x10 | Driver ID, Low Byte | |
| 0x12 | Driver ID, High Byte | |
| 0x14 | Number of bytes used | 0x0C |
| 0x16 | CRC | |
| OFFSET | DESCRIPTION | VALUE |

***Table 3.1: Typical ID Space Layout***

## 3.2 IP MODULE IO SPACE

The CPCI-SIP-PLX decodes 128 bytes of IO space for each IP module. The two IP I/O spaces can be accessed at fixed offsets from Base Address 1, as indicated in Table 2.5.

## 3.3 IP MODULE MEMORY SPACE

The CPCI-SIP-PLX decodes 8 Mbytes of MEM space for each IP module. The two IP MEM spaces can be accessed at fixed offsets from Base Address 2 as indicated in Table 2.6.

### 3.4 IP MODULE INTERRUPT SPACE

The CPCI-SIP-PLX routes the interrupts from all IP modules to the LINTI # signal of the PLX 9080.

The CPCI-SIP-PLX decodes 2 16-bit words of INT space for each IP module to supply an optional interrupt vector. The two IP INT spaces can be accessed at fixed offsets from Base Address 1, as indicated in Table 2.5.

Some IP modules may require that the host processor perform a read to INT space to clear pending interrupts.

## 4. RESET SIGNALS

The **CPCI-SIP-PLX** can be reset from four different sources:

- At power on
- The PLX 9080 has a bit called SYSRST that the HOST can toggle to reset all the IP's at the same time. This will result on the LRESETO #signal to been asserted.
- By performing a write access (any data) to the local registers :
  Base IP_A +$A8 for IP_A,
  Base IP_A +$AA for IP_B,

- By performing a write access (any data) to the location :
  Base IP_A +$88 ( Global IP_reset).

## 5. LED INDICATORS

There are Four LED indicators visible at the CPCI card bracket. They are marked with a legend on the bracket, and they are labeled on the PCB as L1 – L3 where L1 is at the top of the card.

The LED's have the following meanings:

| LED | Meaning |
|---|---|
| SL1 | CPCI Accessing IP- A |
| SL2 | CPCI HOST accessing |
| SL3 | STROBE accessing |
| SL4 | CPCI Accessing IP- B |

***Table 5.1: LED Descriptions***

## 6. CONNECTIONS

### 6.1 IP I/O CONNECTORS (P5,P2)

The I/O signals for the two IP's are directly routed off the card through the front panel.

| Connector | I/O for |
|---|---|
| P1 (lower) | IP_A |
| P1 (Upper) | IP_B |

50 pin Ribbon Style connectors are used to route all the IP I/O signals off the card. ALPHI Technology can supply transition modules and cable assemblies to meet any special requirements. Contact the factory for additional information.

Connectors are manufactured by 3M

| Use | Model |
|---|---|
| On PC Board | 3433-D302 |
| Suggested Plug | 3425-7600 |

***Table 6.1: I/O Connector Model Numbers***

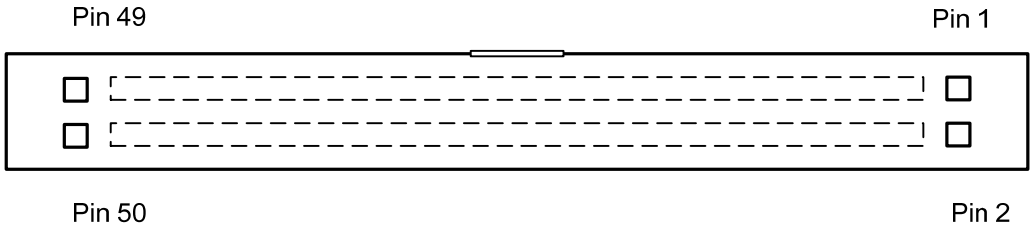


***Figure 1.2: IP I/O CONNECTORS***