CPCI-ISC8

Intelligent 8 Channel
Serial Communications Controller
for *CompactPCI*™ systems

REFERENCE MANUAL

756-00-001-4000
Version 1.0
February 1999

ALPHI TECHNOLOGY CORPORATION

6202 S. Maple Avenue #120
Tempe, AZ 85283 USA
Tel: (480) 838-2428
Fax: (480) 838-4477

NOTICE

The information in this document has been carefully checked and is believed to be entirely reliable. While all reasonable efforts to ensure accuracy have been taken in the preparation of this manual, ALPHI TECHNOLOGY assumes no responsibility resulting from omissions or errors in this manual, or from the use of information contain herein.

ALPHI TECHNOLOGY reserves the right to make any changes, without notice, to this or any of ALPHI TECHNOLOGY's products to improve reliability, performance, function or design.

ALPHI TECHNOLOGY does not assume any liability arising out of the application or use of any product or circuit described herein; nor does ALPHI TECHNOLOGY convey any license under its patent rights or the rights of others.

Part Number : 724-20-000-4000

TABLE OF CONTENTS

Part Number : 724-20-000-4000

1. GENERAL DESCRIPTION

1.1 INTRODUCTION

The **CPCI-ISC8** is an intelligent DSP based serial communication board. This 3U board is based on the ***CPCI-IPC*** product and has been modified to remove the IP interface and to support additional I/O features. The **CPCI-ISC8** provides mechanical support and the electrical interfaces for an I/O mezzanine board. Multiple **CPCI-ISC8** boards may be installed in a single system. The primary features of the **CPCI-ISC8** are as follows:

- Integrated DSP (TI TMS320C31) at 32 MHz to offload I/O operation from host or for standalone applications
- Support for application specific serial mezzanine I/O
- Direct memory mapped control of DSP from CPCI bus via AMCC 5933 PCI Chip
- Full interrupt support of host and DSP
- Front panel I/O connectors for all mezzanine I/O
- Four (4) 16 MHz Z85230 SCC devices
- All Z85230 I/O lines routed to mezzanine connectors
- One external interrupt input

1.2 FUNCTIONAL DESCRIPTION

A functional block diagram of the **CPCI-ISC8** is presented below in Figure 1-1. The jumper placement and the connector placement is depicted in Figure 1-2. The **CPCI-ISC8** can operate as a slave that is managed by the host processor on the CPCI bus or it can operate in a standalone mode of operation without a host.

The **CPCI-ISC8** is supported by ALPHI Technology under *Windows NT* by a **Board Support Package** which is supplied with the card. Other documentation supplied with the card will describe this support in full detail.

The card is also supported by a **DSP Support Library** providing the following features:

- Common access routines for communications with the HOST
- Mapping C language standard input and output by each of the DSPs to the onboard 8530 serial chips
- Identify the applicable card resources and parameters

All these are provided in a manner consistent across ALPHI Technology platforms. Other documentation supplied with the card will describe the support in full detail.

A bootloader provided on the card allows for control by the HOST and for independent operation in stand alone operation. User code can be downloaded to FLASH memory and booted automatically on reset. Access to the card can be made both by the HOST CPCI bus and serially through the 8530.

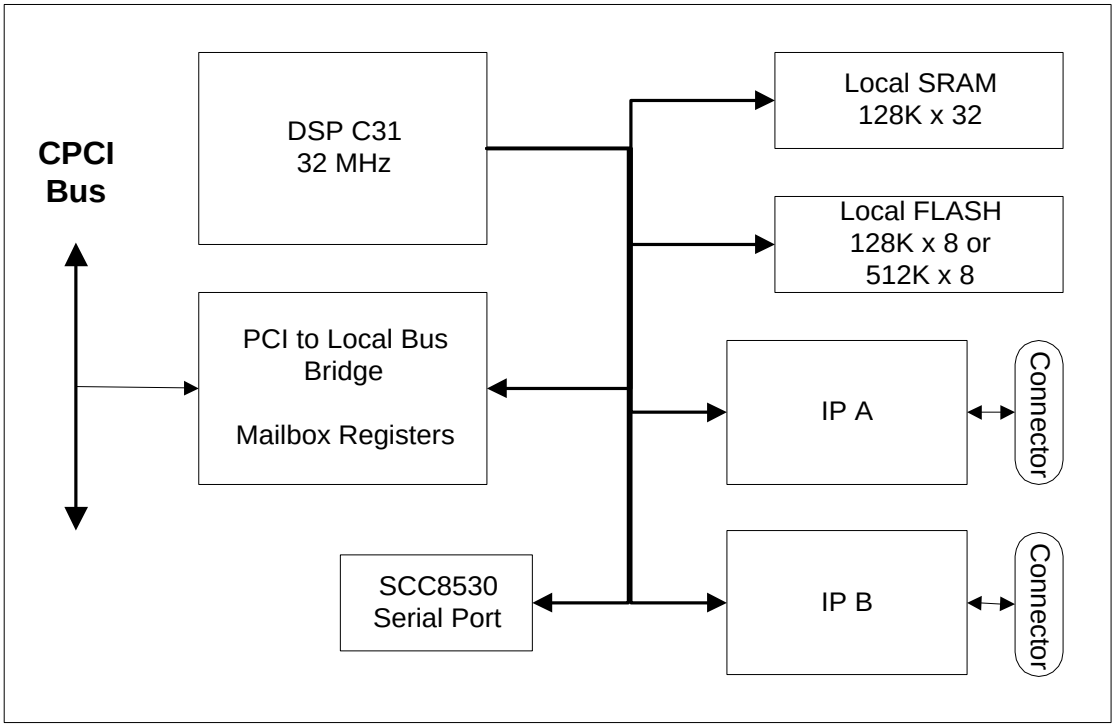

Figure 1.1: Block Diagram

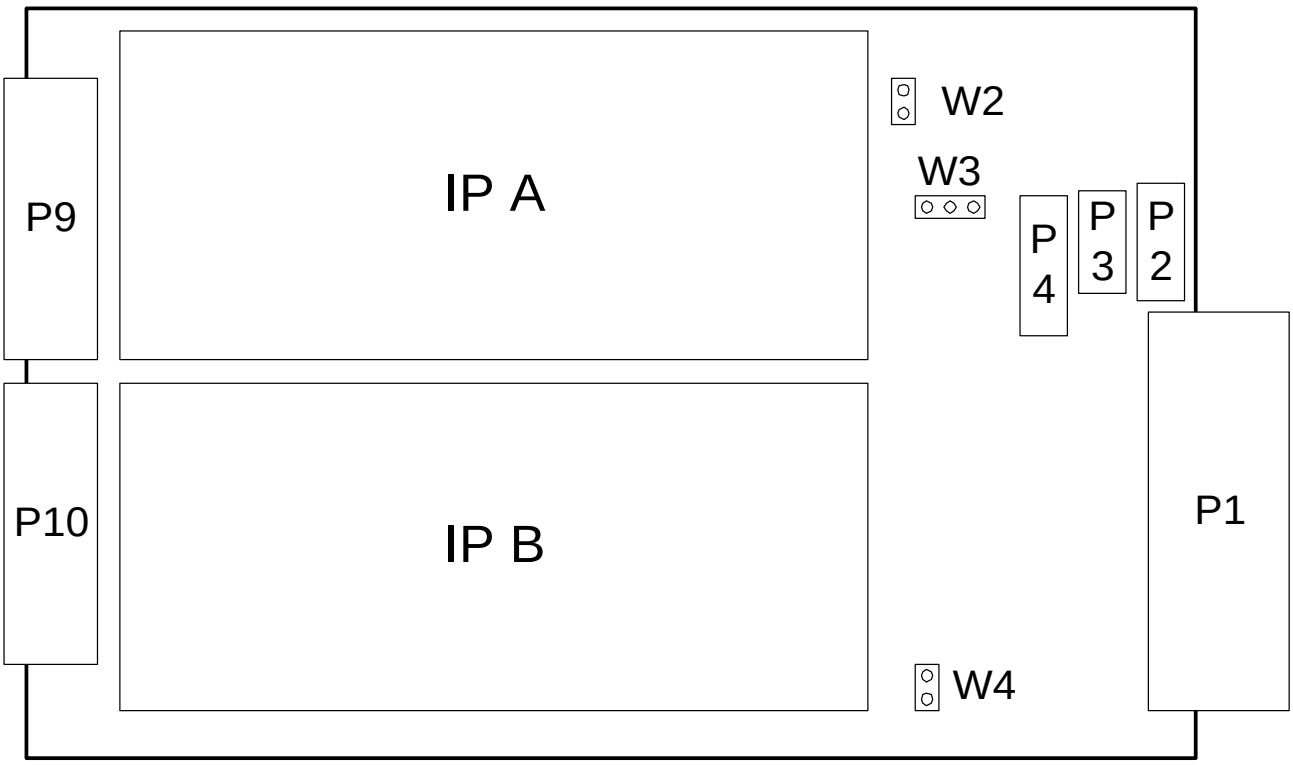

Figure 1.2: Jumper and Connector Locations

1.3 REFERENCE MATERIALS LIST

The reader should refer to the PCI Local Bus Specification for a detailed explanation of the PCI bus architecture and timing requirements. This specification is available from the following source:

PCI Special Interest Group
PO Box 14070
Portland, OR 97214
Tel: (800) 433-5177
Tel: (503) 797-4207
Fax: (503) 234-6762

The reader is also referred to the S5933 PCI Controller data book:

AMCC Applied Micro Circuits Corporation
6195 Lusk Boulevard
San Diego, CA 92121-2793
Tel: (800) 755-2622
http://www.amcc.com

WindowsNT and Windows95 Programming Tools:

BlueWater Systems
144 Railroad Ave. Suite #217
Edmonds, WA 98020
Tel: (206) 771-3610
Fax: (206) 771-2742
E-Mail: info@bluewatersystems.com
Web: http://www.bluewatersystems.com

2. HOST (CPCI) SIDE

2.1 PCI CONFIGURATION REGISTERS

The card presents the following configuration values to the CPCI system, based on the values stored in the NVRAM device read by the AMCC PCI interface chip.

Register	Value (Meaning)
Vendor ID	0x13c5 (ALPHI Technology)
Device ID	0x0101 (CPCI-ISC8) uses CPCI-IPC ID
Revision ID	0x00
Class Code	0xff0000 (Device does not fit into defined class codes)
Interrupt Line	0xff
Interrupt Pin	A
Multifunction Device	No
Build In Self Test	No
Latency Timer	0x00
Minimum Grant	0x00
Maximum Latency	0x00
Expansion ROM Size	None

Table 2.1: CPCI Configuration Registers

2.2 PCI BASE ADDRESS REGISTERS

The card requests base address regions from the CPCI system after RESET, based on the values stored in the NVRAM device read by the AMCC PCI interface chip.

The decode addresses of these regions are assigned by the host processor. The **CPCI-ISC8** uses 1 of the 5 AMCC mapped base address registers. The AMCC is normally programmed at the factory to request the following resource from the CPCI BIOS:

BAR	From	To	Description	Type
0	0x00000000	0x00000003F	AMCC PCI Operation Registers	MEM

Table 2.2: Base Address and Use

NOTE: The AMCC has been programmed to request memory above 1 Mbytes.

2.3 CPCI OPERATION REGISTERS

The host processor communicates with the **CPCI-ISC8** card via the AMCC pass-through interface. After the base address register has been programmed by the CPCI configurator, incoming CPCI I/O or Memory cycles are used to access the registers of the AMCC chip. The PCI Operation Registers of the AMCC 5933 chip are depicted below:

Offset	Register Name
0x00	OMB1 Outgoing Mailbox Register 1
0x04	OMB2 Outgoing Mailbox Register 2
0x08	OMB3 Outgoing Mailbox Register 3
0x0C	OMB4 Outgoing Mailbox Register 4
0x10	IMB1 Incoming Mailbox Register 1
0x14	IMB2 Incoming Mailbox Register 2
0x18	IMB3 Incoming Mailbox Register 3
0x1C	IMB4 Incoming Mailbox Register 4
0x20	FIFO Register Port (bi-directional)
0x24	MWAR Master Write Address Register
0x28	MWTC Master Write Transfer Counter
0x2C	MRAR Master Read Address Register
0x30	MRTC Master Read Transfer Counter
0x34	MBEF Mailbox Empty/Full Status
0x38	INTCSR Interrupt Control/Status Register
0x3C	MCSR Bus Master Control/Status Register

Table 2.3: AMCC Registers (HOST)

For more information about these registers refer to the AMCC PCI controller manual.

3. C31 SIDE

3.1 INTERNAL ORGANIZATION

The **CPCI-ISC8** card is divided into different sections. Each section and its relationship to other sections will be discussed. The **CPCI-ISC8** sections are:

- CPCI interface
- Local I/O interface

3.2 CPCI INTERFACE

The local DSP processor communicates with the CPCI bus through the AMCCS9533 chip that provides bi-directional FIFO and Mailbox registers. The **CPCI-ISC8** can function as both a servant (CPCI target) or as a master (CPCI initiator) for DMA access. The following interface descriptions refer to the CPCI interface as seen by the local DSP. The AMCC registers are located at DSP address 0xf00080.

3.2.1 BI-DIRECTIONAL FIFO

Two separate FIFO data paths are implemented within the AMCCS9533, a read FIFO that allows data transfers from the module to the CPCI bus and a write FIFO that transfers data from the CPCI to the module. Size of the FIFO is 32 bit X 8. Read and write DMA access to the host can occur via the FIFO registers if it is supported by the software on the HOST and is enabled. Alternatively, the FIFO registers can utilize a polled scheme on the HOST and

DSP. Both FIFOs are accessed via access to the same location as seen by the DSP, offset 0x08.

3.2.2 MAILBOX REGISTERS

The Mailbox registers of the AMCCS9533 provide a bi-directional data path that can be used to send data or software control information between the HOST and DSP of that half of the **CPCI-ISC8** module. Interrupts can be enabled based on a specific mailbox event. There are 4 incoming mailboxes and 4 outgoing mailboxes. Each mailbox is 32 bits wide. The address offsets for the mailboxes are shown below in Table 3-1.

3.2.3 ADDITIONAL REGISTERS

The AMCC S5933 PCI controller has a set of additional registers to control and monitor the behavior of the CPCI interface.

The address offsets of these registers are shown below in Table 3-1.

Offset	Register Name
0x00	Incoming Mailbox Reg 1
0x01	Incoming Mailbox Reg 2
0x02	Incoming Mailbox Reg 3
0x03	Incoming Mailbox Reg 4
0x04	Outgoing Mailbox Reg 1
0x05	Outgoing Mailbox Reg 2
0x06	Outgoing Mailbox Reg 3
0x07	Outgoing Mailbox Reg 4
0x08	Add-on FIFO port
0x09	Bus master write Address Register
0x0A	Add-on Pass through Address
0x0B	Add-on Pass trough Data
0x0C	Bus master read Address Register
0x0D	Add-on Mailbox Empty/full Status
0x0E	Add-on Interrupt Control
0x0F	Add-on General Control/Status Register

Table 3.1: AMCC Registers (DSP)

For more information about these registers refer to the AMCC PCI controller manual.

3.3 DSP MEMORY AND REGISTER MAP SUMMARY

NAME	START	END	DATA	R/W	COMMENTS
SRAM	0x000000	0x01FFFF	D00-D31	R/W	Zero wait state static RAM
FLASH	0x400000	0x41FFFF	D00-D07	R/W	128K x 8 Protected
STAT1	0xF00001	0xF00001	D00-D03	R	Z85230 SCC Interrupt Status
IVEC1	0xF00008	0xF00008	D00-D07	R	SCC1 Interrupt Vector
IVEC2	0xF00009	0xF00009	D00-D07	R	SCC2 Interrrupt Vector
IVEC3	0xF0000A	0xF0000A	D00-D07	R	SCC3 Interrupt Vector
IVEC4	0xF0000B	0xF0000B	D00-D07	R	SCC4 Interrrupt Vector
SCC1	0xF00010	0xF00013	D00-D07	R/W	SCC1 Z85230
SCC2	0xF00014	0xF00017	D00-D07	R/W	SCC2 Z85230
SCC3	0xF00018	0xF0001B	D00-D07	R/W	SCC3 Z85230
SCC4	0xF0001C	0xF0001F	D00-D07	R/W	SCC4 Z85230
SCC8530	0xF00048	0xF0004C	D00-D07	R/W	System Console Port
AMCC	0xF00080	0xF000FF	D00-D31	R/W	AMCC REGISTERS

Table 3.2: DSP Memory Map

3.3.1 STAT1INTERRUPT STATUS REGISTER (Read Only)

BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 00
				SCC4 IREQ	SCC3 IREQ	SCC2 IREQ	SCC1 IREQ

Each Z85230 devices can generate and interrupt. When any SCC generates an interrupt, the corresponding interrupt is ORed with other pending interrupts. The DSP can read this register to determine which interrupts are pending.

3.3.2 SERIAL PORT (Read / Write)

The DSP processor on the **CPCI-ISC8** has access to an SCC85C30 serial communication controller. The 8530 provides an RS232C asynchronous serial communication port. Port B of the 8530 is not connected.

The bootloader and hardware support libraries supplied with the **CPCI-ISC8** utilizes the RS232C port for a console for standard input and output by the DSP. The customer may alternatively wish to write his own software to use this port. Examples are provided in the **Board Support Package**.

3.4 RESET SIGNALS

The **CPCI-ISC8** can be reset from two different sources:

- At power on or when the PCI RESET is asserted, the watchdog timer will hold the C31 RESET line low for 200 ms.
- The AMCC has a bit called SYSRST which the HOST can toggle to reset the DSP.
- Software should hold the RESET asserted for 200 mS .

3.5 LOCAL DSP INTERRUPT SOURCES

The local DSP has four interrupt lines. The source of each interrupt is listed in the table below. Additionally, at reset, the INT1 line is pulsed to tell the C31 to find the FLASH image at 0x400000 (if boot mode is MC).

SOURCE	ENABLE SIGNAL	INTERRUPT LEVEL
External Input	None	INT0
AMCC	Inside 5933	INT1
AMCC FIFO: WR not Full RD not Empty	None	INT2
SCC1 – SCC4 Z85230 Interrupts	Inside Z85230s	INT3

Table 3.5: Interrupt Sources

4. JUMPER DESCRIPTIONS

JUMPER	FACTORY SETTING	DESCRIPTION
W1	2-3	Connects the external interrupt signal EX_GPS to pull-up or pull-down resistors. W1 1-2 selects pull-up W1 2-3 selects pull-down
W2	2-3	Selects 16 MHz processor H1 or Oscillator U12 as PCLK source for all 8530 devices W2 1-2 selects U12 source W2 2-3 selects processor H1
W3	None	Routes the buffered U13 clock signal to each 85230 Receive Clock (RTXC) pin W3 1-2 RTXCA System Console Port W3 3-4 RTXCB SCC4 W3 5-6 RTXCA SCC4 W3 7-8 RTXCB SCC3 W3 9-10 RTXCA SCC3 W3 10-11 RTXCB SCC2 W3 12-13 RTXCA SCC2 W3 14-15 RTXCB SCC1 W3 16-17 RTXCA SCC1
W4	None	W4 1-2 Asserts Local Reset
W5	None	W5 1-2 Connects the DSP clock to the CompactPCI CLK pin. (used for standalone operation)
W6	None	W6 1-2 Connects the CompactPCI RST# signal to +5 via a 10K pullup. (used for standalone operation)
W7	None	Select falling or rising edge external interrupt mode. Use this jumper in conjunction with W1 as required.

Table 4.1 Jumper Descriptions

5. LED INDICATORS

There are two LED indicators visible at the CPCI card bracket. They are marked with a legend on the bracket, and they are labeled on the PCB as L1 – L2 where L1 is at the top of the card.

The LEDs have the following meanings:

LED	LEGEND	Meaning
L1	RD	DSP is reading a register in the AMCC.
L2	WR	DSP is writing a register in the AMCC.

Table 5.1 LED Descriptions

6. CONNECTIONS

6.1 IP I/O CONNECTORS (P9, P10)

Connector	I/O for
P9	Mezzanine I/O 1 1-50
P10	Mezzanine I/O 2 1-50

50 pin high density flat cable connectors are used to route all the IP I/O signals off the card. ALPHI Technology can supply transition modules and cable assemblies to meet any special requirements. Contact the factory for additional information.

Connectors are manufactured by HIROSE.

Use	Model
On PC Board	HIF6A-50PA-1.27DS
Suggested Plug	H1F6-50D-1.27R

Table 6.1: I/O Connector Model Numbers

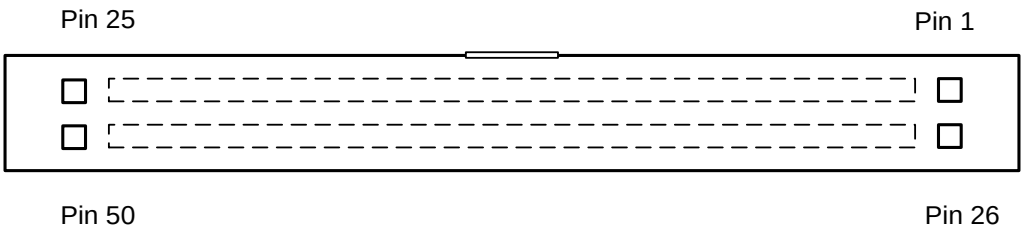

Figure 6.1: IP I/O CONNECTORS

The I/O signals for the mezzanone are directly routed off the card through the front panel.

6.2 SERIAL RS232 PORT (P3)

An 8 pin header is located on the PCB and is used to route the RS232 signals off the card. Port A of the 8530 is configured as an RS232 port, and serves as the console output for the bootloader and any DSP programs linked with the ALPHI_IO.LIB library discussed in the **DSP Support Library**. Port B is not connected.

The connector is a standard 2x8 pin header on 0.100 inch centers.

The pinout is described in the table below.

Pin	Description	Pin	Description
1	Request To Send	2	Transmit Data
3	Receive Data	4	Clear To Send
5	Ground	6	Ground
7	No Connection	8	No Connection

Table 6.2: Serial RS232 Port (P3)

6.3 EMULATOR CONNECTION (P4)

This connector is used to connect the emulator to the C31 DSP. It follows the standard form as described by TI in their processor manual.

6.4 FACTORY USE (P2)

This connector is used at the factory for programming the FPGA.

6.5 32 BIT CPCI BUS (P1)

This connector plugs into the backplane and provides the standard CPCI signals for all CPCI systems.

7. STANDALONE OPERATION

It is possible to operate the card is a stand-alone mode without a CPCI HOST. Install jumpers on W6 and W5. ALPHI TECHNOLOGY can supply an P1 adaptor to allow operation outside of a CompactPCI chassis or backplane. When the board is operated in stand alone mode, the board can by operated under an emulator and by downloading and executing programs via the serial port under control of the bootloader.