

CPCI-IPC

**Intelligent DSP Based
Dual IndustryPack[®] Carrier
for *CompactPCI*[™] systems**

REFERENCE MANUAL

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CPCI-IPC REFERENCE MANUAL

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1. GENERAL DESCRIPTION

1.1 INTRODUCTION

The **CPCI-IPC** is an intelligent DSP based IP carrier in a 3U CPCI form factor. The **CPCI-IPC** provides mechanical support and the electrical interfaces for two single width IP modules, or a double width IP module. Multiple **CPCI-IPC** boards may be installed in a single system. The primary features of the **CPCI-IPC** are as follows:

- Integrated DSP (TI TMS320C31) at 32 MHz to offload I/O operation from host or for standalone applications
- Support for up to two IP modules
- 8 MHz or 32 MHz IP operation via jumper selection
- Supports double-wide form factor IndustryPack®
- Direct memory mapped control of DSP from CPCI bus via AMCC 5933 PCI Chip
- Full interrupt support of host and DSP
- Front panel I/O connectors for all IPs

1.2 FUNCTIONAL DESCRIPTION

A functional block diagram of the **CPCI-IPC** is presented below in Figure 1-1. The jumper placement and the connector placement is depicted in Figure 1-2. The **CPCI-IPC** can operate as a slave that is managed by the host processor on the CPCI bus or it can operate in a standalone mode of operation without a host. Each pair of IP modules share a common clock that can be jumpered for 8 or 32 MHz operation.

The **CPCI-IPC** is supported by ALPHI Technology under *Windows NT* by a **Board Support Package** which is supplied with the card. Other documentation supplied with the card will describe this support in full detail.

The card is also supported by a **DSP Support Library** providing the following features:

- Common access routines for communications with the HOST
- Mapping C language standard input and output by each of the DSPs to the onboard 8530 serial chips
- Identify the applicable card resources and parameters

All these are provided in a manner consistent across ALPHI Technology platforms. Other documentation supplied with the card will describe the support in full detail.

A bootloader provided on the card allows for control by the HOST and for independent operation in stand alone operation. User code can be downloaded to FLASH memory and booted automatically on reset. Access to the card can be made both by the HOST CPCI bus and serially through the 8530.

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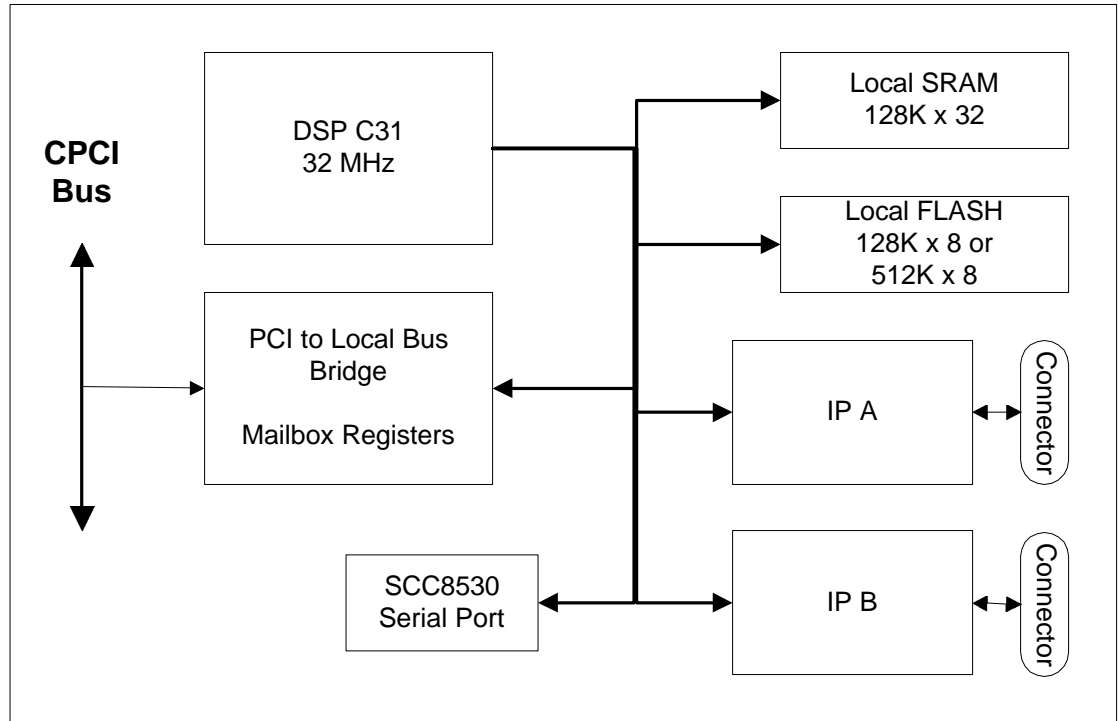


Figure 1.1: Block Diagram

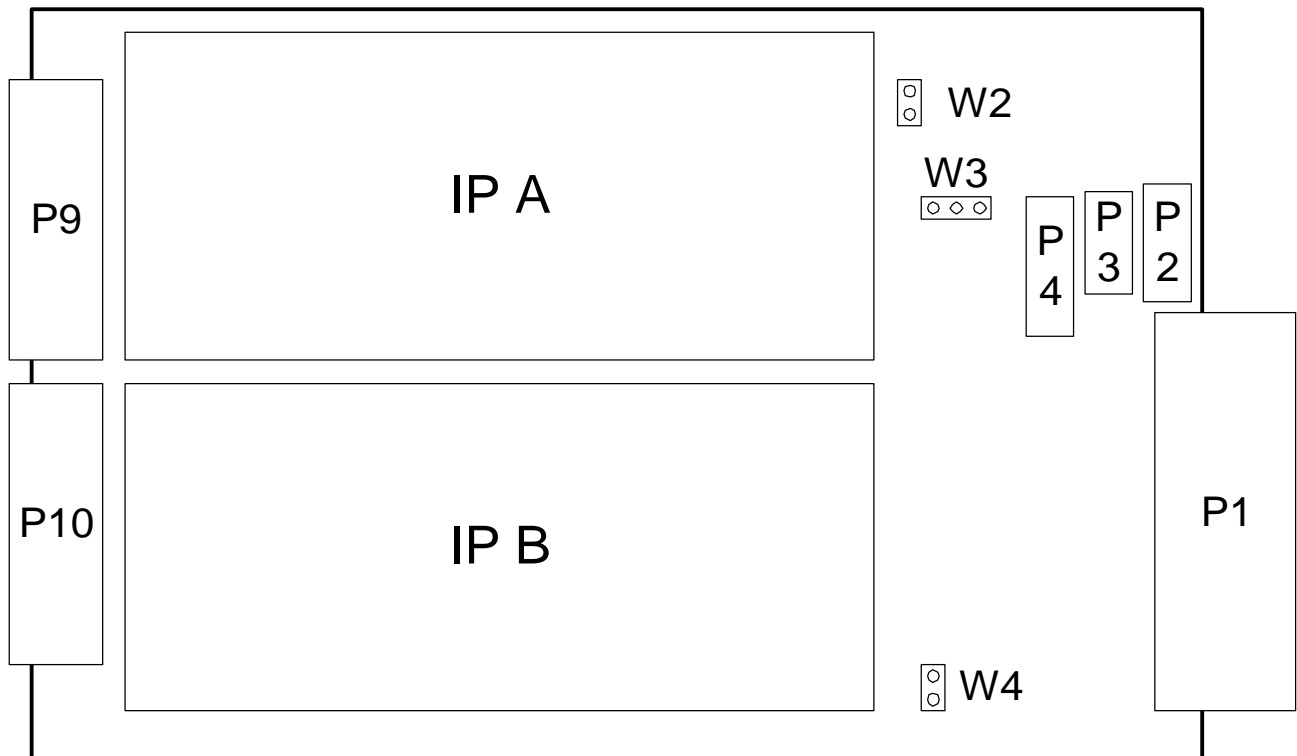


Figure 1.2: Jumper and Connector Locations

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1.3 REFERENCE MATERIALS LIST

The reader should refer to the PCI Local Bus Specification for a detailed explanation of the PCI bus architecture and timing requirements. This specification is available from the following source:

PCI Special Interest Group
PO Box 14070
Portland, OR 97214
Tel: (800) 433-5177
Tel: (503) 797-4207
Fax: (503) 234-6762

The reader is also referred to the S5933 PCI Controller data book:

AMCC Applied Micro Circuits Corporation
6195 Lusk Boulevard
San Diego, CA 92121-2793
Tel: (800) 755-2622
<http://www.amcc.com>

WindowsNT and Windows95 Programming Tools:

BlueWater Systems
144 Railroad Ave. Suite #217
Edmonds, WA 98020
Tel: (206) 771-3610
Fax: (206) 771-2742
E-Mail: info@bluewatersystems.com
Web: <http://www.bluewatersystems.com>

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2. HOST (CPCI) SIDE

2.1 PCI CONFIGURATION REGISTERS

The card presents the following configuration values to the CPCI system, based on the values stored in the NVRAM device read by the AMCC PCI interface chip.

Register	Value (Meaning)
Vendor ID	0x13c5 (ALPHI Technology)
Device ID	0x0101 (CPCI-IPC)
Revision ID	0x00
Class Code	0xff0000 (Device does not fit into defined class codes)
Interrupt Line	0xff
Interrupt Pin	A
Multifunction Device	No
Build In Self Test	No
Latency Timer	0x00
Minimum Grant	0x00
Maximum Latency	0x00
Expansion ROM Size	None

Table 2.1: CPCI Configuration Registers

2.2 PCI BASE ADDRESS REGISTERS

The card requests base address regions from the CPCI system after RESET, based on the values stored in the NVRAM device read by the AMCC PCI interface chip.

The decode addresses of these regions are assigned by the host processor. The **CPCI-IPC** uses 1 of the 5 AMCC mapped base address registers. The AMCC is normally programmed at the factory to request the following resource from the CPCI BIOS:

BAR	From	To	Description	Type
0	0x00000000	0x00000003F	AMCC PCI Operation Registers	MEM

Table 2.2: Base Address and Use

NOTE: The AMCC has been programmed to request memory above 1 Mbytes.

2.3 CPCI OPERATION REGISTERS

The host processor communicates with the **CPCI-IPC** card via the AMCC pass-through interface. After the base address register has been programmed by the CPCI configurator, incoming CPCI I/O or Memory cycles are used to access the registers of the AMCC chip. The PCI Operation Registers of the AMCC 5933 chip are depicted below:

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Offset	Register Name
0x00	OMB1 Outgoing Mailbox Register 1
0x04	OMB2 Outgoing Mailbox Register 2
0x08	OMB3 Outgoing Mailbox Register 3
0x0C	OMB4 Outgoing Mailbox Register 4
0x10	IMB1 Incoming Mailbox Register 1
0x14	IMB2 Incoming Mailbox Register 2
0x18	IMB3 Incoming Mailbox Register 3
0x1C	IMB4 Incoming Mailbox Register 4
0x20	FIFO Register Port (bi-directional)
0x24	MWAR Master Write Address Register
0x28	MWTC Master Write Transfer Counter
0x2C	MRAR Master Read Address Register
0x30	MRTC Master Read Transfer Counter
0x34	MBEF Mailbox Empty/Full Status
0x38	INTCSR Interrupt Control/Status Register
0x3C	MCSR Bus Master Control/Status Register

Table 2.3: AMCC Registers (HOST)

For more information about these registers refer to the AMCC PCI controller manual.

3. C31 SIDE

3.1 INTERNAL ORGANIZATION

The **CPCI-IPC** card is divided into different sections. Each section and its relationship to other sections will be discussed. The **CPCI-IPC** sections are:

- CPCI interface
- IP interface

3.2 CPCI INTERFACE

The local DSP processor communicates with the CPCI bus through the AMCCS9533 chip that provides bi-directional FIFO and Mailbox registers. The **CPCI-IPC** can function as both a servant (CPCI target) or as a master (CPCI initiator) for DMA access. The following interface descriptions refer to the CPCI interface as seen by the local DSP. The AMCC registers are located at DSP address 0xf00080.

3.2.1 BI-DIRECTIONAL FIFO

Two separate FIFO data paths are implemented within the AMCCS9533, a read FIFO that allows data transfers from the module to the CPCI bus and a write FIFO that transfers data from the CPCI to the module. Size of the FIFO is 32 bit X 8. Read and write DMA access to the host can occur via the FIFO registers if it is supported by the software on the HOST and

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is enabled. Alternatively, the FIFO registers can utilize a polled scheme on the HOST and DSP. Both FIFOs are accessed via access to the same location as seen by the DSP, offset 0x08.

3.2.2 MAILBOX REGISTERS

The Mailbox registers of the AMCCS9533 provide a bi-directional data path that can be used to send data or software control information between the HOST and DSP of that half of the **CPCI-IPC** module. Interrupts can be enabled based on a specific mailbox event. There are 4 incoming mailboxes and 4 outgoing mailboxes. Each mailbox is 32 bits wide. The address offsets for the mailboxes are shown below in Table 3-1.

3.2.3 ADDITIONAL REGISTERS

The AMCC S5933 PCI controller has a set of additional registers to control and monitor the behavior of the CPCI interface.

The address offsets of these registers are shown below in Table 3-1.

Offset	Register Name
0x00	Incoming Mailbox Reg 1
0x01	Incoming Mailbox Reg 2
0x02	Incoming Mailbox Reg 3
0x03	Incoming Mailbox Reg 4
0x04	Outgoing Mailbox Reg 1
0x05	Outgoing Mailbox Reg 2
0x06	Outgoing Mailbox Reg 3
0x07	Outgoing Mailbox Reg 4
0x08	Add-on FIFO port
0x09	Bus master write Address Register
0x0A	Add-on Pass through Address
0x0B	Add-on Pass through Data
0x0C	Bus master read Address Register
0x0D	Add-on Mailbox Empty/full Status
0x0E	Add-on Interrupt Control
0x0F	Add-on General Control/Status Register

Table 3.1: AMCC Registers (DSP)

For more information about these registers refer to the AMCC PCI controller manual.

3.3 IP INTERFACE and PAGED MEMORY

The ID and IO space for the IPs are directly accessed based on the memory map below. IP memory space is overlaid with the FLASH space, and is controlled via the register CTRL.

3.4 DSP MEMORY AND REGISTER MAP SUMMARY

NAME	START	END	DATA	R/W	COMMENTS
SRAM	0x000000	0x01FFFF	D00-D31	R/W	Zero wait state static RAM
FLASH	0x400000	0x41FFFF	D00-D07	R/W	128K x 8 Protected
IPMEMSL_A	0x400000	0x7FFFFFF	D00-D15	R/W	IP_A memory (8 Mbytes)
IPMEMSL_B	0x400000	0x7FFFFFF	D00-D15	R/W	IP_B memory (8 Mbytes)
CTRL	0xF00010	0xF00010	D00-D03	W	Controls internal settings
INTGNT_A	0xF00020	0xF00021	D00-D15	R	Interrupt vectors from IP_A
INTGNT_B	0xF00022	0xF00023	D00-D15	R	Interrupt vector from IP_B
C31_STAT	0xF00028	0xF00028	D00-D04	R	IP interrupt; Bus Error
BERR_RST	0xF00030	0xF00030	N/A	W	Reset Bus Error Status
IPSTROBE	0xF00038	0xF00038	N/A	W	Assert *IPSTROBE
SCC8530	0xF00048	0xF0004C	D00-D07	R/W	Serial communication port
AMCC	0xF00080	0xF000FF	D00-D31	R/W	AMCC REGISTERS
IOSEL_A	0xF00200	0xF0023F	D00-D15	R/W	IP_A I/O Space
IOSEL_B	0xF00240	0xF0027F	D00-D15	R/W	IP_B I/O Space
IDSEL_A	0xF00280	0xF002BF	D00-D15	R/W	IP_A ID Space
IDSEL_B	0xF002C0	0xF002FF	D00-D15	R/W	IP_B ID Space

Table 3.2: DSP Memory Map

3.4.1 CTRL (Write Only)

BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 00
				TCLK1_EN	BANKSEL	32BIT_AB	FLASH

TCLK1_EN **Signal routing to IPSTROBE**

See the following table for routing signals to *IPSTROBE.

TCLK1_EN,	Result
0	Connect DSP Timer 1 output to *IPSTROBE
1	Software writes to register IPSTROBE (0xF00038) output to *IPSTROBE

Table 3.3: IPSTROBE Connection

FLASH, BANKSEL **Memory Page Selection**

The FLASH and the two IP memory spaces are all paged into a common DSP address range starting at 0x400000. Selection of the appropriate page is accomplished by programming the FLASH and BANKSEL bits.

BANKSEL	FLASH	Page Selection
X	0	FLASH (default)
0	1	IP_A Memory Space
1	1	IP_B Memory Space

Table 3.4: Memory Page Selection

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32BIT_AB 32-bit Width Enable

Setting this bit to a one enables the IP interface A and B for 32-bit transfers. Setting this bit to a zero disables the 32-bit transfers (default setting). This bit must be set to a one when using a double width IP. Note that the DSP always reads or writes in 32-bits, however only the lower 16 bits are valid when 32BIT_AB = 0.

3.4.2 C31_STAT INTERRUPT STATUS REGISTER (Read Only)

BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 00
			CBERR	IP_B IREQ1	IP_B IREQ0	IP_A IREQ1	IP_A IREQ0

Each IP module can generate two different interrupts. When any Industry Pack generates an interrupt, the corresponding interrupt is ORed with other pending interrupts. The DSP can read this register to determine which interrupts are pending.

CBERR Bus Error Status

Any access to a non-existent IP will never complete since no device will assert *IPACK.

To prevent this from happening, and hanging the DSP, any access to an IP also starts a timer to ensure that the cycle completes. The fact that a cycle has timed out has occurred is reported in **C31_STAT**, and can be cleared by writing to **BERR_RST**.

The DSP C31 can read this bit to know that a access to an IP has not responded by asserting *IPACK. This status is reset with a write to **BERR_RST**.

This event will also cause a DSP interrupt, so any DSP interrupt routine which hooks the 8530 interrupt should be prepared to handle it (by at least writing to **BERR_RST**).

3.4.3 BERR_RST (Write Strobe Only)

A write to this location will reset the CBERR bit in the **C31_STAT** register.

3.4.4 IPSTROBE (Write Strobe Only)

If the **CTRL** Register is configured to allow it, a write to this location will trigger a pulse on the *IPSTROBE line to all the IPs.

3.4.5 SERIAL PORT (Read / Write)

The DSP processor on the **CPCI-IPC** has access to an SCC85C30 serial communication controller. The 8530 provides an RS232C asynchronous serial communication port. Port B of the 8530 is not connected.

The bootloader and hardware support libraries supplied with the **CPCI-IPC** utilizes the RS232C port for a console for standard input and output by the DSP. The customer may alternatively wish to write his own software to use this port. Examples are provided in the **Board Support Package**.

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3.5 RESET SIGNALS

The **CPCI-IPC** can be reset from two different sources:

- At power on or when the PCI RESET is asserted, the watchdog timer will hold the C31 RESET line and the IP reset lines low for 200 ms.
- The AMCC has a bit called SYSRST which the HOST can toggle to reset the DSP and IP resets. Software should hold the RESET asserted for 200 mS to meet the IP specifications

3.6 LOCAL DSP INTERRUPT SOURCES

The local DSP has four interrupt lines. The source of each interrupt is listed in the table below. Additionally, at reset, the INT1 line is pulsed to tell the C31 to find the FLASH image at 0x400000 (if boot mode is MC).

SOURCE	ENABLE SIGNAL	INTERRUPT LEVEL
SCC8530	Inside SCC8530	INT0
Bus Error	None	INT0
AMCC	Inside 5933	INT1
AMCC FIFO: WR not Full RD not Empty	None	INT2
IP interrupt	None	INT3

Table 3.5: Interrupt Sources

4. JUMPER DESCRIPTIONS

JUMPER	FACTORY SETTING	DESCRIPTION
W2	None	DSP Boot Mode: MC/~MP. The DSP's boot mechanism is designed to operate in MC mode, booting from the FLASH.
W3	2-3	IP A, B Clock Speed. 1-2 for 32 MHz, 2-3 for 8 MHz. 8 MHz is default.
W4	None	When shorted, provides DSP and IP reset.

Table 4.1 Jumper Descriptions

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5. LED INDICATORS

There are four LED indicators visible at the CPCI card bracket. They are marked with a legend on the bracket, and they are labeled on the PCB as L1 – L4 where L1 is at the top of the card.

The LEDs have the following meanings:

LED	LEGEND	Meaning
L1	RD	DSP is reading a register in the AMCC.
L2	IP B	DSP is accessing IP B.
L3	WR	DSP is writing a register in the AMCC.
L4	IP A	DSP is accessing IP A.

Table 5.1 LED Descriptions

6. CONNECTIONS

6.1 IP I/O CONNECTORS (P9, P10)

Connector	I/O for
P9	IP_A
P10	IP_B

50 pin high density flat cable connectors are used to route all the IP I/O signals off the card. ALPHI Technology can supply transition modules and cable assemblies to meet any special requirements. Contact the factory for additional information.

Connectors are manufactured by HIROSE.

Use	Model
On PC Board	HIF6A-50PA-1.27DS
Suggested Plug	H1F6-50D-1.27R

Table 6.1: I/O Connector Model Numbers

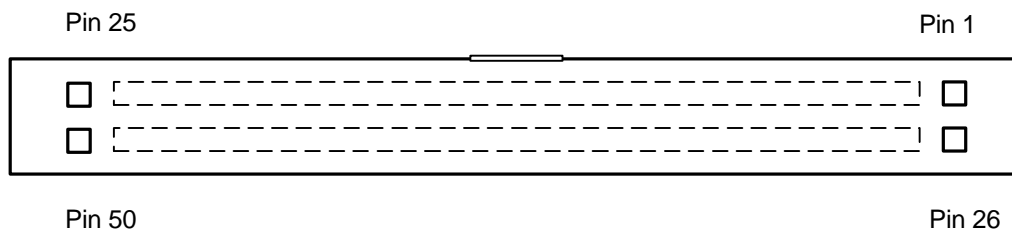


Figure 6.1: IP I/O CONNECTORS

The I/O signals for the two IPs are directly routed off the card through the front panel.

6.2 SERIAL RS232 PORT (P3)

An 8 pin header is located on the PCB and is used to route the RS232 signals off the card. Port A of the 8530 is configured as an RS232 port, and serves as the console output for the

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bootloader and any DSP programs linked with the ALPHI_IO.LIB library discussed in the **DSP Support Library**. Port B is not connected.

The connector is a standard 2x8 pin header on 0.100 inch centers.

The pinout is described in the table below.

Pin	Description	Pin	Description
1	Request To Send	2	Transmit Data
3	Receive Data	4	Clear To Send
5	Ground	6	Ground
7	No Connection	8	No Connection

Table 6.2: Serial RS232 Port (P3)

6.3 EMULATOR CONNECTION (P4)

This connector is used to connect the emulator to the C31 DSP. It follows the standard form as described by TI in their processor manual.

6.4 FACTORY USE (P2)

This connector is used at the factory for programming the FPGA.

6.5 32 BIT CPCI BUS (P1)

This connector plugs into the backplane and provides the standard CPCI signals for all CPCI systems.

7. STANDALONE OPERATION

It is possible to operate the card in a stand-alone mode without a CPCI HOST. Contact the factory for more details.

When the board is operated in stand alone mode, the board can be operated under an emulator and by downloading and executing programs via the serial port under control of the bootloader.