CPCI-ADDA

Intelligent Analog I/O
Quad 16 bit A/D and D/A with Digital I/O
for *CompactCPCI*™ systems

REFERENCE MANUAL

721-20-000-4000
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Part Number : 721-20-000-4000

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1. GENERAL DESCRIPTION

1.1 INTRODUCTION

The **CPCI-ADDA** is a 3U CPCI expansion card with a variety of types of input and output. Multiple **CPCI-ADDA** boards may be installed in a single system. The primary features of the **CPCI-ADDA** are as follows:

- DSP (TI TMS320C31) running at 32 MHz
- Four 16 bit 10 uS A/D converters with digitally controlled gain and with selectable differential or single ended inputs.
- Four 16 bit D/A converters with buffered outputs.
- Eight TTL digital inputs with internal pullups.
- Eight TTL digital outputs.
- Dual RS-232 serial ports, one with front panel connections.
- Direct memory mapped access to the DSP from CPCI bus via AMCC 5933 PCI Chip
- Full interrupt support of host and DSP
- Front panel I/O connectors

1.2 FUNCTIONAL DESCRIPTION

A functional block diagram of the **CPCI-ADDA** is presented below in Figure 1-1. The jumper and connector placement is depicted in Figure 1-2. The **CPCI-ADDA** can operate as a slave that is managed by the host processor on the CPCI bus or it can operate in a stand-alone mode of operation without a host.

The **CPCI-ADDA** is supported by ALPHI Technology under *Windows NT* by a **Board Support Package** which is supplied with the card. Other documentation supplied with the card will describe this support in full detail.

The card is also supported by a **DSP Support Library** providing the following features:

- Common access routines for communications with the host
- Mapping C language standard input and output by the DSP to the onboard 8530 serial chip
- Identify the applicable card resources and parameters

All these are provided in a manner consistent across ALPHI Technology platforms. Other documentation supplied with the card will describe the support in full detail.

A bootloader provided on the card allows for control by the HOST and for independent operation in stand alone operation. User code can be downloaded to FLASH memory and booted automatically on reset. Access to the card can be made both by the HOST CPCI bus and serially through the 8530.

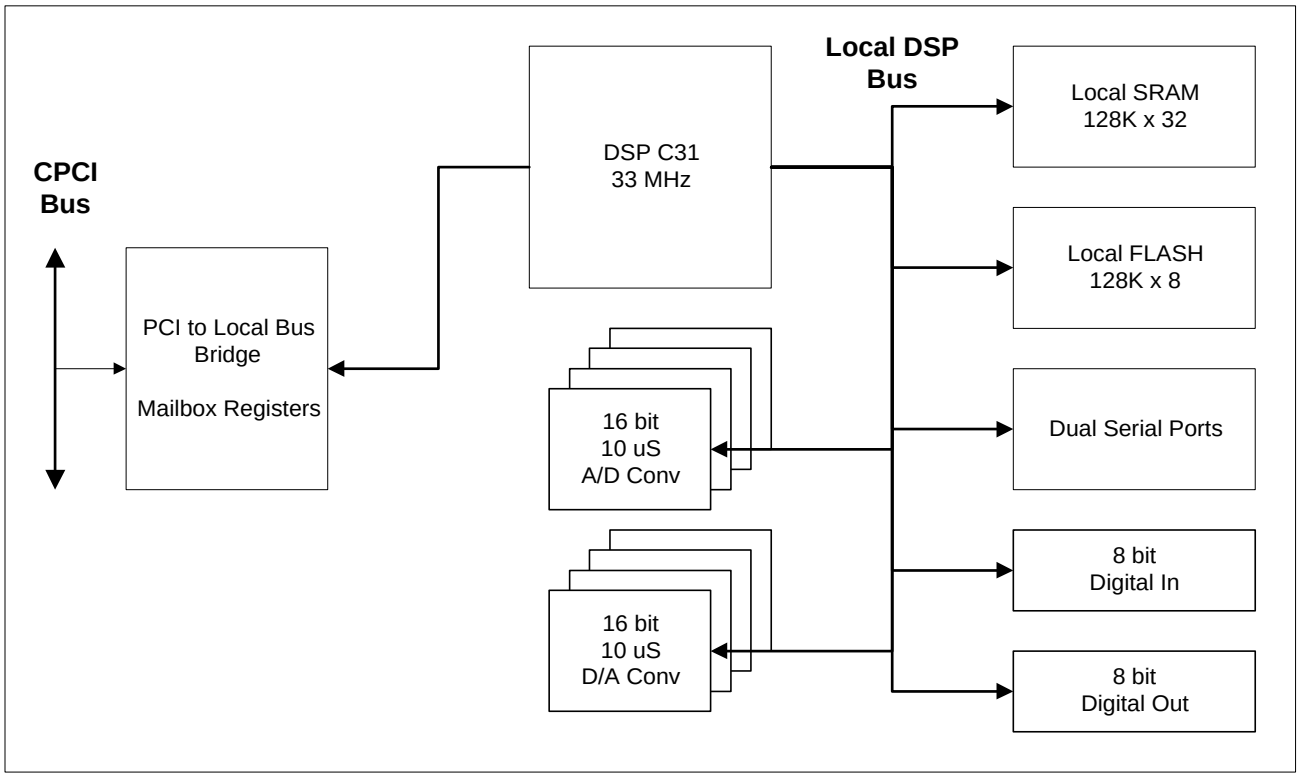

Figure 1.1: Block Diagram

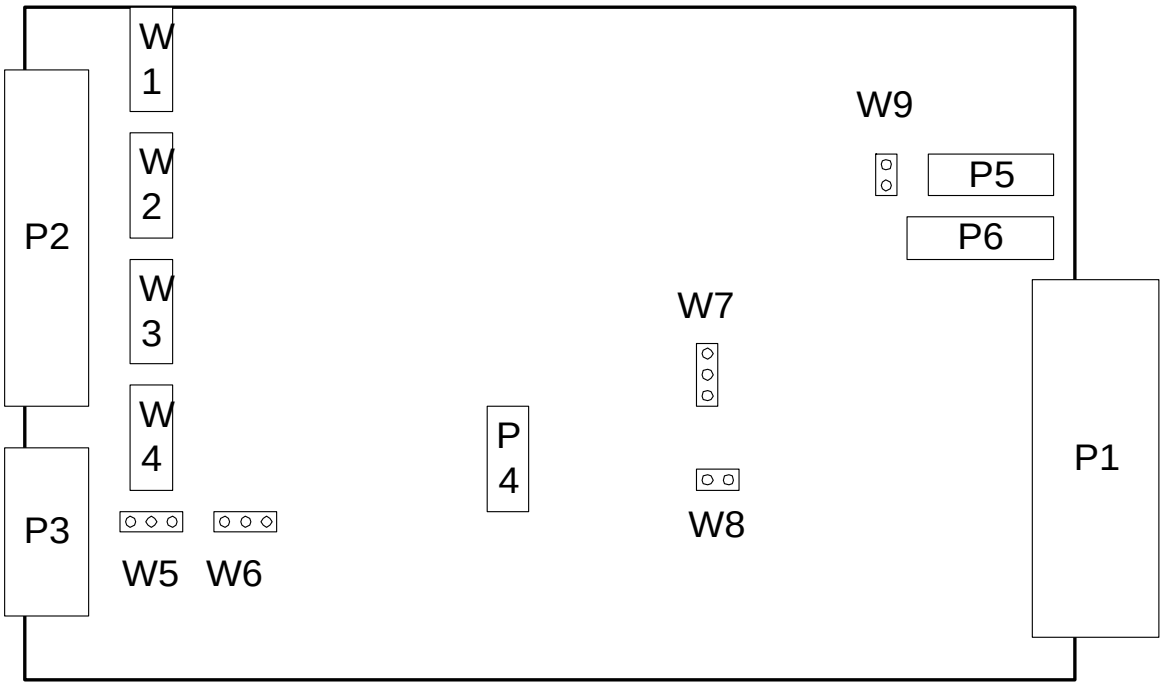

Figure 1.2: Jumper and Connector Locations

1.3 REFERENCE MATERIALS LIST

The reader should refer to the PCI Local Bus Specification for a detailed explanation of the PCI bus architecture and timing requirements. This specification is available from the following source:

PCI Special Interest Group
PO Box 14070
Portland, OR 97214
Tel: (800) 433-5177
Tel: (503) 797-4207
Fax: (503) 234-6762

The reader is also referred to the S5933 PCI Controller data book:

AMCC Applied Micro Circuits Corporation
6195 Lusk Boulevard
San Diego, CA 92121-2793
Tel: (800) 755-2622
http://www.amcc.com

WindowsNT and Windows95 Programming Tools:

BlueWater Systems
144 Railroad Ave. Suite #217
Edmonds, WA 98020
Tel: (206) 771-3610
Fax: (206) 771-2742
E-Mail: info@bluewatersystems.com
Web: http://www.bluewatersystems.com

2. HOST (CPCI) SIDE

2.1 CPCI CONFIGURATION REGISTERS

The card presents the following configuration values to the CPCI system, based on the values stored in the NVRAM device read by the AMCC PCI interface chip.

Register	Value (Meaning)
Vendor ID	0x13c5 (ALPHI Technology)
Device ID	0x0105 (CPCI-ADDA)
Revision ID	0x00
Class Code	0xff0000 (Device does not fit into defined class codes)
Interrupt Line	0xff
Interrupt Pin	A
Multifunction Device	No
Build In Self Test	No
Latency Timer	0x00
Minimum Grant	0x00
Maximum Latency	0x00
Expansion ROM Size	None

Table 2.1: CPCI Configuration Registers

2.2 CPCI BASE ADDRESS REGISTERS

The card requests base address regions from the CPCI system after RESET, based on the values stored in the NVRAM device read by the AMCC PCI interface chip.

The decode addresses of these regions are assigned by the host processor. The **CPCI-ADDA** uses only 1 of the 5 AMCC mapped base address registers. The AMCC is normally programmed at the factory to request the following resource from the CPCI BIOS:

BAR	From	To	Description	Type
0	0x00000000	0x00000003F	AMCC PCI Operation Registers	MEM

Table 2.2: Base Address and Use

NOTE: The AMCC has been programmed to request memory above 1 Mbytes.

2.3 CPCI OPERATION REGISTERS

The host processor communicates with the **CPCI-ADDA** module via the AMCC pass-through interface. After the base address registers have been programmed by the CPCI configurator, incoming CPCI I/O or Memory cycles are translated into accesses to the AMCC chip. The CPCI Operation Registers of the AMCC 5933 chip are depicted below:

Offset	Register Name
0x00	OMB1 Outgoing Mailbox Register 1
0x04	OMB2 Outgoing Mailbox Register 2
0x08	OMB3 Outgoing Mailbox Register 3
0x0C	OMB4 Outgoing Mailbox Register 4
0x10	IMB1 Incoming Mailbox Register 1
0x14	IMB2 Incoming Mailbox Register 2
0x18	IMB3 Incoming Mailbox Register 3
0x1C	IMB4 Incoming Mailbox Register 4
0x20	FIFO Register Port (bi-directional)
0x24	MWAR Master Write Address Register
0x28	MWTC Master Write Transfer Counter
0x2C	MRAR Master Read Address Register
0x30	MRTC Master Read Transfer Counter
0x34	MBEF Mailbox Empty/Full Status
0x38	INTCSR Interrupt Control/Status Register
0x3C	MCSR Bus Master Control/Status Register

Table 2.3: AMCC Registers (HOST)

For more information about these registers refer to the AMCC PCI controller manual.

3. C31 SIDE

3.1 INTERNAL ORGANIZATION

The **CPCI-ADDA** card is divided into different sections. Each section and its relationship to other sections will be discussed. The **CPCI-ADDA** sections are:

- CPCI interface
- Analog input
- Analog output
- Digital input and output

3.2 CPCI INTERFACE

The local DSP processor communicates with the CPCI bus through the AMCCS9533 chip that provides bi-directional FIFO and Mailbox registers. The **CPCI-ADDA** can function as both a servant (PCI target) or as a master (PCI initiator) for DMA access. The following interface descriptions refer to the CPCI interface as seen by the local DSP. The AMCC registers are located at DSP address 0xf00080.

3.2.1 BI-DIRECTIONAL FIFO

Two separate FIFO data paths are implemented within the AMCCS9533, a read FIFO that allows data transfers from the module to the CPCI bus and a write FIFO that transfers data from the CPCI to the module. Size of the FIFO is 32 bit X 8. Read and write DMA access to

the host can occur via the FIFO registers if it is supported by the software on the HOST and is enabled. Alternatively, the FIFO registers can utilize a polled scheme on the HOST and DSP. Both FIFOs are accessed via access to the same location as seen by the DSP, offset 0x08.

3.2.2 MAILBOX REGISTERS

The Mailbox registers of the AMCCS9533 provide a bi-directional data path that can be used to send data or software control information between the HOST and the **CPCI-ADDA** module. Interrupts can be enabled based on a specific mailbox event. There are 4 incoming mailboxes and 4 outgoing mailboxes. Each mailbox is 32 bits wide. The address offsets for the mailboxes are shown below in Table 3-1.

3.2.3 ADDITIONAL REGISTERS

The AMCCS5933 PCI controller has a set of additional registers to control and monitor the behavior of the CPCI interface.

The address offsets of these registers are shown below in Table 3-1.

Offset	Register Name
0x00	Incoming Mailbox Reg 1
0x01	Incoming Mailbox Reg 2
0x02	Incoming Mailbox Reg 3
0x03	Incoming Mailbox Reg 4
0x04	Outgoing Mailbox Reg 1
0x05	Outgoing Mailbox Reg 2
0x06	Outgoing Mailbox Reg 3
0x07	Outgoing Mailbox Reg 4
0x08	Add-on FIFO port
0x09	Bus master write Address Register
0x0A	Add-on Pass through Address
0x0B	Add-on Pass trough Data
0x0C	Bus master read Address Register
0x0D	Add-on Mailbox Empty/full Status
0x0E	Add-on Interrupt Control
0x0F	Add-on General Control/Status Register

Table 3.1: AMCC Registers (DSP)

For more information about these registers refer to the AMCC PCI controller manual.

3.3 ANALOG INPUT

The **CPCI-ADDA** has four analog inputs each with its own 10 uS 16 bit A/D converter. An instrumentation amplifier conditions each input signal with digitally programmed gains selected by a DSP register. Several input modes are selectable, including full differential, and single ended. The inputs are +/- 10 Volts.

The A/D converters can be powered by the +/- 12 volts available from the CPCI bus, or by an externally provided +/- 15 volts supply.

The instrumentation amplifier also provides over-voltage protection to the input circuits.

3.3.1 Input Mode

The four analog inputs can operate in one of several modes, depending upon the jumper selections at the inputs. These jumpers are labeled W1 – W4 and correspond to channels 1 through 4 respectively. If selected, the return path is through a 10 Megohm resistor to local ground.

Input Mode	Jumpers
Full Differential	1-2
Full Differential with Return Path	1-2, 5-6
Single Ended referenced to Local (card) Ground	7-8
Single Ended referenced to Remote Ground (RG)	3-4
Single Ended referenced to Remote Ground (RG) with Return Path	3-4, 5-6

Table 3.2: Input Mode Selection

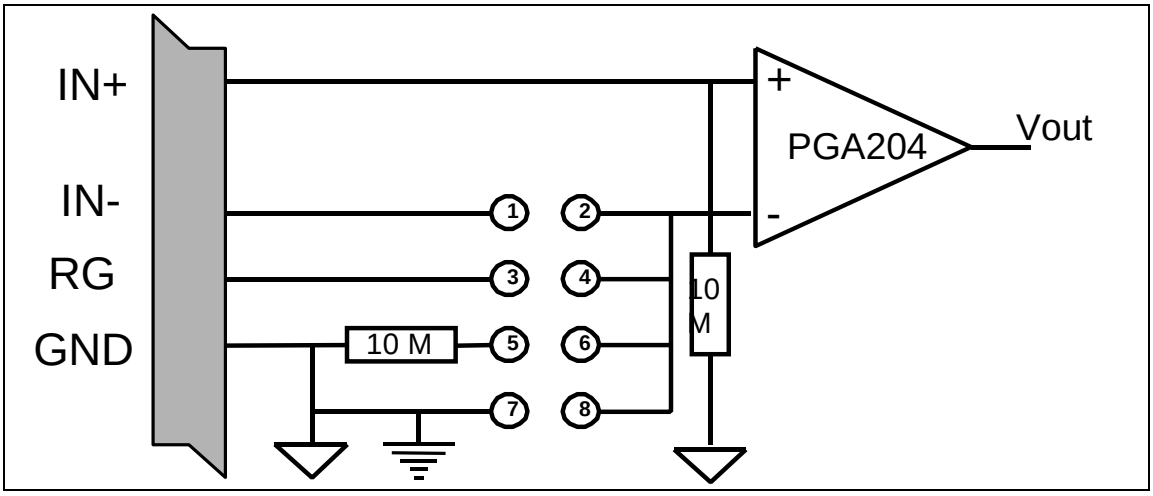

Figure 3.1: Input Equivalent Circuit

3.3.2 Gain Selection

The instrumentation amplifier gains are easily set by the DSP through the **AD_GAIN** register. The gains can be set to 1, 10, 100, or 1000. See the description of the **AD_GAIN** register for more details.

3.3.3 Conversion

The four 16 bit A/D converters can be clocked from the following sources:

- Internal sampling clock provided by DSP timer 1 (output on **SAMPLE_CLK_OUT**)
- External sampling clock provided on **SAMPLE_CLK_IN**.
- Triggered by the DSP writing to **SAMPLE_AD**

The DSP will be interrupted on INT2 when the conversions are complete.

The data is read from two 32 bit registers, **AD_DATA_12** and **AD_DATA_34** with one channel in the low WORD and the other in the high WORD.

3.4 ANALOG OUTPUT

The **CPCI-ADDA** has four 16 bit D/A converters and high current drivers for analog outputs. The drivers are capable of supplying up to 250 mA and are designed to directly drive inductive loads. The outputs are +/- 10 Volts.

3.4.1 Conversion

There are four output registers (**DA_DATA_1** to **DA_DATA_4**) accessible by the DSP. The D/A outputs are immediately updated when the DSP writes to the registers. If it is desired to clock the converters at a specific rate, either DSP timer 0 can provide an internal timebase interrupt, or the **EXT_INTERRUPT** can generate a DSP interrupt from an external clock.

3.4.2 Reset

The four D/A converters can be reset to a 0 voltage output by one of the following means:

- The DSP writes to DA_RESET register
- An external source drives **EXT_RESET_DA** low, when the ***EXT_RST_DA_EN*** bit is set to 1.

Additionally, if the ***EXT_RST_DA_EN*** and ***EXT_RST_DA_INT_EN*** bits are set to 1, a DSP interrupt can be generated.

3.5 DIGITAL INPUT AND OUTPUT

There is an 8 bit TTL compatible digital input port and an 8 bit TTL compatible digital output port. There is 22 K of internal pullup on the digital inputs.

3.6 LOCAL MEMORY AND REGISTER MAP SUMMARY

NAME	START	END	DATA	R/W	COMMENTS
SRAM	0x000000	0x01FFFF	D00-D31	R/W	Zero wait state static RAM
FLASH	0x400000	0x41FFFF	D00-D07	R/W	Software write protected
DA_DATA_1	0xF00000	0xF00000	D00-D15	W	D/A Channel 1
DA_DATA_2	0xF00001	0xF00001	D00-D15	W	D/A Channel 2
DA_DATA_3	0xF00002	0xF00002	D00-D15	W	D/A Channel 3
DA_DATA_4	0xF00003	0xF00003	D00-D15	W	D/A Channel 4
DA_RESET	0xF00018	0xF00018	N/A	W	Reset D/A Channels
CTRL1	0xF00020	0xF00020	D00-D03	R/W	Controls internal settings
CTRL2	0xF00021	0xF00021	D00-D03	R/W	Controls internal settings
SAMPLE_AD	0xF00038	0xF00038	N/A	R	Start A/D Conversion
AD_DATA_12	0xF00040	0xF00040	D00-D31	R	A/D Channels 1 and 2
AD_GAIN	0xF00040	0xF00040	D00-D07	W	Input Gains
AD_DATA_34	0xF00041	0xF00041	D00-D31	R	A/D Channels 3 and 4
DOUT	0xF00041	0xF00041	D00-D07	W	Digital Output
DIN	0xF00042	0xF00042	D00-D07	R	Digital Input
SCC8530	0xF00048	0xF0004B	D00-D07	R/W	Serial communication ports
AMCC	0xF00080	0xF0008F	D00-D31	R/W	AMCC REGISTERS

Table 3.3: DSP Memory Map

3.6.1 DA_DATA_1 to DA_DATA_4 (Write only)

These registers immediately update the output D/A converter to the written value. A count of 0x7FFF represents +10 V (if the input gain is 1), and a count of 0x8000 represents –10 V.

3.6.2 DA_RESET (Write strobe only)

When the DSP writes to this location, the D/A converters are reset to 0x0000 with a 0 voltage output.

3.6.3 CTRL1 (Read / Write)

BIT 03	BIT 02	BIT 01	BIT 00
EXT_RST_DA_INT_EN	EXT_RST_DA_EN	EXT_INT_EN	EXT_SAMP_CLK_EN

EXT_SAMP_CLK_EN ***Enable External Sampling Clock***

When this bit is set to 1, a rising edge on **SAMPLE_CLK_IN** will trigger the A/D converters in addition to the selection of the bit ***INT_SAMP_CLK_EN*** in **CTRL2**. When this bit is 0, the **SAMPLE_CLK_IN** line is ignored.

EXT_INT_EN ***Enable External Interrupt***

When this bit is set to 1, a falling edge on **EXT_INTERRUPT** will trigger a DSP interrupt on line INT0. When this bit is 0, the **EXT_INTERRUPT** line is ignored.

EXT_RST_DA_EN ***Enable External DAC Reset***

When this bit is set to 1, a falling edge on **EXT_RESET_DA** will reset the DAC outputs. When this bit is 0, no reset occurs.

EXT_RST_DA_INT_EN ***Enable Interrupt On External DAC Reset***

When this bit is set to 1, a falling edge on **EXT_RESET_DA** will trigger a DSP interrupt on line INT0. When this bit is 0, no interrupt occurs.

3.6.4 CTRL2 (Read / Write)

BIT 03	BIT 02	BIT 01	BIT 00
EXT_RESET_DA	INT_SAMP_CLK_EN	EXT_INTERRUPT	EXT_RESET_DA_INT

EXT_RESET_DA_INT ***INT0 Caused by* EXT_RESET_DA**

If this bit reads as 1, then the interrupt 0 was caused by the **EXT_RESET_DA** line This bit will remain a 1 until cleared by writing a 1 to this bit. Writing a 0 will not affect it. Note that this bit must be cleared in the interrupt routine, or no further interrupts will be received.

EXT_INTERRUPT ***INT0 Caused by* EXT_INTERRUPT**

If this bit reads as 1, then the interrupt 0 was caused by the **EXT_INTERRUPT** line This bit will remain a 1 until cleared by writing a 1 to this bit. Writing a 0 will not affect it. Note that this bit must be cleared in the interrupt routine, or no further interrupts will be received.

INT_SAMP_CLK_EN ***Enable Internal Sampling Clock***

When this bit is set to 1, the DSP timer 1 output will trigger the sampling and conversion of the A/D converters. When this bit is 0, a DSP write to the register **SAMPLE_AD** will trigger a conversion.

The DSP timer 1 output is always output upon **SAMPLE_CLK_OUT** regardless of this bit.

EXT_RESET_DA ***Current State of the* EXT_RESET_DA *line***

Current state of the **EXT_RESET_DA** line from P2.

3.6.5 SAMPLE_AD (Write strobe only)

A write to this location will trigger a conversion of the four A/D converters, if ***INT_SAMP_CLK_EN*** is cleared to 0.

3.6.6 AD_GAIN (Write only)

BIT 07	BIT 06	BIT 05	BIT04	BIT 03	BIT 02	BIT 01	BIT 00
AING4_1	AING4_0	AING3_1	AING3_0	AING2_1	AING2_0	AING1_1	AING1_1

This register sets the input gains for the four analog inputs based on the following table:

AINGx_1	AINGx_0	Gain
0	0	1
0	1	10
1	0	100
1	1	1000

Table 3.4: Input Gain Selections

3.6.7 AD_DATA_12 (Read only)

BITS 31 - 16	BITS 15 - 0
A/D 1 Data	A/D 2 Data

This 32 bit register contains the results from both input converters. Each result is a 16 bit 2's complement integer. A count of 0x7FFF represents +10 V (if the input gain is 1), and a count of 0x8000 represents –10 V.

3.6.8 AD_DATA_34 (Read only)

BITS 31 - 16	BITS 15 - 0
A/D 3 Data	A/D 4 Data

This 32 bit register contains the results from both input converters. Each result is a 16 bit 2's complement integer. A count of 0x7FFF represents +10 V (if the input gain is 1), and a count of 0x8000 represents –10 V.

3.6.9 DOUT (Write only)

BIT 07	BIT 06	BIT 05	BIT04	BIT 03	BIT 02	BIT 01	BIT 00
DOUT07	DOUT06	DOUT05	DOUT04	DOUT03	DOUT02	DOUT01	DOUT00

This register is directly output to the digital outputs available at the front panel connector.

3.6.10 DIN (Read only)

BIT 07	BIT 06	BIT 05	BIT04	BIT 03	BIT 02	BIT 01	BIT 00
DIN07	DIN06	DIN05	DIN04	DIN03	DIN02	DIN01	DIN00

This register returns the signal levels present at the front panel connector.

3.6.11 SERIAL PORT (Read / Write)

The DSP processor on the **CPCI-ADDA** has access to a SCC85C30 serial communication controller. The 8530 provides two RS232C asynchronous serial communication ports.

The bootloader and hardware support libraries supplied with the **CPCI-ADDA** utilizes the RS232C port for a console for standard input and output by the DSP. The customer may alternatively wish to write his own software to use this port. Examples are provided in the **Board Support Package**.

3.7 RESET SIGNALS

The **CPCI-ADDA** can be reset from two different sources:

- At power on, the watchdog timer will hold the C31 RESET line low for 200 ms.
- The AMCC has a bit called SYSRST which the HOST can toggle to reset the DSP.

3.8 LOCAL DSP INTERRUPT SOURCES

The local DSP has four interrupt lines with the sources listed in the table below. At reset, the INT1 line is pulsed to tell the C31 to find the FLASH image at 0x400000 (if boot mode is MC). If an interrupt is desired at the start of conversion, and the sample clock is generated internally in DSP timer 1, create a software routine to process the interrupt from that timer.

SOURCE	ENABLE BIT	STATUS BIT	LINE
SCC8530	Inside SCC8530	Inside SCC8530	INT0
EXT_INTERRUPT	***EXT_INT_EN***	***EXT_INTERRUPT***	INT0
EXT_RESET_DA	***EXT_RST_DA_INT_EN***	***EXT_RESET_DA_INT***	INT0
AMCC	Inside 5933	Inside 5933	INT1
A/D Conversions Complete	None	None	INT2
SAMPLE_CLK_IN	None	None	INT3

Table 3.5: Interrupt Sources and Enables

4. JUMPER DESCRIPTIONS

JUMPER	FACTORY SETTING	DESCRIPTION
W1	1-2, 5-6	Analog Input Mode1. See section 3.3.1.
W2	1-2, 5-6	Analog Input Mode2. See section 3.3.1.
W3	1-2, 5-6	Analog Input Mode3. See section 3.3.1.
W4	1-2, 5-6	Analog Input Mode4. See section 3.3.1.
W5	2-3	Analog Power (pos): 1-2 for external +15V, 2-3 for CPCI bus power.
W6	2-3	Analog Power (neg): 1-2 for external –15V, 2-3 for CPCI bus power.
W7	2-3	DSP clock: 1-2 for CPCI bus, 2-3 for internal 32 MHz clock.
W8	None	When shorted, provides DSP reset.
W9	None	DSP Boot Mode: MC/~MP. The card's boot mechanism is designed to operate in MC mode, booting from the FLASH.

Table 4.1 Jumper Descriptions

5. LED INDICATORS

There are two LED indicators visible at the CPCI card bracket. They are not marked with a legend on the bracket, but the one on the left is L1.

The LEDs have the following meanings:

LED	Meaning
L1	A/D conversion is complete.
L2	DSP is accessing a register in the AMCC.

Table 5.1 LED Descriptions

6. CONNECTIONS

6.1 I/O CONNECTOR (P2)

A 50 pin connector is used to route all the analog and digital signals off the card. ALPHI Technology can supply transition modules and cable assemblies to meet any special requirements. Contact the factory for additional information.

Connectors are manufactured by AMP.

Use	Model
On PC Board	787190-5
Suggested Plug	749111-4

Table 6.1: I/O Connector Model Numbers

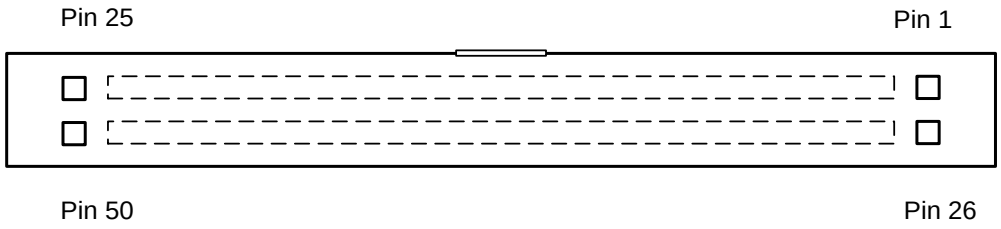

Figure 6.1: I/O CONNECTOR

Pin	Signal	Pin	Signal
1	D_GND	26	D_GND
2	DIN07	27	DOUT07
3	DIN06	28	DOUT06
4	DIN05	29	DOUT05
5	DIN04	30	DOUT04
6	DIN03	31	DOUT03
7	DIN02	32	DOUT02
8	DIN01	33	DOUT01
9	DIN00	34	DOUT00
10	D_GND	35	D_GND
11	EXT_RESET_DA	36	AOUT01
12	SAMPLE_CLK_OUT	37	A_GND
13	EXT_INTERRUPT	38	AOUT02
14	D_GND	39	A_GND
15	SAMPLE_CLK_IN	40	AOUT03
16	D_GND	41	A_GND
17	-15 V External	42	AOUT04
18	A_GND	43	REMOTE_GND
19	+15 V External	44	D_GND
20	A_GND	45	A_GND
21	AIN02 -	46	AIN04 -
22	AIN02 +	47	AIN04 +
23	A_GND	48	A_GND
24	AIN01 -	49	AIN03 -
25	AIN01 +	50	AIN03 +

Table 6.2: I/O Connections

6.2 SERIAL RS232 PORT (P3)

A 9 pin subminiature D shelled connector is used to route the 8530 port A signals off the card. Port A of the 8530 is configured as an RS232 port, and it serves as the console output for the bootloader and any DSP programs linked with the ALPHI_IO.LIB library discussed in the **DSP Support Library**.

Connectors are manufactured by ITT Cannon.

Use	Model
On PC Board	MDSM-9PE-C10
Suggested Plug	MDSM-9SC-Z11

Table 6.3: Serial Connector Model Numbers

The pinout is described in the table below.

Pin	Description	Pin	Description

1	No Connection	2	Transmit Data
3	Receive Data	4	Clear To Send
5	Ground	6	Request To Send
7	Ground	8	No Connection
9	No Connection		

Table 6.4: Serial RS232 Port (P3)

6.3 SERIAL RS232 PORT (P4)

Port B of the 8530 is configured as RS232 port, and is available for use by any DSP programs linked with the ALPHI_IO.LIB library discussed in the **DSP Support Library**. The connections are made to a header on the card and the pinout is described in the table below. An optional serial cable is available from the factory which connects to P4 and terminates in a 9 PIN D, suitable for connection to a computer or terminal.

Pin	Description	Pin	Description
1	No Connection	2	Request To Send
3	Transmit Data	4	Ground
5	Receive Data	6	No Connection
7	Clear To Send	8	No Connection
9	Ground	10	No Connection

Table 6.5: Serial RS232 Port (P4)

6.4 EMULATOR CONNECTION (P6)

This connector is used to connect the emulator to the C31 DSP. It follows the standard form as described by TI in their processor manual.

6.5 FACTORY USE (P5)

This connector is used at the factory for programming the FPGA.

6.6 32 BIT CPCI BUS (P1)

This connector plugs into the backplane and provides the standard CPCI signals for all CPCI systems.

7. STANDALONE OPERATION

It is possible to operate the card is a stand-alone mode without a CPCI HOST. Contact the factory for more details.

When the board is operated in stand alone mode, the board can by operated under an emulator and by downloading and executing programs via the serial port under control of the bootloader.