

# **CPCI-AD320**

**16-32 Channel High Performance  
Analog Data Acquisition Card  
for 6U *CompactPCI*™ systems**

## **REFERENCE MANUAL**

767-13-000-4000

Version 1.3

March 2001

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## **1. GENERAL DESCRIPTION**

### **1.1 INTRODUCTION**

The **CPCI-AD320** is a DSP based data acquisition and processing system, in a 6U CPCI form factor, targeted for general purpose analog data acquisition systems. The **CPCI-AD320** provides from 16 to 32 differential analog inputs (depending upon option ordered), with programmable gain, to individual A/D converters, operating at a maximum conversion rate of 200 kHz.

The **CPCI-AD320** is also a fully compatible PMC carrier for a single PMC module. Additional processing horsepower is available by adding an additional PMC module with DSP processing to the **CPCI-AD320**. Software control of this card is fully available to the on board DSP, any DSP or processor on the PMC module, as well as the HOST processor on the CPCI bus.

Connections to the input signals are available at the front panel and at the rear panel I/O connectors, and are fully supported by ALPHI Technology's line of Rear Panel I/O modules targeted towards data acquisition applications. In particular, the following modules are applicable:

- **RPIO-SGEX**: 8 channels of DC Bridge/Load Cell input.
- **RPIO-SGEX-M**: Additional 8 channels of DC Bridge/Load Cell input.
- **RPIO-CAL-M**: Adds bridge calibration, bridge completion, and monitoring of the excitation current for the 8 channels in the **RPIO-SGEX**.
- **RPIO-LVDT-SGEX**: 4 channels of LVDT signal conditioning and 4 channels of DC Bridge/Load Cell input.

Additionally, the **CPCI-AD320** is fully PXI compatible, and can make use of the PXI triggering signals to support synchronizing multiple boards.

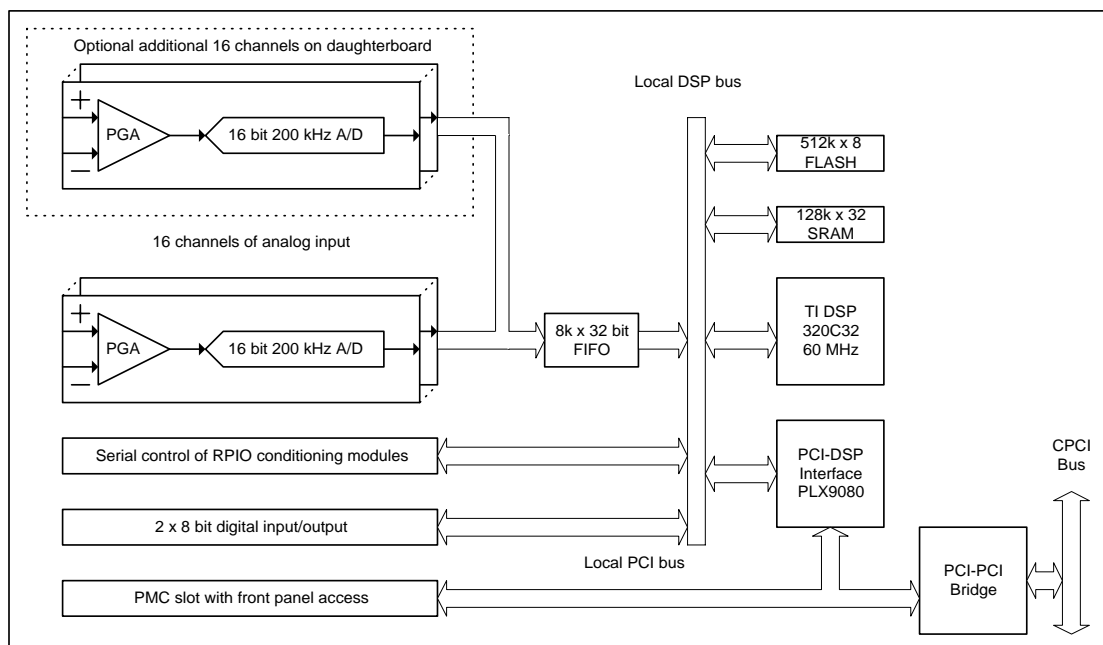
The primary features of the **CPCI-AD320** are as follows:

- 16-32 channels of simultaneous 16 bit A/D acquisition at 200 kHz.
- Integrated DSP (TI TMS320C32) at 60 MHz available to process the data, if desired, or to offload I/O operation from PMC processors or the HOST.
- 128K x 32 bit zero wait state SRAM for the DSP.
- 512K by 8 bit FLASH device for bootloader and customer applications.
- Programmable PGAs allow for gains of 1, 2, 4, or 8, or 1, 2, 5, or 10 on a per channel basis (determined at time of order ).
- Extremely flexible triggering, including internal, external, and PXI trigger/gate sources.
- Two channels of Bus Master DMA with Scatter/Gather support to offload the PMC and the HOST processor.
- Fully shared access to SRAM, card peripherals by HOST and PMC Processor.
- DSP is fully capable of accessing PMC, HOST RAM, and any other devices present on the CPCI bus
- 16 bits of digital input and output.

- 4 bits of digital output to control peripherals on the RPIO modules.
- One RS232 port and one RS422 port.
- Full software support including DSP code and Drivers/DLL for WinNT.

## 1.2 FUNCTIONAL DESCRIPTION

An overview block diagram of the **CPCI-AD320** is presented in Figure 1-1.



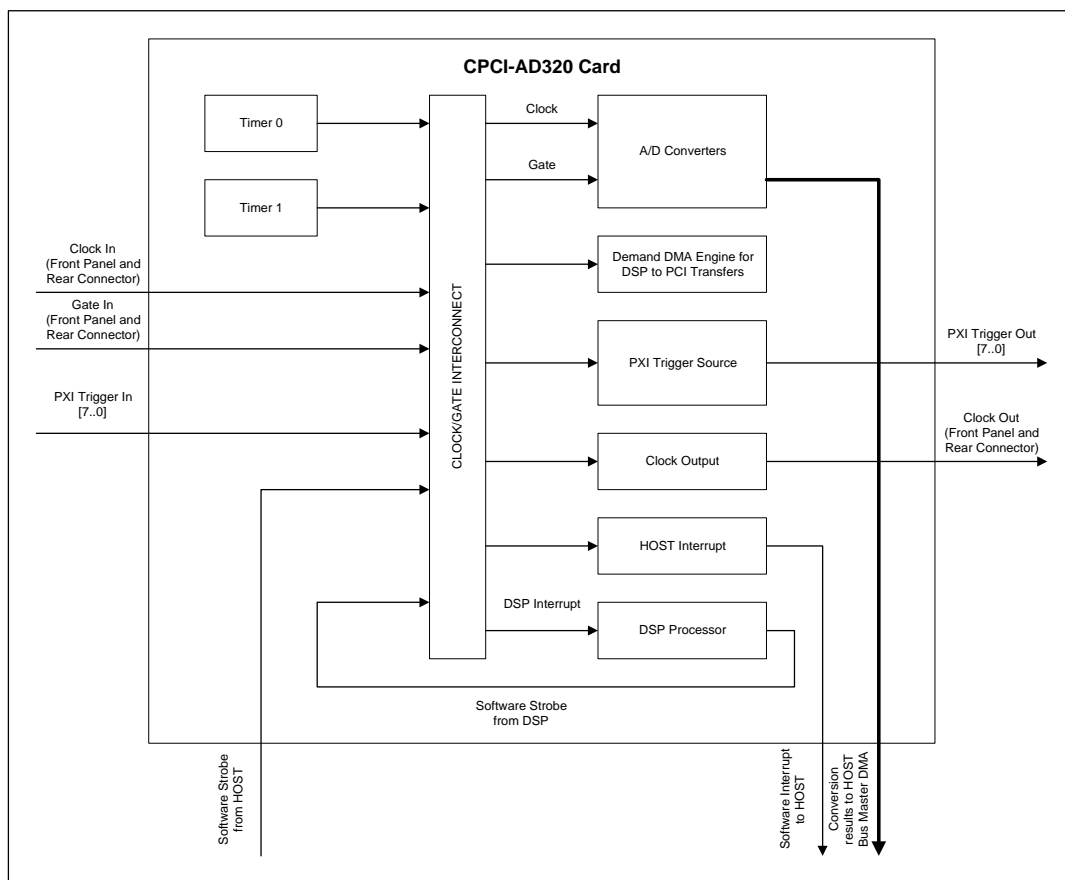
**Figure 1.1: Overview Block Diagram**

The CPCI to local PCI bridge completely isolates local PCI accesses between the PMC and this card from the main CPCI bus. This will allow high speed, low latency transfers to the PMC module.

There is full bi-directional access through the PCI to Local Bus bridge. The DSP can directly address and access memory on the HOST processor in addition to DMA. The HOST can directly access resources on the Local DSP bus.

## 1.3 TRIGGERING DESCRIPTION

The **CPCI-AD320** has extremely flexible triggering. The triggering clock / gate block diagram is presented in Figure 1-2.



**Figure 1.2: Trigger Clock / Gate Signal Block Diagram**

It is easier to describe the sources and targets separately. Any source can be connected to any target, except for the PXI Outputs which are described as a special case.

### 1.3.1 CLOCK / TRIGGER SOURCES

#### DSP Timers

There are two timers internal to the DSP which are capable of generating clock outputs. The outputs can be selected between positive or negative pulses, and square wave. Periods are multiples of 66.7 nS.

#### External TTL inputs

There are two front panel SMB connectors labeled Clock and Gate. The inputs are TTL compatible.

#### PXI Trigger Inputs

There are 8 PXI trigger lines, which may be used to synchronize multiple boards, provided that the other boards and the CPCI backplane are PXI compatible.

#### Trigger by DSP

The DSP can trigger a pulse by writing to a location in the registers.

### **Trigger by HOST**

The HOST can trigger a pulse by writing to a location in the registers.

### **Discrete Logic Level**

A forced 0 or 1 can be used as a source. This may be useful for the A/D Gate if the Gate functionality is not desired.

## **1.3.2 CLOCK/TRIGGER TARGETS**

These targets can be connected to any of the above sources.

### **A/D Converters**

The A/D converters are controlled by two signals: Clock and Gate. A rising edge on Clock will trigger the start of a conversion. Gate serves as a Clock qualifier, and must be high for Clock to be recognized.

### **Demand DMA Engine for DSP to PCI Transfers**

One of the two DSP to PCI bridge DMA engines can be operated in demand mode, transferring a fixed number of DWORDs based on a selected trigger signal.

### **External Clock Output**

There is a front panel SMB connector labeled Clock Output. The output is TTL compatible.

### **HOST Interrupt**

The HOST can be interrupted on a rising edge of the source.

### **DSP Interrupt**

The DSP can be interrupted on a rising edge of the source.

## **1.3.3 PXI TRIGGER OUTPUTS**

The card can source signals on the PXI Trigger lines from the following sources.

- DSP Timers
- External TTL inputs
- Trigger by DSP
- Trigger by HOST
- Discrete Logic Level



## **1.4 SOFTWARE SUPPORT**

The **CPCI-AD320** is supported under *Windows NT* by a **Board Support Package** which is supplied with the card.

The card is also supported by a **DSP Support Library** providing the following features:

- Common access routines for communications with the HOST. These routines also allow for Direct and DMA access to HOST memory.
- Identify the applicable card resources and parameters.
- Allow for serial communication through the provided serial port for debugging DSP code and configuring the card.

A bootloader provided on the card allows for control by the HOST, including downloading custom DSP code. User code can also be downloaded to FLASH memory and booted automatically on reset.

All these are provided in a manner consistent across ALPHI Technology platforms. Other documentation supplied with the card will describe the support in full detail.

## **1.5 REFERENCE MATERIALS LIST**

### **PCI Local Bus Specification:**

PCI Special Interest Group  
Tel: (800) 433-5177  
Tel: (503) 797-4207  
Fax: (503) 234-6762

### **PXI Specification: PCI Extensions for Instrumentation:**

PXI System Alliance  
<http://www.pxisa.org>

### **PCI 9080 PCI Controller data book:**

PLX Technology Corporation  
Tel: (408) 744-9060  
<http://www.plxtech.com>  
[apps@plxtech.com](mailto:apps@plxtech.com)

### **DSP (TMS320C32) C Compiler, Assembler, Linker:**

*Part Number TMDU3243855-02*

Texas Instruments  
Tel: (410) 312-7900  
<http://www.ti.com>

### **DSP Debugger and Integrated Development Environment:**

*Code Composer*

GO-DSP Corporation  
Tel: (416) 599-6868  
<http://www.go-dsp.com>

### **DSP Emulators suitable for use with *Code Composer* or TI debugger:**

White Mountain DSP  
(603) 833-2430  
<http://www.wmdsp.com>

### **WindowsNT and Windows95 Programming Tools:**

BlueWater Systems  
Tel: (206) 771-3610  
Fax: (206) 771-2742  
[info@bluewatersystems.com](mailto:info@bluewatersystems.com)  
<http://www.bluewatersystems.com>

## **2. CPCI BRIDGE TO LOCAL PCI BUS**

A Standard PCI to PCI bridge chip is used to connect the CPCI Bus to the local PCI bus present on the **CPCI-AD320**. There are two PCI type devices present on the local PCI bus.

- PLX 9080 bridge between the Local PCI bus and the DSP bus.
- Installed PMC Module.

The bridge is necessary to meet the CPCI bus loading requirements, and it also affords a few added benefits.

### **2.1 OFFLOADING OF CPCI BUS**

Local PCI Bus traffic does not affect the CPCI bus. The PLX9080 and the PMC module can communicate at high rates and low latency without affecting the HOST CPCI bus. Both devices can request the Local PCI bus for direct bus mastered transfers, both to each other, as well as the rest of the CPCI bus through the CPCI bridge.

This bridge allows the HOST CPCI bus to independently access both the PMC and the **CPCI-AD320** registers on the DSP bus. Standard HOST drivers for the PMC module will work without any modification.

Because of buffering within the CPCI to Local PCI bridge, overall bus utilization can be maintained at a high percentage.

### **2.2 DSP HANDLING OF PMC INTERRUPT**

The hardware on the **CPCI-AD320** makes it possible to intercept the PMC interrupt line from reaching the CPCI bus, and can route the interrupt to the DSP. This may be helpful for applications involving processor PMC modules or data communication PMC modules. Custom software on the DSP can then offload the HOST processor.

### **2.3 NO BRIDGE PROGRAMMING REQUIRED**

Many HOST operating systems will automatically configure the bridge with no intervention required. The CPCI to Local PCI bridge is fully compatible with the PCI bridge specifications.

### **2.4 STAND ALONE OPERATION**

If the **CPCI-AD320** is used in a stand-alone configuration without a CPCI bus, the CPCI to Local PCI bridge will not be populated, and hardware on the **CPCI-AD320** will take over the local PCI clocking and bus request and grant. The DSP and the PLX9080 can configure the PMC PCI configuration registers.

### **3. LOCAL PCI BRIDGE TO LOCAL DSP BUS**

A PLX PCI9080 bridge chip is used to interface the Local DSP Bus to the local PCI Bus on the **CPCI-AD320**. This interface provides the card with the following features.

- Completely transparent access by HOST and PMC to the Local DSP Bus.
- Completely transparent access by DSP to the CPCI bus and PMC.
- Eight mailbox registers and two doorbell registers for communication between the HOST/PMC and the DSP.
- Two Bus Master DMA channels with scatter / gather support for transfers between the local PCI or CPCI bus and the DSP bus.
- Full interrupt support to HOST and DSP.
- Ability to intercept PCI interrupt from PMC to handle by DSP.

#### **3.1 INTERFACE TO HOST (CPCI)**

All PCI devices contain a set of registers in Configuration Space which allow for determining the manufacturer and model of the device, determining the resources necessary for the correct operation of the device, and other configuration information. Configuration space is decoded on a per slot / device basis via a mechanism described in the PCI specification.

All PCI devices can be relocated in physical memory by means of several Base Address Registers. These registers contain the high address bits, which must be matched for any access to the card to be successful. Part of the protocol of programming the Base Address Registers allows for the transfer of information regarding the size of the regions. The actual Base Address Registers are located in Configuration Space.

Normally, configuring the card is performed by the system controller and some form of firmware or BIOS. Unfortunately, determining Base Addresses and other configuration information in Configuration Space is operating system dependent. One of the primary functions of the device driver under Windows NT is to map these resources to the user application.

The card is actually accessed through the decoded base address registers.

#### **3.2 CPCI CONFIGURATION SPACE**

*DSP Address:*                0x880000 – 0x88000F  
*PCI Address:*                CONFIG:0x00 – 0x3C  
*Mode of Access:*            Read/Write  
*Reset By*                    CPCI Hardware Reset

The card has the following registers available to PCI Configuration Space. They are implemented in the PLX chip. The registers are also accessible from the DSP Local bus.

| Offset Into<br>PCI CFG | DSP<br>Address | 31 – 24  | 23 – 16        | 15 – 8                  | 7 – 0              |
|------------------------|----------------|--|----------------|-------------------------|--------------------|
| 0x00                   | 0x880000       | Device ID  |                | Vendor ID               |                    |
| 0x04                   | 0x880001       | Status   |                | Command                 |                    |
| 0x08                   | 0x880002       | Class Code   |                |                         | Revision ID        |
| 0x0C                   | 0x880003       | BIST   | Header<br>Type | PCI<br>Latency<br>Timer | Cache Line<br>Size |
| 0x10                   | 0x880004       | PCI Base Address 0<br>(Memory Access to PLX Registers)               |                |                         |                    |
| 0x14                   | 0x880005       | PCI Base Address 1<br>(I/O Access to PLX Registers)                  |                |                         |                    |
| 0x18                   | 0x880006       | PCI Base Address 2<br>(Memory Access to DSP SRAM and card registers) |                |                         |                    |
| 0x1C                   | 0x880007       | PCI Base Address 3<br>(Not Used for this card)                       |                |                         |                    |
| 0x20                   | 0x880008       | Unused PCI Base Address 4  |                |                         |                    |
| 0x24                   | 0x880009       | Unused PCI Base Address 5  |                |                         |                    |
| 0x28                   | 0x88000A       | Cardbus CIS Pointer (Not Supported)                                  |                |                         |                    |
| 0x2C                   | 0x88000B       | Subsystem ID   |                | Subsystem Vendor ID     |                    |
| 0x30                   | 0x88000C       | PCI Base Address for Expansion ROM                                   |                |                         |                    |
| 0x34                   | 0x88000D       | Reserved   |                |                         |                    |
| 0x38                   | 0x88000E       | Reserved   |                |                         |                    |
| 0x3C                   | 0x88000F       | Max<br>Latency   | Min Grant      | Interrupt<br>Pin        | Interrupt<br>Line  |

**Table 3.1: CPCI Configuration Space**

The card presents the following initial configuration values to the CPCI system, based on the values stored in the NVRAM device read by the PLX PCI9080 interface chip.

| <b>Register</b>      | <b>Value (Meaning)</b>  |
|----------------------|---|
| Vendor ID            | 0x13C5 (ALPHI Technology)                                     |
| Device ID            | 0x0205  |
| Revision ID          | 0x00  |
| Class Code           | 0xff0000 (Device does not fit into defined class codes)       |
| Interrupt Line       | 0xff  |
| Interrupt Pin        | A   |
| Multifunction Device | No  |
| Build In Self Test   | No  |
| Latency Timer        | 0x00  |
| Minimum Grant        | 0x00  |
| Maximum Latency      | 0x00  |
| Base Address 0 Size  | 0x100 Bytes (Memory Access to PLX Registers)                  |
| Base Address 1 Size  | 0x100 Bytes (I/O Access to PLX Registers)                     |
| Base Address 2 Size  | 0x200000 Bytes (Memory Access to DSP SRAM and card registers) |
| Base Address 3 Size  | None (Not applicable to this card)                            |
| Expansion ROM Size   | None  |

**Table 3.2: PCI Configuration Register Default Values**

### **3.3 CPCI BASE ADDRESS REGIONS**

There are 4 base address regions available on the PLX PCI9080. The **CPCI-AD320** uses 3 of these regions.

- BAR0: Memory access the PLX operation registers.
- BAR1: I/O access the PLX operation registers.
- BAR2: Passthru to the DSP bus and is used to access the DSP SRAM and the card control / status registers. The passthru is established at PCI reset via the NVRAM.
- BAR3: Not used on this design.

***NOTE: Regions, which are accessed by memory cycles, will reside at physical addresses above 1MB. Therefore, non-protected (real) mode operating systems running on a x86 class processor, such as DOS, will not be able to access these regions. Any applications, which must run under DOS, must be compiled with a DOS Protected Mode Extender, such as PharLap or will require making DPMI calls to switch to protected mode. ALPHI Technology does not provide any DOS software support, but we will be happy to help with hardware technical issues.***

#### **4. LOCAL DSP BUS**

The following devices are present on the Local DSP Bus at the addresses specified. Many of these devices are also accessible by the HOST directly through the Base Address Regions. The PLX PCI9080 accesses the Local DSP Bus by placing the DSP in a HOLD state, performing any cycles necessary, and releasing the DSP from HOLD.

| <b>HOST Address</b>         | <b>DSP Address</b>    | <b>Data</b> | <b>R/W</b> | <b>Description</b>              |
|-----------------------------|-----------------------|-------------|------------|---------------------------------|
| BAR2: 0x000000 – 0x07FFFF   | 0x000000 – 0x01FFFF   | D31-D00     | R/W        | Local SRAM                      |
| BAR2: 0x080000 – 0x0FFFFFFF | 0x020000 – 0x03FFFF   | D31-D00     | R/W        | Local SRAM repeated             |
| BAR2: 0x100000 – 0x17FFFF   | 0x040000 – 0x05FFFF   | D31-D00     | R/W        | Card Control / Status Registers |
| BAR0: 0x00 – 0xFF           | 0x880000 – 0x88003F   | D31-D00     | R/W        | PLX Operation Registers         |
| Not Accessible              | 0x900000 – 0x97FFFF   | D07-D00     | RO         | Local FLASH                     |
| Not Accessible              | 0xC00000 – 0xFFFFFFFF | D31-D00     | R/W        | Pass through to CPCI bus        |

**Table 4.1: Local DSP Bus Overview**

In certain applications, it may be necessary to calculate the impact of accessing the Local DSP Bus from the HOST. The following table of events should help to explain the timing of a SRAM read. A single 32 bit read will stall the DSP for 10 clocks, or 333 nS. Burst access will add a single clock for each additional word. Of course, the DSP can continue running from the DSP cache and using internal RAM inside the DSP. Additionally, access to the Local Bus by the PLX can be turned off by the DSP for short periods of time during critical code sections.

| <b>Cycle</b> | <b>Action by DSP</b>              | <b>Action by PLX</b>               |
|--------------|-----------------------------------|------------------------------------|
| 0            | Normal Access                     | Signals request for bus            |
| 1            | Idles bus prior to relinquish     | Waits for acknowledgement          |
| 2            | Relinquishes bus and acknowledges | Seizes bus, driving idle           |
| 3            | Waits for release                 | Drives Address Phase for Read      |
| 3+1          | Waits for release                 | Performs Data Phase for Read       |
| 3+2          | Waits for release                 | Optionally continue burst Read     |
| ...          | ...                               | ...                                |
| 3+n          | Waits for release                 | Last burst read                    |
| 4+n          | Waits for release                 | Internal Synchronization           |
| 5+n          | Waits for release                 | Internal Synchronization           |
| 6+n          | Waits for release                 | Releases bus. Driven idle by card. |
| 7+n          | One cycle lost to synchronization | Idle                               |
| 8+n          | DSP recognizes release            | Idle                               |
| 9+n          | DSP performs idle cycle           | Idle                               |

**Table 4.2: HOST Read of Local DSP SRAM**

#### **4.1 LOCAL SRAM**

DSP Address:            0x000000 - 0x03FFFF, Bits 31-00  
 PCI Address:            BAR2:0x000000 - 0x0FFFFFF, Bits 03-00  
 Mode of Access:        Read/Write

There is 128k x 32 of Local SRAM for storing DSP programs and buffering data. The SRAM is accessible to both the DSP and the HOST.

The SRAM operates at zero wait states to the DSP, and one wait state on the first read by the PLX PCI9080 due to the separate address and data phase. Additional access in burst mode by the PLX will occur at zero wait state.

The decoding of the SRAM occurs twice, at 0x000000 and 0x020000 in order to make use of the 4k section at 0x000000 which is normally lost to internal DSP access. This memory can be accessed at 0x020000 – 0x020FFF.

#### **4.2 CARD CONTROL / STATUS REGISTERS**

The following locations are the Control / Status registers for the card. These registers are accessible to both the DSP and the HOST.

These registers operate with two wait states to the DSP.



| HOST Address<br>BAR2: | DSP<br>Address | Data    | R/W | Description   |
|-----------------------|----------------|---------|-----|---|
| 0x100000              | 0x040000       | D03-D00 | R/W | 9080 Control / Status Register                        |
| 0x100020              | 0x040008       | N/A     | WS  | HOST Interrupt Acknowledge                            |
| 0x100040              | 0x040010       | D07-D00 | R/W | Board Control / Status Register                       |
| 0x100060              | 0x040018       | N/A     | WS  | Reset the hardware FIFO                               |
| 0x100080              | 0x040020       | D15-D00 | R   | Read the hardware FIFO                                |
| 0x100080              | 0x040020       | D15-D00 | W   | Write the hardware FIFO for testing and configuration |
| 0x1000A4              | 0x040029       | N/A     | WS  | Reset Watchdog Timer                                  |
| 0x1000C0              | 0x040030       | D31-D00 | WO  | PGA Gain Registers                                    |
| 0x1000E0              | 0x040038       | N/A     | WS  | Software Strobe for manual clocking by DSP            |
| 0x100100              | 0x040040       | D07-D00 | R/W | Trigger / Gate Configuration Registers                |
| 0x100120              | 0x040048       | D07-D00 | R/W | 8530 Serial Ports                                     |
| 0x100140              | 0x040050       | N/A     | WS  | Software Strobe for manual clocking by HOST           |
| 0x100160              | 0x040058       | D07-D00 | R/W | RPIO Serial Bus and Digital Port Configuration        |
| 0x100180              | 0x040060       | D15-D00 | R/W | Digital Ports A and B                                 |
| 0x100200              | 0x040080       | D07-D00 | R/W | DSP Interrupt Status Register                         |
| 0x100224              | 0x040081       | D07-D00 | R/W | DSP Interrupt Enable Register                         |
| 0x100228              | 0x040082       | D07-D00 | R/W | DSP Bootmode Register                                 |
| 0x10022C              | 0x040083       | D07-D00 | R/W | Null Pace / Limit Register                            |
| 0x100234              | 0x040085       | D07-D00 | R/W | Demand DMA Control Register                           |
| 0x100238              | 0x040086       | D07-D00 | R/W | Demand DMA 0 Transfer Count Register                  |
| 0x10023C              | 0x040087       | D07-D00 | R/W | Demand DMA 1 Transfer Count Register                  |

**Table 4.3: Control / Status Registers**

#### **4.2.1 9080 CONTROL / STATUS REGISTER**

DSP Address:            0x040000, Bits 03-00  
 PCI Address:            BAR2:0x100000, Bits 03-00  
 Mode of Access:        Mixed

This register allows for simplified determination of the cause of a DSP interrupt from the PLX, as well as providing a way to temporarily lockout access by the HOST.

| BIT 03 | BIT 02 | BIT 01 | BIT 00      |
|--------|--------|--------|-------------|
| LSERR  | LINTO  | DMPAF  | LOCKOUT9080 |

**LSERR**

*DSP Address:* 0x040000, Bit 03  
*PCI Address:* BAR2:0x100000, Bit 03  
*Mode of Access:* Read Only  
*Reset By* See PLX Documentation

This bit tracks the current state of the LSERR line from the PLX PCI9080. When this is low, (0), it implies that the DSP interrupt was caused by this hardware signal. See the PLX documentation for more details and for a list of causes.

**LINTO**

*DSP Address:* 0x040000, Bit 02  
*PCI Address:* BAR2:0x100000, Bit 02  
*Mode of Access:* Read Only  
*Reset By* See PLX Documentation

This bit tracks the current state of the LINTO line from the PLX PCI9080. This line is the normal way in which the PLX interrupts the DSP. When this is low, (0), it implies that the DSP interrupt was caused by this hardware signal. See the PLX documentation for more details and for the enable bits.

**DMPAF**

*DSP Address:* 0x040000, Bit 01  
*PCI Address:* BAR2:0x100000, Bit 01  
*Mode of Access:* Read Only  
*Reset By* See PLX Documentation

This bit tracks the current state of the DMPAF line from the PLX PCI9080. This line can be used to throttle direct writes by the DSP to the HOST PCI bus. When this is low, (0), it implies that the FIFO inside the PLX has a programmable number of accesses queued, but not yet completed for the HOST PCI bus. See the PLX documentation for more details and for the enable bits.

**LOCKOUT9080**

*DSP Address:* 0x040000, Bit 00  
*PCI Address:* BAR2:0x100000, Bit 00  
*Mode of Access:* Read/Write  
*Reset By* CPCI Hardware Reset, Software Reset, Watchdog Reset

This bit, when set (1) will prevent the PLX PCI9080 from seizing the Local Bus. This can allow for time critical DSP code to complete in a timely manner. This bit should only be set for short intervals of time, since it may potentially lock up the HOST PCI bus until it has been cleared (when an access to the card is performed).

**4.2.2 HOST INTERRUPT ACKNOWLEDGE**

*DSP Address:* 0x040008  
*PCI Address:* BAR2:0x100020  
*Mode of Access:* Write Strobe

The HOST can write to this register to turn off the HOST interrupt generated by LINTI. It is intended for use by the HOST device driver.

### 4.2.3 BOARD CONTROL / STATUS REGISTER

DSP Address: 0x040010, Bits 07-00  
 PCI Address: BAR2:0x100040, Bits 07-00  
 Mode of Access: Mixed

This register allows for querying the current state of the hardware FIFO flags and a means to program the FIFO.

| BIT 07     | BIT 06      | BIT 05      | BIT 04     | BIT 03 | BIT 02 | BIT 01             | BIT 00      |
|------------|-------------|-------------|------------|--------|--------|--------------------|-------------|
| FIFO<br>FF | FIFO<br>PAF | FIFO<br>PAE | FIFO<br>EF | N/A    | N/A    | DISABLE<br>PMC INT | FIFO<br>REG |

#### FIFO FF

DSP Address: 0x040010, Bit 07  
 PCI Address: BAR2:0x100040, Bit 07  
 Mode of Access: Read Only  
 Set By Write to **Reset the Hardware FIFO**

This bit, when low (0), indicates that there are 8192 samples stored in the hardware FIFO.

#### FIFO PAF

DSP Address: 0x040010, Bit 06  
 PCI Address: BAR2:0x100040, Bit 06  
 Mode of Access: Read Only  
 Set By Write to **Reset the Hardware FIFO**

This bit, when low (0), indicates that there is a programmable number of samples stored in the hardware FIFO.

#### FIFO PAE

DSP Address: 0x040010, Bit 05  
 PCI Address: BAR2:0x100040, Bit 05  
 Mode of Access: Read Only  
 Reset By Write to **Reset the Hardware FIFO**

This bit, when low (0), indicates that there is less than a programmable number of samples stored in the hardware FIFO.

#### FIFO EF

DSP Address: 0x040010, Bit 04  
 PCI Address: BAR2:0x100040, Bit 04  
 Mode of Access: Read Only  
 Reset By Write to **Reset the Hardware FIFO**

This bit, when low (0), indicates that there are no samples stored in the hardware FIFO.

#### DISABLE PMC INT

DSP Address: 0x040010, Bit 01  
 PCI Address: BAR2:0x100040, Bit 01  
 Mode of Access: Read/Write  
 Reset By CPCI Hardware Reset, Software Reset, Watchdog Reset

When this bit is high (1), the PMC interrupt is blocked from causing an interrupt to the HOST computer. The DSP can catch the interrupt on its INT2 line, and perform its own handling of the PMC, if desired. When this bit is low (0), the PMC interrupt is passed to the HOST for normal processing.

## FIFO REG

DSP Address: 0x040010, Bit 00  
PCI Address: BAR2:0x100040, Bit 00  
Mode of Access: Read/Write  
Reset By CPCI Hardware Reset, Software Reset, Watchdog Reset

This bit, when cleared to low (0), causes writes to **Write the Hardware FIFO** to be placed into the FIFO for testing purposes. Reads of **Read the Hardware FIFO** will access the contents of the FIFO. When the bit is set high (1), writes to and reads of the FIFO will access the FIFO programming registers.

### 4.2.4 RESET THE HARDWARE FIFO

DSP Address: 0x040018  
PCI Address: BAR2:0x100060  
Mode of Access: Write Strobe

A write to this location will reset the hardware FIFO to empty. It is required to initialize the FIFO before any access is made.

### 4.2.5 READ THE HARDWARE FIFO

DSP Address: 0x040020, Bits 31-00  
PCI Address: BAR2:0x100080, Bits 31-00  
Mode of Access: Read Access  
Reset By Write to **Reset the Hardware FIFO**

If the **FIFO REG** bit is clear (0), then a read of this location will respond with the oldest pair of samples in the FIFO. If the **FIFO REG** bit is set (1), then a read of this location will read the internal configuration registers of the FIFO.

Data is stored as pairs of 16 bit WORDs in 2's complement format, but must be read as 32 bit DWORDs. The even numbered channels are in the high WORD, and the odd channels in the low WORD.

When the state machine writes to the FIFOs, it writes all 32 conversion results as 16 pairs in channel order (ch2|ch1, ch4|ch3, ch6|ch5, ch8|ch7, ch10|ch9, ch12|ch11, ch14|ch13, ch16|ch15, ch18|ch17, ch20|ch19, ch22|ch21, ch24|ch23, ch26|ch25, ch28|ch27, ch30|ch29, ch32|ch31).

### 4.2.6 WRITE THE HARDWARE FIFO

DSP Address: 0x040020, Bits 31-00  
PCI Address: BAR2:0x100080, Bits 31-00  
Mode of Access: Write Access  
Reset By Write to **Reset the Hardware FIFO**

If the **FIFO REG** bit is clear (0), then a write to this location will directly add the value to the FIFO for testing purposes. If the **FIFO REG** bit is set (1), then a write to this location will program the internal configuration registers of the FIFO.

The FIFO is actually four 8k x 9 FIFOs from Cypress, model CY7C5251.

#### **4.2.7 RESET WATCHDOG TIMER**

DSP Address:            0x040029  
 PCI Address:            BAR2:0x1000A4  
 Mode of Access:        Write Strobe

The **CPCI-AD320** incorporates a watchdog timer to help ensure that the DSP will always be operating correctly.

Use of the watchdog is optional. By default, and as a result of a CPCI Hardware Reset, a Software Reset, and the Watchdog Reset, the hardware will automatically strobe the watchdog timer to prevent inadvertent RESET. The first time that this location is written, the hardware will enter a mode where automatic strobes stop, and the write to this location resets the watchdog timer.

If this location is then not repeatedly written within a period of approximately 250 – 1000 mS, the watchdog timer will reset the entire **CPCI-AD320**. Since the watchdog RESET will also clear the **Bootmode Register**, the DSP will be forced to boot from the FLASH device.

#### **4.2.8 PGA GAIN REGISTERS**

DSP Address:            0x040030 – 0x40033, Bits 07-00  
 PCI Address:            BAR2:0x1000C0 – 0x1000CC, Bits 07-00  
 Mode of Access:        Write Only  
 Reset By                Not Reset by any signal

There are four to eight PGA gain registers as follows. Channels 17-32 only exist if the optional additional 16 channels (on the daughter card) is present.

| HOST Address<br>BAR2: | DSP<br>Address | BITS 07-<br>06 | BITS 05-<br>04 | BITS 03-<br>02 | BITS 01-<br>00 |
|-----------------------|----------------|----------------|----------------|----------------|----------------|
| 0x1000C0              | 0x040030       | Chan 4         | Chan 3         | Chan 2         | Chan 1         |
| 0x1000C4              | 0x040031       | Chan 8         | Chan 7         | Chan 6         | Chan 5         |
| 0x1000C8              | 0x040032       | Chan 12        | Chan 11        | Chan 10        | Chan 9         |
| 0x1000CC              | 0x040033       | Chan 16        | Chan 15        | Chan 14        | Chan 13        |
| 0x1000D0              | 0x040034       | Chan 20        | Chan 19        | Chan 18        | Chan 17        |
| 0x1000D4              | 0x040035       | Chan 24        | Chan 23        | Chan 22        | Chan 21        |
| 0x1000D8              | 0x040036       | Chan 28        | Chan 27        | Chan 26        | Chan 25        |
| 0x1000DC              | 0x040037       | Chan 32        | Chan 31        | Chan 30        | Chan 29        |

The gains can be selected from the following:

| BITS 01-00 | Factory Default | Special Order | Special Order |
|------------|-----------------|---------------|---------------|
| 00         | x1              | x1            | x1            |
| 01         | x2              | X2            | x10           |
| 10         | x4              | X5            | x100          |
| 11         | x8              | X10           | X1000         |

**Table 4.4: Programmable Gain Selections**

**4.2.9 SOFTWARE STROBE FOR MANUAL CLOCKING BY DSP**

DSP Address:            0x040038  
 PCI Address:            BAR2:0x1000E0  
 Mode of Access:        Write Strobe

A write to this location can potentially trigger a conversion or other event if selected in the **Trigger / Gate Configuration Registers**.

**4.2.10 TRIGGER / GATE CONFIGURATION REGISTERS**

DSP Address:            0x040040 – 0x040047, Bits 07 – 00  
 PCI Address:            BAR2:0x100100 – 0x10011C, Bits 07 – 00  
 Mode of Access:        Mixed  
 Reset By                CPCI Hardware Reset, Software Reset,  
                             Watchdog Reset

These registers control the trigger and gate signal routing inside the card, as well as allow for the control and monitoring of the PXI trigger lines. All of the registers are read/write, except for the PXI monitoring bits, which are read only.

| HOST Address<br>BAR2: | DSP<br>Address | BITS 07-04            | BITS 03-00                               |
|-----------------------|----------------|-----------------------|--|
| 0x100100              | 0x040040       | A/D Clock Source      | A/D Gate Source                          |
| 0x100104              | 0x040041       | HOST Interrupt Source | Front Panel /Rear<br>Clock Output Source |
| 0x100108              | 0x040042       | N/A                   | DSP Interrupt Source                     |

**Table 4.5: Trigger / Gate Source Registers**

| HOST Address<br>BAR2: | DSP<br>Address | BITS 07-00                |
|-----------------------|----------------|---------------------------|
| 0x10010C              | 0x040043       | PXI Trigger Direct Output |

**Table 4.6: PXI Programmable Output Register**

| HOST Address<br>BAR2: | DSP<br>Address | BIT 07      | BITS 06-04  | BIT 03      | BITS 02-00  |
|-----------------------|----------------|-------------|-------------|-------------|-------------|
| 0x100110              | 0x040044       | PXI1<br>Mon | PXI1 Source | PXI0<br>Mon | PXI0 Source |
| 0x100114              | 0x040045       | PXI3<br>Mon | PXI3 Source | PXI2<br>Mon | PXI3 Source |
| 0x100118              | 0x040046       | PXI5<br>Mon | PXI5 Source | PXI4<br>Mon | PXI4 Source |
| 0x10011C              | 0x040047       | PXI7<br>Mon | PXI7 Source | PXI6<br>Mon | PXI6 Source |

**Table 4.7: PXI Trigger Source Registers**

**Trigger / Gate Sources**

*DSP Address:* 0x040040 – 0x40042, Bits 07 – 00  
*PCI Address:* BAR2:0x100100 – 0x100108, Bits 07 – 00  
*Mode of Access:* Read/Write  
*Reset By* CPCI Hardware Reset, Software Reset,  
 Watchdog Reset

The following signals can be selected from several sources.

- A/D Clock
- A/D Gate
- Front Panel / Rear Clock Output
- HOST Interrupt
- DSP Interrupt

| <b>BITS 03-00</b> | <b>BITS 07-04</b> | <b>Source</b>                                |
|-------------------|-------------------|--|
| 0x0               |                   | Low (0)                                      |
| 0x1               |                   | High (1)                                     |
| 0x2               |                   | DSP Timer 0                                  |
| 0x3               |                   | DSP Timer 1                                  |
| 0x4               |                   | Trigger Input (Front Panel / Rear Connector) |
| 0x5               |                   | Gate Input (Front Panel/ Rear Connector)     |
| 0x6               |                   | Strobe Register from HOST                    |
| 0x7               |                   | Strobe Register from DSP                     |
| 0x8               |                   | PXI Trigger 0                                |
| 0x9               |                   | PXI Trigger 1                                |
| 0xA               |                   | PXI Trigger 2                                |
| 0xB               |                   | PXI Trigger 3                                |
| 0xC               |                   | PXI Trigger 4                                |
| 0xD               |                   | PXI Trigger 5                                |
| 0xE               |                   | PXI Trigger 6                                |
| 0xF               |                   | PXI Trigger 7                                |

**Table 4.8: Trigger / Gate Sources**

**PXI Trigger Direct Output**

*DSP Address:* 0x040043, Bits 07 – 00  
*PCI Address:* BAR2:0x10010C, Bits 07 – 00  
*Mode of Access:* Read/Write  
*Reset By* CPCI Hardware Reset, Software Reset,  
 Watchdog Reset

The PXI Trigger can be driven to a specific logic state for gating or other applications.

If the **PXI Trigger Source** is set to PXI Trigger Direct Output, then the associated bit is output to the PXI Trigger line.

**PXI Trigger Monitor**

DSP Address: 0x040044 – 0x40047, Bits 07 and 03  
 PCI Address: BAR2:0x100110 – 0x10011C, Bits 07 and 03  
 Mode of Access: Read Only

These bits reflect the current state of the PXI Trigger lines.

**PXI Trigger Source**

DSP Address: 0x040044 – 0x40047, Bits 06-04 and 02-00  
 PCI Address: BAR2:0x100110 – 0x10011C, Bits 06-04 and 02-00  
 Mode of Access: Read/Write  
 Reset By: CPCI Hardware Reset, Software Reset, Watchdog Reset

The PXI Trigger lines can be sourced from several sources, if desired.

| BITS 02-00<br>BITS 06-04 | Source                                       |
|--------------------------|--|
| 0x0                      | Line used as input or unused                 |
| 0x1                      | PXI Trigger Direct Output                    |
| 0x2                      | DSP Timer 0                                  |
| 0x3                      | DSP Timer 1                                  |
| 0x4                      | Trigger Input (Front Panel / Rear Connector) |
| 0x5                      | Gate Input (Front Panel/ Rear Connector)     |
| 0x6                      | Strobe Register from HOST                    |
| 0x7                      | Strobe Register from DSP                     |

**Table 4.9: PXI Trigger Sources**

**4.2.11 8530 SERIAL PORTS**

The **CPCI-AD320** includes an Z85C30 serial communications controller chip from ZILOG. There are two communications ports on this chip. Port 1 is connected to RS-232 drivers and is available at the front panel and at the rear panel I/O connectors. Port 2 is connected to RS-422 drivers, and is also available at the front panel and the rear panel.

The Z85C30 is clocked at 7.3728 MHz, and allows for a multitude of common frequencies, including 115,200, 57,600, 38,400, and 19,200 baud.

The bootloader and hardware support libraries supplied with the **CPCI-AD320** utilizes the RS-232 port for a console for standard input and output by the DSP. The customer may alternatively wish to write his own software to use this port. Examples are provided in the **Board Support Package**.

There is hardware support for many RS422 and RS485 applications including HDLC, SDLC, and multidrop configurations. Clocking can be provided externally or internally.

The 8530 can interrupt the DSP for servicing. The 8530 is routed to INT2 via the interrupt control logic. See the DSP Interrupt Status Register and the DSP Interrupt Enable Register for details.

See documentation from ZILOG for more details about programming this device.



| HOST Address<br>BAR2: | DSP<br>Address | BITS 07-00              |
|-----------------------|----------------|-------------------------|
| 0x100120              | 0x040048       | Control Port for RS-422 |
| 0x100124              | 0x040049       | Data Port for RS-422    |
| 0x100128              | 0x04004A       | Control Port for RS-232 |
| 0x10012C              | 0x04004B       | Data Port for RS-232    |

**Table 4.10: Z85C30 Serial Port**

#### 4.2.12 SOFTWARE STROBE FOR MANUAL CLOCKING BY HOST

DSP Address:            0x040050  
 PCI Address:            BAR2:0x100140  
 Mode of Access:        Write Strobe

A write to this location can potentially trigger a conversion or other event if selected in the **Trigger / Gate Configuration Registers**.

#### 4.2.13 RPIO SERIAL BUS AND DIGITAL PORT CONFIGURATION

DSP Address:            0x040058  
 PCI Address:            BAR2:0x100160  
 Mode of Access:        Read/Write  
 Reset By                CPCI Hardware Reset, Software  
                               Reset, Watchdog Reset

This register controls the direction of the 16 digital I/O lines, and allows control of the RPIO Serial Peripheral Bus.

| BIT<br>07-06 | BIT 05    | BIT 04    | BIT 03 | BIT 02 | BIT 01 | BIT 00 |
|--------------|-----------|-----------|--------|--------|--------|--------|
| N/A          | PB<br>DIR | PA<br>DIR | SRST   | SLD    | SCK    | SDI    |

#### **PB DIR**

DSP Address:            0x040058, Bit 05  
 PCI Address:            BAR2:0x100160, Bit 05  
 Mode of Access:        Read/Write  
 Reset By                CPCI Hardware Reset, Software Reset,  
                               Watchdog Reset

When this bit is clear (0), digital port B is configured as an input. When this bit is set (1), digital port B is configured as an output. There are 10k pull resistors on the digital lines, so the RESET state will be HIGH on the digital lines.

#### **PA DIR**

DSP Address:            0x040058, Bit 04  
 PCI Address:            BAR2:0x100160, Bit 04  
 Mode of Access:        Read/Write  
 Reset By                CPCI Hardware Reset, Software  
                               Reset, Watchdog Reset

When this bit is clear (0), digital port A is configured as an input. When this bit is set (1), digital port A is configured as an output. There are 10k pull resistors on the digital lines, so the RESET state will be HIGH on the digital lines.

### **SRST**

*DSP Address:* 0x040058, Bit 03  
*PCI Address:* BAR2:0x100160, Bit 03  
*Mode of Access:* Read/Write  
*Reset By* CPCI Hardware Reset, Software Reset, Watchdog Reset

This bit directly controls the SRST line to the RPIO devices on the Serial Peripheral Bus.

When this bit is clear (0), the RPIO devices on the Serial Peripheral Bus will be reset. Since this bit is cleared at RESET, the RPIO devices will also be cleared at RESET. When this bit is set (1), the RPIO devices on the Serial Peripheral Bus will be in their normal operating mode.

### **SLD**

*DSP Address:* 0x040058, Bit 02  
*PCI Address:* BAR2:0x100160, Bit 02  
*Mode of Access:* Read/Write  
*Reset By* CPCI Hardware Reset, Software Reset, Watchdog Reset

This bit directly controls the SLD line to the RPIO devices on the Serial Peripheral Bus. Note that the SLD line is driven through an inverter.

When this bit is set and then cleared, an active low pulse will appear on the SLD line to the RPIO devices on the Serial Peripheral Bus. Since this bit is cleared on a RESET, and the line is driven through an inverter, the hardware line will be HIGH on RESET.

### **SCK**

*DSP Address:* 0x040058, Bit 01  
*PCI Address:* BAR2:0x100160, Bit 01  
*Mode of Access:* Read/Write  
*Reset By* CPCI Hardware Reset, Software Reset, Watchdog Reset

This bit directly controls the SCK line to the RPIO devices on the Serial Peripheral Bus.

When this bit is set and then cleared, an active high pulse will appear on the SCK line to the RPIO devices on the Serial Peripheral Bus. This will cause the first device to latch the data on SDI, and the remaining devices to move the configuration data to the next device.

### **SDI**

*DSP Address:* 0x040058, Bit 00  
*PCI Address:* BAR2:0x100160, Bit 00  
*Mode of Access:* Read/Write  
*Reset By* CPCI Hardware Reset, Software Reset, Watchdog Reset

This bit directly controls the SDI line to the RPIO devices on the Serial Peripheral Bus.

This bit represents the next data bit to be clocked along the Serial Peripheral Bus on the next clock edge.

#### 4.2.14 DIGITAL PORTS A AND B

DSP Address:            0x040060, Bits 15-00  
 PCI Address:            BAR2:0x100180, Bits 15-00  
 Mode of Access:        Read/Write  
 Reset By                Not Reset by any signal

When written, this register sets the output state for the two digital ports for when they are in output mode.

When read, this register will report the current state of the digital lines.

When initializing the digital ports for output, be sure to program any values to be output before setting the direction bits in **RPIO Serial Bus and Digital Port Configuration** register.

There are 10k pull resistors on the digital lines, so the RESET state will be HIGH on the digital lines.

| BITS 15 – 08   | BITS 07 – 00   |
|----------------|----------------|
| Digital Port B | Digital Port A |

#### 4.2.15 DSP INTERRUPT STATUS REGISTER

DSP Address:            0x040080, Bits 07-00  
 PCI Address:            BAR2:0x100200, Bits 07-00  
 Mode of Access:        Mixed Access

This register allows the DSP interrupt routine for INT2 to determine which of several sources are causing an interrupt. Additionally, it allows for determination of the current state of the HOST and DSP trigger interrupts.

| BIT 07 | BIT 06          | BIT 05         | BIT 04         | BIT 03     | BIT 02     | BIT 01 | BIT 00      |
|--------|-----------------|----------------|----------------|------------|------------|--------|-------------|
| N/A    | HOST<br>TRIGGER | DSP<br>TRIGGER | INT2<br>ACTIVE | EXT<br>INT | PMC<br>INT | N/A    | 8530<br>INT |

#### HOST TRIGGER

DSP Address:            0x040080, Bit 06  
 PCI Address:            BAR2:0x100200, Bit 06  
 Mode of Access:        Read Only

This bit monitors the current state of the HOST TRIGGER selected in the **Trigger / Gate Configuration Registers**. A rising edge on HOST TRIGGER will generate an interrupt to the HOST processor.

#### DSP TRIGGER

DSP Address:            0x040080, Bit 05  
 PCI Address:            BAR2:0x100200, Bit 05  
 Mode of Access:        Read Only

This bit monitors the current state of the DSP TRIGGER selected in the **Trigger / Gate Configuration Registers**. A rising edge on DSP TRIGGER will generate INT1 to the DSP processor.

### INT2 ACTIVE

DSP Address: 0x040080, Bit 04  
PCI Address: BAR2:0x100200, Bit 04  
Mode of Access: Read Only

When this bit is high (1), it indicates that one of the enabled sources for INT2 is currently generating an interrupt. Since the interrupt logic on the DSP is edge triggered, and a falling edge on this combined interrupt is required to interrupt the DSP, this line makes it possible in the DSP interrupt handler to ensure that all the causes have been handled, and that the line is de-asserted before returning. The line is de-asserted by writing a 1 to the active interrupt source in the lower 4 bits of this register, or by clearing the cause in the appropriate device.

### EXT INT

DSP Address: 0x040080, Bit 03  
PCI Address: BAR2:0x100200, Bit 03  
Mode of Access: Read / Write 1 to set

When this bit is read as low (0), it indicates that a falling edge has been detected on the external interrupt line located on the rear panel I/O connector. It is cleared by writing a 1 to this bit. This will reset the bit to set (1), and prepare the edge detector for the next interrupt.

If this interrupt is enabled, and this bit is low, then **INT2 ACTIVE** will also be low. Be sure at the end of the interrupt routine that all the active interrupts have been acknowledged by writing 1's to this status register, or by clearing the interrupt in the device.

### PMC INT

DSP Address: 0x040080, Bit 02  
PCI Address: BAR2:0x100200, Bit 02  
Mode of Access: Read Only

When this bit is low (0), it indicates that the PMC module is currently asserting its interrupt line. Since the interrupt logic on the DSP is edge triggered, and a falling edge on the PMC interrupt is required to interrupt the DSP, this bit makes it possible in the DSP interrupt handler to ensure that the line is de-asserted before returning.

If this interrupt is enabled, and this bit is low, then **INT2 ACTIVE** will also be low. Be sure at the end of the interrupt routine that all the active interrupts have been acknowledged by writing 1's to this status register, or by clearing the interrupt in the device.

### 8530 INT

DSP Address: 0x040080, Bit 00  
PCI Address: BAR2:0x100200, Bit 00  
Mode of Access: Read Only

When this bit is read as low (0), it indicates that the 8530 serial controller chip is asserting its interrupt line. It is cleared by performing the appropriate action to the 8530 controller chip.

If this interrupt is enabled, and this bit is low, then **INT2 ACTIVE** will also be low. Be sure at the end of the interrupt routine that all the active interrupts have been

acknowledged by writing 1's to this status register, or by clearing the interrupt in the device.

**4.2.16 DSP INTERRUPT ENABLE REGISTER**

*DSP Address:* 0x040081, Bits 07-00  
*PCI Address:* BAR2:0x100204, Bits 07-00  
*Mode of Access:* Mixed  
*Reset By* CPCI Hardware Reset, Software Reset, Watchdog Reset

This register allows the DSP to select which interrupts should be allowed to generate INT2 on the DSP. Additionally, it allows for determination of the type of option board installed.

| BIT 07 | BIT 06-04    | BIT 03     | BIT 02     | BIT 01 | BIT 00      |
|--------|--------------|------------|------------|--------|-------------|
| N/A    | OPTION SENSE | EXT INT EN | PMC INT EN | N/A    | 8530 INT EN |

**OPTION SENSE**

*DSP Address:* 0x040081, Bits 06-04  
*PCI Address:* BAR2:0x100204, Bits 06-04  
*Mode of Access:* Read Only

These three bits allow a determination of the type of option daughter-board installed on the main card. As of this time, the following options are defined.

| BITS 06-04 | OPTION  |
|------------|---|
| 0x7        | No option present (total of 16 analog channels).  |
| 0x6        | Additional 16 channel option for CPCI-AD320 (total of 32 analog channels).                                |
| 0x5        | Option for CPCI-SERVO8 (total of 16 analog input channels, 8 analog output channels, other special logic) |

**EXT INT EN**

*DSP Address:* 0x040081, Bit 03  
*PCI Address:* BAR2:0x100204, Bit 03  
*Mode of Access:* Read/Write  
*Reset By* CPCI Hardware Reset, Software Reset, Watchdog Reset

When this bit is set (1), a falling edge on the external interrupt line located on the rear panel I/O connector will cause the DSP to see INT2. When this bit is clear (0), the external interrupt line is ignored, and any pending interrupt is cleared.

**PMC INT EN**

*DSP Address:* 0x040081, Bit 02  
*PCI Address:* BAR2:0x100204, Bit 02  
*Mode of Access:* Read/Write  
*Reset By* CPCI Hardware Reset, Software Reset, Watchdog Reset

When this bit is set (1), a falling edge on the PMC interrupt line will cause the DSP to see INT2. When this bit is clear (0), the PMC interrupt line is ignored.

**8530 INT EN**

DSP Address: 0x040081, Bit 00  
 PCI Address: BAR2:0x100204, Bit 00  
 Mode of Access: Read/Write  
 Reset By: CPCI Hardware Reset, Software Reset, Watchdog Reset

When this bit is set (1), a falling edge on the 8530 serial controller chip interrupt line will cause the DSP to see INT2. When this bit is clear (0), the 8530 interrupt line is ignored.

**4.2.17 DSP BOOTMODE REGISTER**

DSP Address: 0x040082, Bits 03-00  
 PCI Address: BAR2:0x100208, Bits 03-00  
 Mode of Access: Read/Write  
 Reset By: Watchdog Reset

This register allows for selecting several sources for booting the DSP. The choices are as follows.

- Booting a ROM image from FLASH device at 0x900000.
- Booting a ROM image from SRAM at 0x1000. This requires that the DSP be held in RESET, using the mechanism described in the RESET section, and an external PCI device copy the ROM image to the SRAM.
- Directly executing an executable image in SRAM at the reset vector located at 0x0. This requires that the DSP be held in RESET, using the mechanism described in the RESET section, and an external PCI device copy the executable image to the SRAM.

| BIT 03 | BIT 02 | BIT 01   | BIT 00 |
|--------|--------|----------|--------|
| N/A    | NB     | BOOT RAM | MC_MP  |

**NB**

DSP Address: 0x040082, Bit 02  
 PCI Address: BAR2:0x100208, Bit 02  
 Mode of Access: Read/Write  
 Reset By: Watchdog Reset

This bit directly controls the /NB line to the PLX, through an inverter. When it is LOW, after a PCI reset the PCI devices will be issued a retry until the DSP sets the Local Init Status bit in register CNTRL in the PLX. If this bit is HIGH, PCI accesses will be permitted immediately.

**BOOT RAM**

DSP Address: 0x040082, Bit 01  
 PCI Address: BAR2:0x100208, Bit 01  
 Mode of Access: Read/Write  
 Reset By: Watchdog Reset

When this bit is set (1), and the **MC\_MP** bit is clear (0), the DSP will boot from a RESET into a ROM image placed in SRAM by an external PCI agent.

When this bit is clear (0), and the **MC\_MP** bit is clear (0), the DSP will boot from a RESET into a ROM image placed in FLASH.

**MC\_MP**

DSP Address: 0x040082, Bit 00  
 PCI Address: BAR2:0x100208, Bit 00  
 Mode of Access: Read/Write  
 Reset By Watchdog Reset

When this bit is set (1), the DSP will immediately begin executing an executable image in SRAM at the reset vector located at 0x0, once it is taken from RESET. The executable image must be placed in RAM by an external PCI agent.

When this bit is clear (0), the DSP will boot a ROM image from either the FLASH or the RAM.

Note that this bit is reversed from the meaning in the DSP processor manuals.

**4.2.18 NULL PACE / LIMIT REGISTER**

DSP Address: 0x040083, Bits 07-00  
 PCI Address: BAR2:0x10020C, Bits 07-00  
 Mode of Access: Mixed  
 Reset By CPCI Hardware Reset, Software Reset, Watchdog Reset

The Clock In and Gate In lines on the front panel have a second function on other configurations of this hardware, which are not applicable to the **CPCI-AD320**. Therefore, to preserve functionality, some of these bits must remain 0.

This register allows for control and monitoring of the NULL PACE and LIMIT lines, and control of the USER LED.

| BIT 07-06 | BIT 05   | BIT 04  | BIT 03 | BIT 02   | BIT 01    | BIT 00    |
|-----------|----------|---------|--------|----------|-----------|-----------|
| N/A       | CLOCK IN | GATE IN | N/A    | USER LED | KEEP AS 0 | KEEP AS 0 |

**CLOCK IN**

DSP Address: 0x040083, Bit 05  
 PCI Address: BAR2:0x10020C, Bit 05  
 Mode of Access: Read Only

This bit represents the current state of the CLOCK IN line from the front panel or the rear panel I/O. It will read the current state of the line.

**GATE IN**

DSP Address: 0x040083, Bit 04  
 PCI Address: BAR2:0x10020C, Bit 04  
 Mode of Access: Read Only

This bit represents the current state of the GATE IN line from the front panel or the rear panel I/O. It will read the current state of the line.

**USER LED**

DSP Address: 0x040083, Bit 02  
 PCI Address: BAR2:0x10020C, Bit 02  
 Mode of Access: Read/Write  
 Reset By: CPCI Hardware Reset, Software Reset, Watchdog Reset

When this bit is set (1), the USER LED will be illuminated. When this bit is clear (0), the USER LED will extinguish.

**KEEP AS 0**

DSP Address: 0x040083, Bits 01-00  
 PCI Address: BAR2:0x10020C, Bits 01-00  
 Mode of Access: Read/Write  
 Reset By: CPCI Hardware Reset, Software Reset, Watchdog Reset

Keep these bits set to 0 to maintain full functionality.

**4.2.19 DEMAND DMA CONTROL REGISTER**

DSP Address: 0x040085, Bits 07-00  
 PCI Address: BAR2:0x100214, Bits 07-00  
 Mode of Access: Read/Write  
 Reset By: CPCI Hardware Reset, Software Reset, Watchdog Reset

The two DMA engines in the PLX can operate in a mode where they are throttled by external hardware signals. There is a state machine on the card to transfer a fixed number of DWORDs based upon a trigger signal.

DMA engine 0 is triggered by a programmable clock source which includes the PXI trigger lines and the DSP timers.

DMA engine 1 is triggered by the PAE flag from the hardware FIFO indicating that the programmed number of samples are available.

| BITS 07-06 | BIT 05               | BIT 04               | BITS 03-00           |
|------------|----------------------|----------------------|----------------------|
| N/A        | DMA 1 Trigger Enable | DMA 0 Trigger Enable | DMA 0 Trigger Source |

**DMA 1 Trigger Enable**

DSP Address: 0x040085, Bit 05  
 PCI Address: BAR2:0x100214, Bit 05  
 Mode of Access: Read/Write  
 Reset By: CPCI Hardware Reset, Software Reset, Watchdog Reset

When this bit is set (1), the DMA hardware will be enabled. Whenever PAE is asserted indicating that there are more than the programmed number of samples stored in the hardware FIFO, this state machine will request that the number of DWORDS specified in **Demand DMA 1 Transfer Count Register** will be read by the PLX DMA engine 1. Presumably, the PLX will have been set up for demand mode.



**DMA 0 Trigger Enable**

DSP Address: 0x040085, Bit 04  
 PCI Address: BAR2:0x100214, Bit 04  
 Mode of Access: Read/Write  
 Reset By: CPCI Hardware Reset, Software Reset, Watchdog Reset

When this bit is set (1), the DMA hardware will be enabled. Whenever a rising edge of the selected trigger source in **DMA 0 Trigger Source** is detected, this state machine will request that the number of DWORDS specified in **Demand DMA 0 Transfer Count Register** will be read by the PLX DMA engine 0. Presumably, the PLX will have been set up for demand mode.

**DMA 0 Trigger Source**

DSP Address: 0x040085, Bits 03-00  
 PCI Address: BAR2:0x100214, Bits 03-00  
 Mode of Access: Read/Write  
 Reset By: CPCI Hardware Reset, Software Reset, Watchdog Reset

This register selects the trigger source for the PLX DMA engine 0.

| BITS 03-00 | Source                                       |
|------------|--|
| 0x0        | Low (0)                                      |
| 0x1        | High (1)                                     |
| 0x2        | DSP Timer 0                                  |
| 0x3        | DSP Timer 1                                  |
| 0x4        | Trigger Input (Front Panel / Rear Connector) |
| 0x5        | Gate Input (Front Panel / Rear Connector)    |
| 0x6        | Strobe Register from HOST                    |
| 0x7        | Strobe Register from DSP                     |
| 0x8        | PXI Trigger 0                                |
| 0x9        | PXI Trigger 1                                |
| 0xA        | PXI Trigger 2                                |
| 0xB        | PXI Trigger 3                                |
| 0xC        | PXI Trigger 4                                |
| 0xD        | PXI Trigger 5                                |
| 0xE        | PXI Trigger 6                                |
| 0xF        | PXI Trigger 7                                |

**Table 4.11: Trigger / Gate Sources**

**4.2.20 DEMAND DMA 0 TRANSFER COUNT REGISTER**

DSP Address: 0x040086  
 PCI Address: BAR2:0x100218  
 Mode of Access: Read/Write  
 Reset By: CPCI Hardware Reset, Software Reset, Watchdog Reset

This 8 bit register sets the number of DWORDs to be transferred by the PLX DMA engine 0 when it is operating in demand mode.

The value programmed is one less than the desired number to transfer. Use 0 to transfer 1 DWORD, and 7 to transfer 8.

### 4.2.21 DEMAND DMA 1 TRANSFER COUNT REGISTER

*DSP Address:* 0x040087  
*PCI Address:* BAR2:0x10021C  
*Mode of Access:* Read/Write  
*Reset By* CPCI Hardware Reset, Software Reset, Watchdog Reset

This 8 bit register sets the number of DWORDs to be transferred by the PLX DMA engine 1 when it is operating in demand mode. It should be set to the same value as the PAE flag in the hardware FIFO.

The value programmed is one less than the desired number to transfer. Use 0 to transfer 1 DWORD, and 7 to transfer 8.

### 4.3 LOCAL FLASH

*DSP Address:* 0x900000 - 0x97FFFF, Bits 07-00  
*PCI Address:* Not Accessible  
*Mode of Access:* Read/Write in page mode

There is 512k x 8 of FLASH memory available to the DSP on the Local Bus. The first 64k is reserved for the use of the DSP Bootloader with the remainder available for customer applications. Access occurs with about 10 wait states due to the slow speed of the device.

Code examples of writing to this device is located in the Board Support Package.

### 4.4 PLX OPERATION REGISTERS

*DSP Address:* 0x880000 – 0x88005E  
*PCI Address:* BAR0/1:0x0 - 0xF8  
*Mode of Access:* Read/Write  
*Reset By* Depends upon register

The HOST processor can access the internal PLX registers through BAR0 and BAR1. BAR0 is accessed via normal memory operations and BAR1 is accessed via I/O operations.

The DSP can access these registers through normal memory cycles at the addresses specified.

The registers can be divided into several categories.

- Local Configuration Registers
- Runtime Registers
- DMA Registers

There are insufficient resources on the card to support I<sub>2</sub>O message queues, so these registers are not described.

**4.4.1 LOCAL CONFIGURATION REGISTERS**

DSP Address:            0x880020 – 0x88005E  
 PCI Address:            BAR0/1:0x0 – 0xF8  
 Mode of Access:        Read/Write  
 Reset By                CPCI Hardware Reset, Software  
                               Reset, Watchdog Reset

See the PLX PCI9080 Documentation for more details about these registers.

| HOST Address<br>BAR0/1: | DSP<br>Address | 31 – 24   | 23 – 16 | 15 – 8 | 7 – 0 |
|-------------------------|----------------|---|---------|--------|-------|
| 0x00                    | 0x880020       | Range for PCI to Local Address Space 0                    |         |        |       |
| 0x04                    | 0x880021       | Local Base Address for PCI to Local Address Space 0       |         |        |       |
| 0x08                    | 0x880022       | Mode / Arbitration Register                               |         |        |       |
| 0x0C                    | 0x880023       | Big / Little Endian Register                              |         |        |       |
| 0x10                    | 0x880024       | Range for PCI to Local Expansion ROM                      |         |        |       |
| 0x14                    | 0x880025       | Local Base Address for PCI to Local Expansion ROM         |         |        |       |
| 0x18                    | 0x880026       | Local Bus Region Descriptors                              |         |        |       |
| 0x1C                    | 0x880027       | Range for Direct Master to PCI                            |         |        |       |
| 0x20                    | 0x880028       | Local Base Address for Direct Master to PCI Memory        |         |        |       |
| 0x24                    | 0x880029       | Local Base Address for Direct Master to PCI IO/CFG        |         |        |       |
| 0x28                    | 0x88002A       | PCI Base Address for Direct Master to PCI                 |         |        |       |
| 0x2C                    | 0x88002B       | PCI Configuration Address for Direct Master to PCI IO/CFG |         |        |       |
| 0xF0                    | 0x88005C       | Range for PCI to Local Address Space 1                    |         |        |       |
| 0xF4                    | 0x88005D       | Local Base Address for PCI to Local Address Space 1       |         |        |       |
| 0xF8                    | 0x88005E       | Local Bus Region Descriptor for PCI to Local              |         |        |       |

**Table 4.12: PLX Local Configuration Registers**

**4.4.2 RUNTIME REGISTERS**

DSP Address:            0x880030 – 0x88003F

PCI Address:            BAR0/1:0x40 – 0x7C

Mode of Access:        Read/Write

Reset By                CPCI Hardware Reset

See the PLX PCI9080 Documentation for more details about these registers.

| HOST Address<br>BAR0/1: | DSP<br>Address | 31 – 24   | 23 – 16 | 15 – 8      | 7 – 0 |
|-------------------------|----------------|---|---------|-------------|-------|
| 0x40                    | 0x880030       | Mailbox Register 0                                  |         |             |       |
| 0x44                    | 0x880031       | Mailbox Register 1                                  |         |             |       |
| 0x48                    | 0x880032       | Mailbox Register 2                                  |         |             |       |
| 0x4C                    | 0x880033       | Mailbox Register 3                                  |         |             |       |
| 0x50                    | 0x880034       | Mailbox Register 4                                  |         |             |       |
| 0x54                    | 0x880035       | Mailbox Register 5                                  |         |             |       |
| 0x58                    | 0x880036       | Mailbox Register 6                                  |         |             |       |
| 0x5C                    | 0x880037       | Mailbox Register 7                                  |         |             |       |
| 0x60                    | 0x880038       | PCI to Local Doorbell Register                      |         |             |       |
| 0x64                    | 0x880039       | Local to PCI Doorbell Register                      |         |             |       |
| 0x68                    | 0x88003A       | Interrupt Control / Status                          |         |             |       |
| 0x6C                    | 0x88003B       | Serial EEPROM, PCI Command Codes, User<br>I/O, Init |         |             |       |
| 0x70                    | 0x88003C       | Device ID   |         | Vendor ID   |       |
| 0x74                    | 0x88003D       | Unused  |         | Revision ID |       |
| 0x78                    | 0x88003E       | Mailbox Register 0                                  |         |             |       |
| 0x7C                    | 0x88003F       | Mailbox Register 1                                  |         |             |       |

**Table 4.13: PLX Runtime Registers**

### 4.4.3 DMA REGISTERS

DSP Address:            0x880040 – 0x88004C  
 PCI Address:            BAR0/1:0x80 – 0xB0  
 Mode of Access:        Read/Write  
 Reset By                CPCI Hardware Reset, Software  
                               Reset, Watchdog Reset

See the PLX PCI9080 Documentation for more details about these registers.

| HOST Address<br>BAR0/1: | DSP<br>Address | 31 – 24                     | 23 – 16 | 15 – 8         | 7 – 0          |
|-------------------------|----------------|-----------------------------|---------|----------------|----------------|
| 0x80                    | 0x880040       | DMA Ch0 Mode                |         |                |                |
| 0x84                    | 0x880041       | DMA Ch0 PCI Address         |         |                |                |
| 0x88                    | 0x880042       | DMA Ch0 Local Address       |         |                |                |
| 0x8C                    | 0x880043       | DMA Ch0 Transfer Byte Count |         |                |                |
| 0x90                    | 0x880044       | DMA Ch0 Descriptor Pointer  |         |                |                |
| 0x94                    | 0x880045       | DMA Ch1 Mode                |         |                |                |
| 0x98                    | 0x880046       | DMA Ch1 PCI Address         |         |                |                |
| 0x9C                    | 0x880047       | DMA Ch1 Local Address       |         |                |                |
| 0xA0                    | 0x880048       | DMA Ch1 Transfer Byte Count |         |                |                |
| 0xA4                    | 0x880049       | DMA Ch1 Descriptor Pointer  |         |                |                |
| 0xA8                    | 0x88004A       | Reserved                    |         | DMA Ch1<br>CSR | DMA Ch0<br>CSR |
| 0xAC                    | 0x88004B       | Mode / Arbitration Register |         |                |                |
| 0xB0                    | 0x88004C       | DMA Threshold Register      |         |                |                |

**Table 4.14: PLX DMA Registers**

#### **4.5 CPCI PASS-THROUGH REGION**

DSP Address:            0xC00000 – 0xFFFFFFFF

Mode of Access:        Read/Write

The **CPCI-AD320** can directly access HOST memory and I/O ports on the CPCI system and the PMC Module through correctly programming the PLX interface. Up to 16 Mbytes of PCI address space can be mapped at a time.

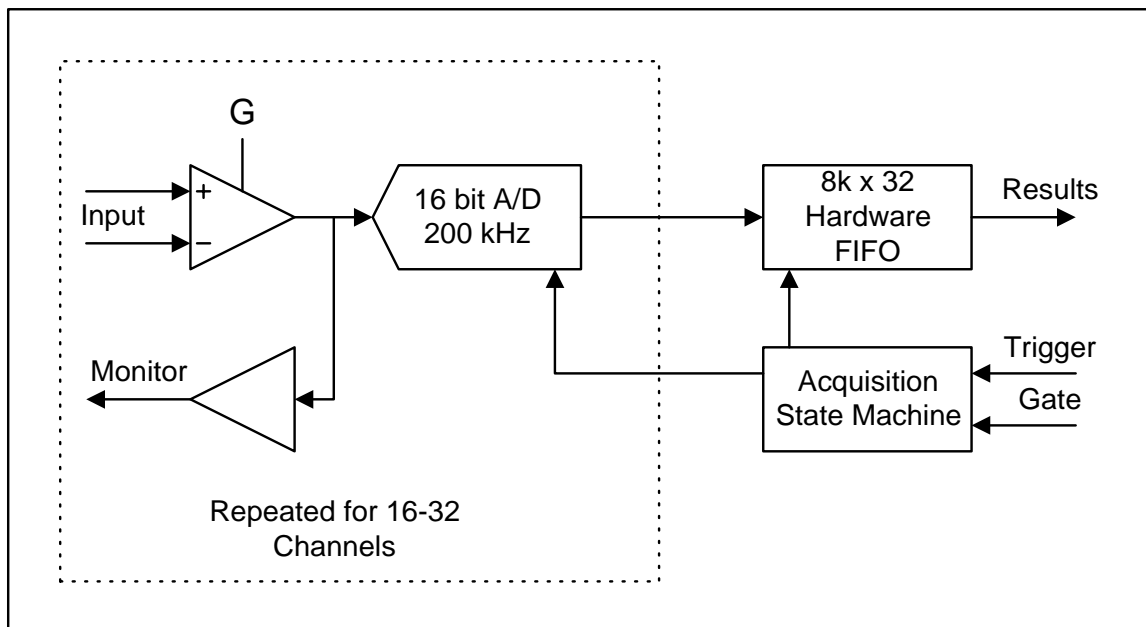
***NOTE: Windows NT/2000 and Windows 95/98 supports virtual memory and separate flat address spaces for each task. Physical memory pages are not contiguous.***

***There is support in the Board Support Package and alphi\_io DSP library to allow the DSP to directly access HOST memory on a per task basis.***

## 5. HARDWARE DETAILS

### 5.1 BOARD PERIPHERALS

#### 5.1.1 A/D CONVERTERS



**Figure 5.1: Main A/D Converters**

Each of the 16-32 main input channels (AIN01 – AIN32) has its own Programmable Gain Amplifier (PGA). Inputs are differential mode, and the gains can be selected under DSP control. Depending on factory input option, the gains are x1, x2, x4, and x8, x1, x2, x5, and x10, or optionally x1, x10, x100, and x1000. Individual channels can have different input options. Note that the X10, X100, and X1000 option will greatly reduce the input bandwidth, depending upon the gain selected. Contact the factory for more details.

16 channels reside on the main board, and an additional 16 channels reside on a daughterboard. The daughterboard is optional.

Upon receipt of a rising edge on the trigger when gate is high, the A/D converters simultaneously sample the output voltages from the PGAs and start a conversion. When the conversions are complete, a hardware state machine copies the conversion results to a hardware FIFO.

When a programmable number of samples are available in the FIFO, either the DSP can transfer them to the on board SRAM for use by the control loop, or the PLX CPCI Interface can DMA the conversion results immediately to the processor(s) on the PMC slot, or send them directly to HOST memory.

The DSP code and NT driver, provided in the Board Support Package, supports full scatter / gather type DMA to the HOST.

### 5.1.2 DIGITAL I/O

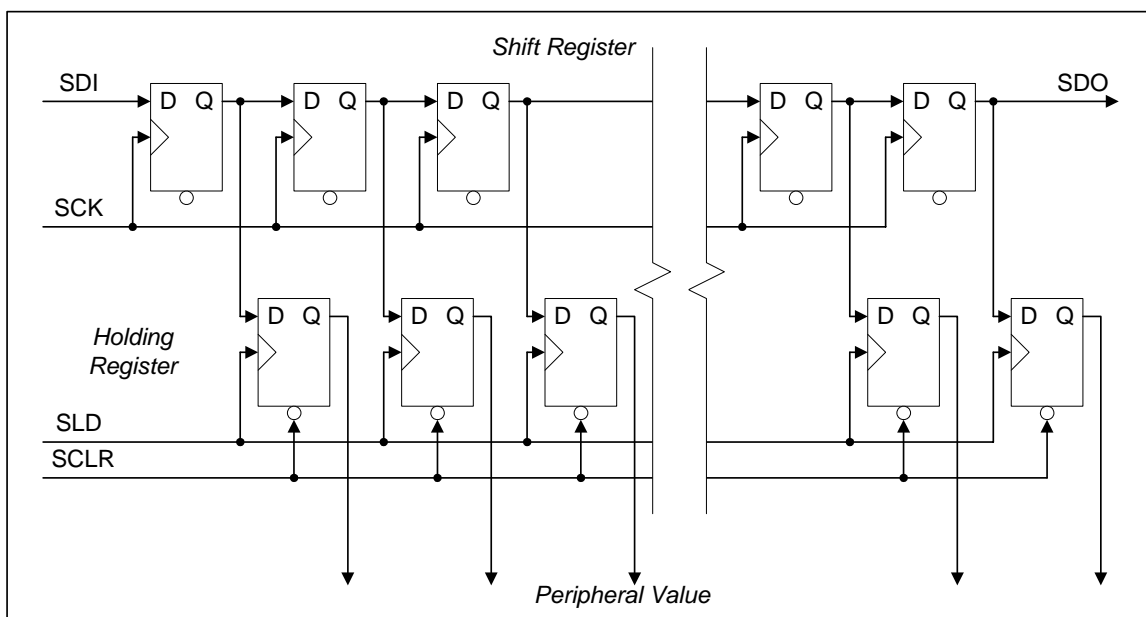
There are two 8 bit bi-directional digital ports. Each port can be set for input or output. There are 10k Ohm resistors serving as pull-ups to ensure that the lines will default to high on reset.

### 5.1.3 SERIAL PERIPHERAL CHAIN

The **CPCI-AD320** is designed to interface with a series of rear panel I/O modules which incorporate peripherals which are programmed using a serial bus. This bus is a chained serial bus which connect all the modules and daughter-boards in sequence. Each module and daughter may have different peripherals and the documentation for each module and daughter-board should be consulted for the overall programming format.

The software for this card will include functions to simplify the programming of this and any other RPIO Modules. See the software manuals for more details.

Details about the programming the devices on the RPIO modules is provided for reference.



**Figure 5.2: Serial Peripherals**

Each peripheral on the serial bus consists of four signals and five connections. These signals originate using a digital port at the A/D Acquisition card. The four signals (five connections) are as follows:

#### **SDI Serial Data In**

Serial stream of program information. Originated by A/D acquisition card, and possibly clocked through earlier devices in the chain.

#### **SDO Serial Data Out**

Serial stream of data which is clocked through the device to the next device in the chain. The number of bits between SDI and SDO is device dependent, and documented below.



### **SCK Serial Clock**

This signal clocks the data along the SDI/SDO chain of shift registers. It is suggested that both a rising edge and falling edge be present on SCK before any changes to the SDI for the next bit. The SCK is not toggled if peripherals are not being programmed.

### **SLD Serial Load**

A falling edge followed by a rising edge on this signal will transfer the contents of the shift registers on all devices to the holding registers on the devices, thus programming the device. All devices on the chain must be programmed at the same time.

### **SCLR Serial Clear**

A falling edge followed by a rising edge on this signal will clear the holding registers to a preset value, depending upon the device. The preset value depends upon the device, and some devices may not support it.

## **5.2 DMA**

There are a total of four DMA channels available on the **CPCI-AD320**. Two are located in the TMS320C32 DSP and two are located in the PLX 9080 PCI to DSP bridge.

### **5.2.1 DSP DMA**

There are two fully independent DMA channels in the DSP which can be used for such purposes as:

- Transferring the main A/D conversion results from hardware FIFO to SRAM memory.
- Performing transfers between the DSP local bus and the PCI, with a slight performance penalty, if the PCI window is set up in the PLX.

These DMA engines can be free-running, or they can be triggered from several DSP interrupt sources, such as:

- FIFO has a programmable number of samples ready. (DSP INT3)
- External trigger event, such as PXI trigger, external PCI device writing to a strobe register. (DSP INT1, source selected in the **Trigger / Gate Configuration Registers**)
- DSP timer causing a trigger. (Internal to DSP)

See the DSP Processor documentation for more details.

### **5.2.2 DSP TO PCI BRIDGE DMA**

The PLX 9080 DSP to PCI bridge contains two DMA engines for transferring between the DSP local bus and the PCI bus, either to the PMC or to the CPCI bus. These DMA engines are the most efficient means of transferring data between the two busses.

The DMA engines are capable of processing a chained list of transfer requests, and can generate interrupts to the DSP or to the HOST processor with each transfer. Scatter/Gather is supported with these chains of requests. The list of requests can reside in PCI memory or in SRAM on the card.

### 5.2.3 DEMAND MODE DMA

Additional logic on the card allow for control of the PLX DMA engines in demand mode. A programmed number of transfers can occur for each hardware request.

Demand mode is independent of the chains of requests. It is of use when scatter/gather modes are being used.

The DMA hardware is pre-assigned for certain tasks:

PLX DMA Engine 1 is intended to transfer the contents of the hardware FIFO to the PCI bus with a minimum of latency. When the PAE flag in the hardware FIFO indicates that more than a certain number of samples are available for transfer, the DMA will trigger, transferring that certain number. Profiling indicates that the time between data available in the FIFO to the request of the PCI bus for access will occur in 1  $\mu$ S.

PLX DMA Engine 0 is intended to be triggered by an external hardware event. This event could be a PXI trigger line, an external PCI device writing to a strobe register, or a DSP timer. A programmed number of samples is transferred for each trigger.

Of course, the demand modes do not have to be used, such as for programmed DMA transfers.

## 5.3 PXI

In 1997, National Instruments Corporation introduced an extension of the CPCI specification called PXI. The intent was to port some of the features of the VXI triggering bus to the CPCI realm.

One of the features of the PXI specification is a bus of 8 trigger lines which are common to all of the slots on a PXI compatible backplane.

By design or by coincidence, 6 of the 8 trigger lines defined by the PXI specification were already reserved and specified to be tied in common on the backplane, as per the CPCI specification.

Therefore, on a correct implementation of a CPCI compatible backplane, but non PXI compatible backplane, at least the first 6 trigger lines should be available for triggering between cards.

The **CPCI-AD320** is designed to make exhaustive use of the PXI trigger lines for communication and synchronization between other **CPCI-AD320** boards and other PXI compatible boards.

The **CPCI-AD320** is capable of driving the following signals to a PXI line:

- A constant 0 or 1, or a signal created by the DSP or PCI device toggling the bit which is output to the PXI trigger line.
- A timing source generated by either of the DSP timers.
- Either the Clock Input or the Gate Input from the front panel connector or through the rear panel I/O connector.
- A pulse generated by a write to a register by either the DSP or another PCI device.

Of course, the trigger output can be tri-stated when it is not used or is for input.

The **CPCI-AD320** is capable of performing the following actions based on a PXI trigger:

- Provide a trigger and a gate to the A/D conversion hardware.
- Outputting the signal to the Clock Output at the front panel connector or through the rear panel I/O connector.
- Provide an interrupt to the HOST.
- Provide an interrupt to the DSP.
- Provide a trigger of the DSP DMA engines.
- Provide a trigger of one of the PLX DMA engines.
- Can be read by the DSP or PCI processor to determine its current state.

## 5.4 INTERRUPTS

### 5.4.1 DSP INTERRUPTS

The TMS320C32 DSP processor has four external interrupt sources. They are called INT0 – INT3. The sources of these interrupts are described below.

#### INT0

INT0 is dedicated to handling PLX9080 issues. This assertion of either LINTO# or LSERR# by the PLX will generate INT0. The DSP can query the **9080 Control / Status Register** bits **LINTO** and **LSERR** to determine the cause of the interrupt, and determine that both signals are HIGH before returning from the interrupt handler.

Individual bits in the PLX will enable the following sources:

- DMA Completion. (**LINTO**)
- DMA Terminal Count Reached. (**LINTO**)
- One or more bits in Doorbell register are set. (**LINTO**)
- PCI write to a Mailbox. (**LINTO**)
- Master Abort on PCI bus. (**LSERR**)
- Target Abort on PCI bus. (**LSERR**)
- Retry count exceeded on PCI bus. (**LSERR**)
- Parity Error on PCI bus. (**LSERR**)

### **INT1**

INT1 is dedicated to handling an interrupt from the source selected in the **Trigger / Gate Configuration Registers**. The following sources can be connected to this interrupt:

- Rising edge on the Clock Input or the Gate Input from the front panel connector or through the rear panel I/O connector.
- Rising edge on a PXI trigger line.
- External PCI device writing to one of the strobe registers.

This interrupt line can be used to trigger a DSP DMA engine, or be handled as an interrupt, of both.

### **INT2**

INT2 is a catchall for the other available interrupt sources. Interrupts can be generated by the following:

- 8530 Serial Interface.
- PMC Module's PCI Interrupt.
- A falling edge on the EXT INT line from the rear panel I/O.

Interrupt enables and status bits are available in the **DSP Interrupt Status Register** and the **DSP Interrupt Enable Register**.

Note that the PMC interrupt can be turned off from interrupting the HOST by setting the **DISABLE PMC INT** bit in the **Board Control / Status Register**. Either the HOST or the DSP should handle the PMC interrupt.

### **INT3**

INT3 is dedicated to handling the A/D hardware FIFO. An interrupt is generated when the PAE line from the FIFO indicates that there are a programmable number of samples available. The FIFO will need to be emptied to reset this interrupt.

This interrupt line can be used to trigger a DSP DMA engine, or be handled as an interrupt, of both.

## **5.4.2 HOST INTERRUPTS**

The PLX can interrupt the CPCI HOST from any of the following causes.

- DMA Completion.
- DMA Terminal Count Reached.
- One or more bits in Doorbell register are set.
- Master Abort on PCI bus.
- Target Abort on PCI bus.
- Retry count exceeded on PCI bus.
- Parity Error on PCI bus.

Individual bits in the PLX will enable the sources. Additionally, the following hardware source can generate a CPCI HOST interrupt.

- HOST interrupt source selected in the Trigger / Gate Configuration Registers.

### 5.5 RESET

The **CPCI-AD320** is reset by several different means.

- PCI Hardware RESET
- Software RESET from a PCI device
- Watchdog RESET

Additionally, it is possible to hold the DSP in reset after a software reset, to allow for loading DSP code, as well as performing any other operation to the card hardware.

#### 5.5.1 PCI HARDWARE RESET

The entire card is reset when the PCI reset line is held low by the CPCI bus. All of the card's registers are reset as described in this manual, and the D/A converters will output 0 Volts. The PLX is fully reset, and the NVRAM image is automatically read by the PLX.

All access by the CPCI bus is locked out until either the DSP sets the **Local Init Status** bit in the **CNTRL** register of the PLX, or the DSP sets the **NB** bit in the **DSP Bootmode Register**.

The DSP will boot into the mode selected in the **DSP Bootmode Register**.

#### 5.5.2 SOFTWARE RESET FROM A PCI DEVICE

A PCI device can reset the DSP, the card registers, and partially reset the PLX. Additionally, the DSP can be held in RESET, after the software is complete.

The reset is accomplished by setting the **PCI Adapter Software Reset** bit in the PLX **CNTRL** register to a 1. After 200 mS, this bit needs to be set to a 0.

The DSP will be forced into reset, the card registers will reset, the D/A converters will output 0 Volts, and the PLX Local Configuration and PLX DMA registers will be reset. This will stop any active DMA, and will eliminate the passthru region BAR2. Any access to BAR2 by the PCI bus will not be acknowledged. Behavior of accessing a region which is not acknowledged is machine dependent.

After the reset is complete, one of two things needs to occur. One is that the PCI device toggle the **Reload Configuration Registers** bit in the PLX **CNTRL** register. This forces the PLX to reload from the NVRAM, thus re-enabling the passthru region. The other possibility is that the DSP is free to run, which will reload the PLX registers from the NVRAM.

#### 5.5.3 HOLDING DSP IN RESET

If it is desired to hold the DSP in reset, the **General Purpose Output** bit in the **CNTRL** register of the PLX should be set to 0 at the same time as the **PCI Adapter Software Reset** is set high. Leave the **General Purpose Output** bit low for as long as it is desired to hold the DSP.

The DSP boot mode can be set in the **DSP Bootmode Register**.

#### **5.5.4 WATCHDOG RESET**

The **CPCI-AD320** incorporates a watchdog timer, which can optionally be used.

At any RESET cause, the hardware will automatically generate reset strobes to the watchdog timer, to prevent the board from being reset.

If the DSP software desires to make use of the watchdog timer, it makes periodic writes to the **Reset Watchdog Timer** register. The first write will set the hardware into a mode which requires periodic reset of the timer with further writes to **Reset Watchdog Timer**.

In the event that the reset has not occurred within between 600 and 1000 mS, the Watchdog timer will force a reset.

The DSP will be forced into reset, the card registers will reset, the D/A converters (if present) will output 0 Volts, digital lines will tri-state and pull high, and the PLX Local Configuration and PLX DMA registers will be reset. This will stop any active DMA, and will eliminate the passthru region BAR2. Any access to BAR2 by the PCI bus will not be acknowledged. Behavior of accessing a region which is not acknowledged is machine dependent.

This reset will also reset the **DSP Bootmode Register**, which will force the DSP to boot from the FLASH device.

After the reset is complete, the DSP is free to run, which will reload the PLX registers from the NVRAM. This will re-enable the passthru region at BAR2.

#### **5.5.5 DSP BOOT MODES**

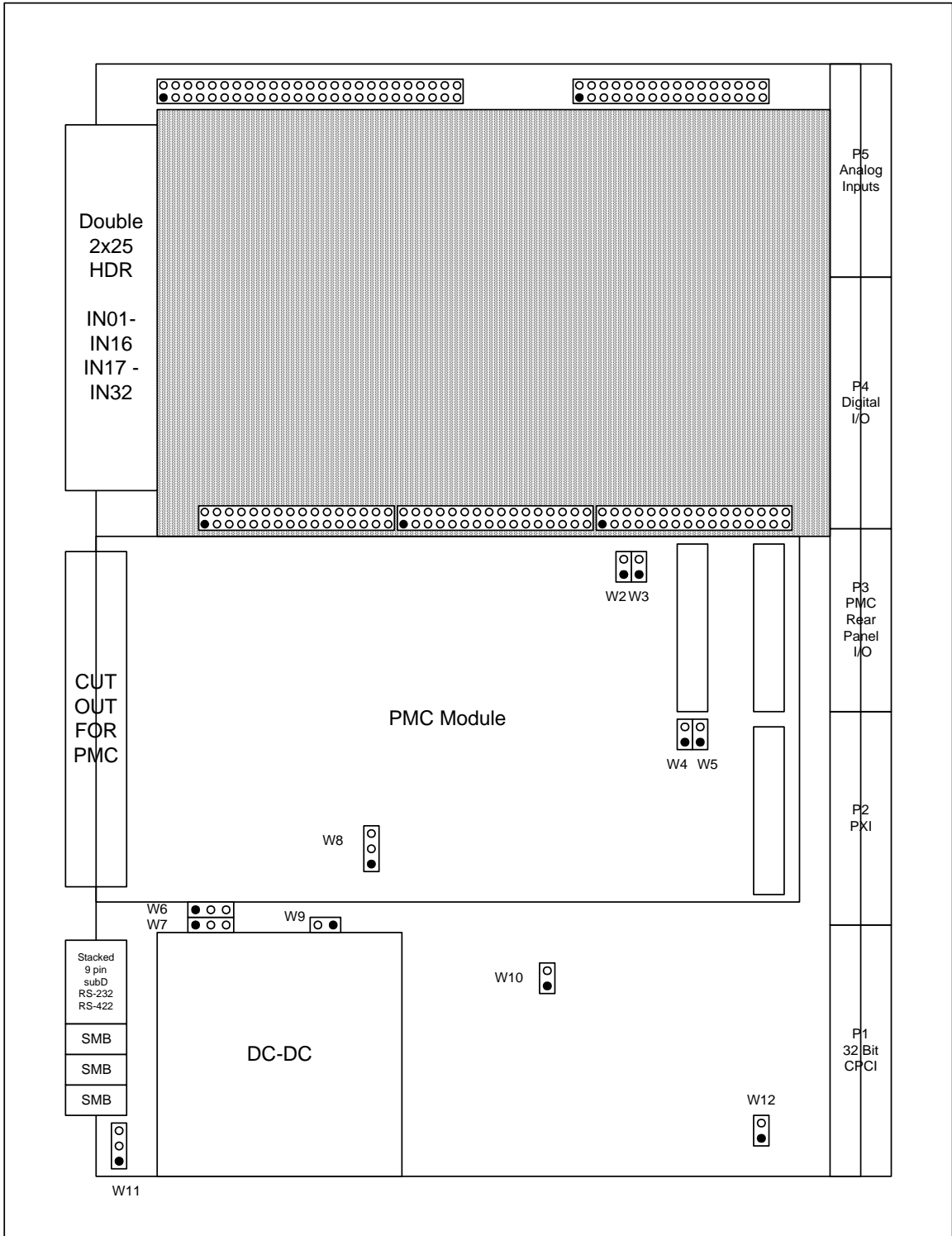
The DSP can be booted from several sources, once it is allowed to run. The choices are as follows.

- Booting a ROM image from FLASH device at 0x900000.
- Booting a ROM image from SRAM at 0x1000. This requires that the DSP be held in RESET, using the mechanism described in the RESET section, and an external PCI device copy the ROM image to the SRAM.
- Directly executing an executable image in SRAM at the reset vector located at 0x0. This requires that the DSP be held in RESET, using the mechanism described in the RESET section, and an external PCI device copy the executable image to the SRAM.

Determination of the boot source is made depending upon the settings in the **DSP Bootmode Register**.

### 5.6 CONNECTORS, JUMPERS, AND LEDS

The jumper and connector placement is depicted below.



**Figure 5.1: Jumper and Connector Locations**

**5.6.1 JUMPER DESCRIPTIONS**

| <b>JUMPER</b> | <b>FACTORY SETTING</b> | <b>DESCRIPTION</b>  |
|---------------|------------------------|---|
| W1            | None                   | Does not exist.   |
| W2            | 1-2                    | Factory use. Always connect 1-2.  |
| W3            | None                   | Factory use. Never connect.   |
| W4            | None                   | Not populated in this configuration.  |
| W5            | None                   | Not populated in this configuration.  |
| W6            | 2-3                    | Select output to RS422 pair 6 and 7. 1-2 to output TXCLK generated by 8530. 2-3 to output RTS from the 8530. RTS is default.  |
| W7            | 2-3                    | Select input from RS422 pair 8 and 9. 1-2 to connect to receive clock of 8530; 2-3 to connect to CTS of 8530. CTS is default.   |
| W8            | 2-3                    | Factory use. Always connect 2-3.  |
| W9            | None                   | RS422 Driver Mode. If present, drive both outputs on RTS; otherwise drive always. Drive always is default.  |
| W10           | 2-3                    | Provides an identical RESET to that of the watchdog timer.  |
| W11           | 1-2                    | Connect 1-2 in this configuration.  |
| W12           | None                   | W12 is used at the factory to supply 3.3 volts to certain components when a CPCI bus is not present. It should not be installed when the card is in a CPCI backplane. |

**Table 5.15 Jumper Descriptions**



5.6.2 FRONT PANEL DESCRIPTION

The following picture shows the front panel.

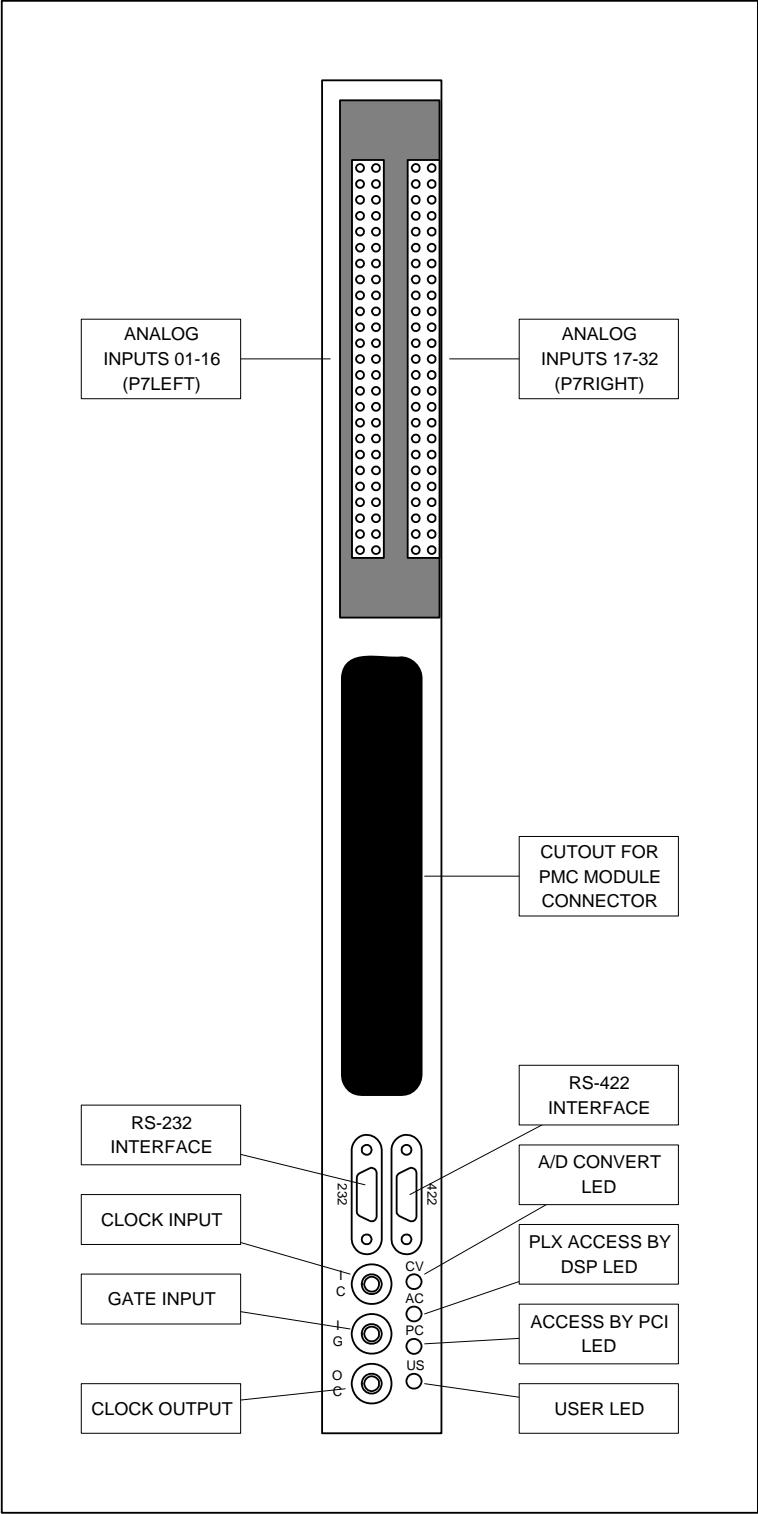
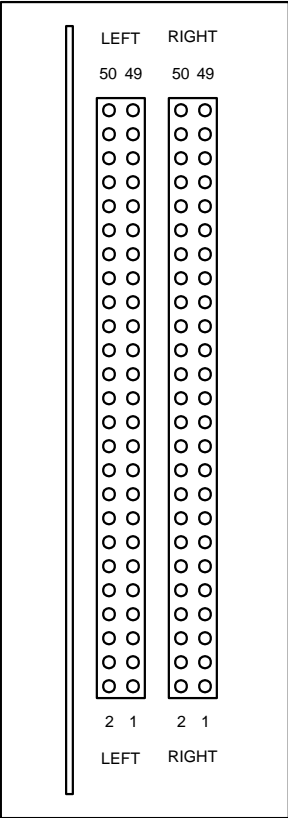


Figure 5.2: Front Panel

**Analog Input Connector (P7)**

A pair of 50 pin ribbon-style connectors are used to connect the analog input signals to this card. ALPHI Technology can supply transition modules and cable assemblies to meet any special requirements. Contact the factory for additional information.

Pins are numbered according to the following diagram. To simplify the description of the connections, P7 is split into two parts, P7LEFT, and P7RIGHT to represent the left and right sides of the connector.



**Figure 5.3: Analog Input Connector (P7)**

| Pin | Connection | Pin | Connection |
|-----|------------|-----|------------|
| 50  | AGND       | 49  | AGND       |
| 48  | AIN01+     | 47  | AIN01-     |
| 46  | AIN02+     | 45  | AIN02-     |
| 44  | AGND       | 43  | AGND       |
| 42  | AIN03+     | 41  | AIN03-     |
| 40  | AIN04+     | 39  | AIN04-     |
| 38  | AGND       | 37  | AGND       |
| 36  | AIN05+     | 35  | AIN05-     |
| 34  | AIN06+     | 33  | AIN06-     |
| 32  | AGND       | 31  | AGND       |
| 30  | AIN07+     | 29  | AIN07-     |
| 28  | AIN08+     | 27  | AIN08-     |
| 26  | AGND       | 25  | AGND       |
| 24  | AIN09+     | 23  | AIN09-     |
| 22  | AIN10+     | 21  | AIN10-     |
| 20  | AGND       | 19  | AGND       |
| 18  | AIN11+     | 17  | AIN11-     |
| 16  | AIN12+     | 15  | AIN12-     |
| 14  | AGND       | 13  | AGND       |
| 12  | AIN13+     | 11  | AIN13-     |
| 10  | AIN14+     | 9   | AIN14-     |
| 8   | AGND       | 7   | AGND       |
| 6   | AIN15+     | 5   | AIN15-     |
| 4   | AIN16+     | 3   | AIN16-     |
| 2   | AGND       | 1   | AGND       |

**Table 5.16: Analog Input Connector (P7LEFT)**

| Pin | Connection | Pin | Connection |
|-----|------------|-----|------------|
| 50  | AGND       | 49  | AGND       |
| 48  | AIN17+     | 47  | AIN17-     |
| 46  | AIN18+     | 45  | AIN18-     |
| 44  | AGND       | 43  | AGND       |
| 42  | AIN19+     | 41  | AIN19-     |
| 40  | AIN20+     | 39  | AIN20-     |
| 38  | AGND       | 37  | AGND       |
| 36  | AIN21+     | 35  | AIN21-     |
| 34  | AIN22+     | 33  | AIN22-     |
| 32  | AGND       | 31  | AGND       |
| 30  | AIN23+     | 29  | AIN23-     |
| 28  | AIN24+     | 27  | AIN24-     |
| 26  | AGND       | 25  | AGND       |
| 24  | AIN25+     | 23  | AIN25-     |
| 22  | AIN26+     | 21  | AIN26-     |
| 20  | AGND       | 19  | AGND       |
| 18  | AIN27+     | 17  | AIN27-     |
| 16  | AIN28+     | 15  | AIN28-     |
| 14  | AGND       | 13  | AGND       |
| 12  | AIN29+     | 11  | AIN29-     |
| 10  | AIN30+     | 9   | AIN30-     |
| 8   | AGND       | 7   | AGND       |
| 6   | AIN31+     | 5   | AIN31-     |
| 4   | AIN32+     | 3   | AIN32-     |
| 2   | AGND       | 1   | AGND       |

**Table 5.17: Analog Input Connector (P7RIGHT)**

**CUTOUT FOR PMC MODULE CONNECTOR**

This cutout allows the front panel from the PMC module to show through the front panel. If no PMC module is present, then a filler panel will be installed.

**RS-232 INTERFACE CONNECTOR**

A 9 pin subminiature D shelled connector is used to route the RS-232 signals off the card. Port A of the 8530 is configured as the RS-232 port, and it serves as the console output for the bootloader and any DSP programs linked with the ALPHI\_IO.LIB library discussed in the **DSP Support Library** documentation.

Connectors are manufactured by ITT Cannon.

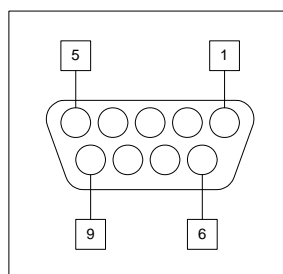
| Use            | Model        |
|----------------|--------------|
| On PC Board    | MDSM-9PE-C10 |
| Suggested Plug | MDSM-9SC-Z11 |

**Table 5.2: Serial Connector Model Numbers**

The pinout is described in the table below.

| Pin | Description   | Pin | Description     |
|-----|---------------|-----|-----------------|
| 1   | No Connection | 2   | Transmit Data   |
| 3   | Receive Data  | 4   | Clear To Send   |
| 5   | Ground        | 6   | Request To Send |
| 7   | Ground        | 8   | No Connection   |
| 9   | No Connection |     |                 |

**Table 5.3: Serial RS232 Port (P4)**



**Figure 5.2: Serial RS232 Port (P4)**

**RS-422 INTERFACE CONNECTOR**

A 9 pin subminiature D shelled connector is used to route the RS-422 signals off the card. Port B of the 8530 is configured as the RS-422 port.

Connectors are manufactured by ITT Cannon.

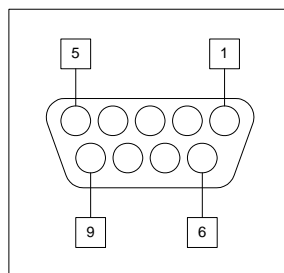
| Use            | Model        |
|----------------|--------------|
| On PC Board    | MDSM-9PE-C10 |
| Suggested Plug | MDSM-9SC-Z11 |

**Table 5.2: Serial Connector Model Numbers**

The pinout is described in the table below.

| Pin | Description       | Pin | Description       |
|-----|-------------------|-----|-------------------|
| 1   | Transmit Data +   | 2   | Transmit Data-    |
| 3   | Receive Data +    | 4   | Receive Data -    |
| 5   | Ground            | 6   | Request To Send + |
| 7   | Request To Send - | 8   | Clear To Send +   |
| 9   | Clear To Send -   |     |                   |

**Table 5.3: Serial RS232 Port (P4)**



**Figure 5.2: Serial RS232 Port (P4)**

### **CLOCK INPUT**

This SMB connector can provide the CLOCK INPUT signal to the card. The input signal is a TTL compatible signal with pull-up resistors. It also can be read by the DSP or a PCI processor. The connector is labeled “IC” on the front panel.

This signal is also available at the rear panel.

### **GATE INPUT**

This SMB connector can provide the GATE INPUT signal to the card. The input signal is a TTL compatible signal with pull-up resistors. It also can be read by the DSP or a PCI processor. The connector is labeled “IC” on the front panel.

This signal is also available at the rear panel.

### **CLOCK OUTPUT**

This SMB connector routes the CLOCK OUTPUT signal off of the card. The output signal is an open drain TTL compatible signal with pull-up resistors. It cannot be read back. The connector is labeled “OC” on the front panel.

This signal is also available at the rear panel.

### **A/D CONVERT LED**

When this LED is glowing, the A/D converters are being triggered. The LED is labeled “CV” on the front panel.

### **PLX ACCESS BY DSP LED**

When this LED is glowing, the DSP is accessing registers on the PLX. The LED is labeled “AC” on the front panel.

### **ACCESS BY PCI LED**

When this LED is glowing, the PLX has been granted access to the Local Bus, usually for access by the PCI bus. The LED is labeled “PC” on the front panel.

### **USER LED**

This LED will glow as a result of setting the **USER LED** bit in the **Null Pace / Limit Register**. The LED is labeled “US” on the front panel.

**5.6.3 REAR PANEL DESCRIPTION**

**32 Bit CPCI Bus Connection (J1)**

This connector plugs into the backplane and provides the standard CPCI signals for all CPCI systems. See the CPCI Bus Documentation for details.

**PXI Trigger Extension Bus (J2)**

This connector plugs into the backplane and provides the PXI triggering connections for PXI systems. It is compatible with both a PXI backplane and a standard 64 bit CPCI backplane.

| PIN | A       | B       | C       | D | E       | F   |
|-----|---------|---------|---------|---|---------|-----|
| 22  |         |         |         |   |         | GND |
| 21  |         | GND     |         |   |         | GND |
| 20  |         |         |         |   |         | GND |
| 19  |         | GND     |         |   |         | GND |
| 18  | PXITRG3 | PXITRG4 | PXITRG5 |   | PXITRG6 | GND |
| 17  | PXITRG2 | GND     |         |   |         | GND |
| 16  | PXITRG1 | PXITRG0 |         |   | PXITRG7 | GND |
| 15  |         | GND     |         |   |         | GND |
| 14  |         |         |         |   |         | GND |
| 13  |         | GND     |         |   |         | GND |
| 12  |         |         |         |   |         | GND |
| 11  |         | GND     |         |   |         | GND |
| 10  |         |         |         |   |         | GND |
| 9   |         | GND     |         |   |         | GND |
| 8   |         |         |         |   |         | GND |
| 7   |         | GND     |         |   |         | GND |
| 6   |         |         |         |   |         | GND |
| 5   |         | GND     |         |   |         | GND |
| 4   |         |         |         |   |         | GND |
| 3   |         | GND     |         |   |         | GND |
| 2   |         |         |         |   |         | GND |
| 1   |         | GND     |         |   |         | GND |

**Table 5.18: PXI Trigger Extension Bus (J2)**

**PMC Module Rear Panel I/O Connection (J3)**

This connector brings the rear panel I/O connector of the PMC module to the rear panel. The pinout specified is the standard one for a PMC module installed into slot 2 on a 6U carrier board.

| PIN | A       | B       | C       | D       | E       | F   |
|-----|---------|---------|---------|---------|---------|-----|
| 19  |         |         |         |         |         | GND |
| 18  |         |         |         |         |         | GND |
| 17  |         |         |         |         |         | GND |
| 16  |         |         |         |         |         | GND |
| 15  |         |         |         |         |         | GND |
| 14  | +5      | +5      | +3.3    | +3.3    | +3.3    | GND |
| 13  | PMCIO00 | PMCIO01 | PMCIO02 | PMCIO03 | PMCIO04 | GND |
| 12  | PMCIO05 | PMCIO06 | PMCIO07 | PMCIO08 | PMCIO09 | GND |
| 11  | PMCIO10 | PMCIO11 | PMCIO12 | PMCIO13 | PMCIO14 | GND |
| 10  | PMCIO15 | PMCIO16 | PMCIO17 | PMCIO18 | PMCIO19 | GND |
| 9   | PMCIO20 | PMCIO21 | PMCIO22 | PMCIO23 | PMCIO24 | GND |
| 8   | PMCIO25 | PMCIO26 | PMCIO27 | PMCIO28 | PMCIO29 | GND |
| 7   | PMCIO30 | PMCIO31 | PMCIO32 | PMCIO33 | PMCIO34 | GND |
| 6   | PMCIO35 | PMCIO36 | PMCIO37 | PMCIO38 | PMCIO39 | GND |
| 5   | PMCIO40 | PMCIO41 | PMCIO42 | PMCIO43 | PMCIO44 | GND |
| 4   | PMCIO45 | PMCIO46 | PMCIO47 | PMCIO48 | PMCIO49 | GND |
| 3   | PMCIO50 | PMCIO51 | PMCIO52 | PMCIO53 | PMCIO54 | GND |
| 2   | PMCIO55 | PMCIO56 | PMCIO57 | PMCIO58 | PMCIO59 | GND |
| 1   | PMCIO60 | PMCIO61 | PMCIO62 | PMCIO63 | +5      | GND |

**Table 5.19: PMC Module Rear Panel I/O Connection (J3)**



**Analog Outputs and Digital Connection to Rear Panel I/O Module (J4)**

| PIN     | A        | B            | C      | D      | E      | F   |
|---------|----------|--------------|--------|--------|--------|-----|
| 25      |          |              | AOUT01 | AGND   | AOUT02 | GND |
| 24      | AGND     |              |        | AOUT03 | AGND   | GND |
| 23      | AOUT04   | AGND         |        |        | AOUT05 | GND |
| 22      | AGND     | AOUT06       | AGND   |        |        | GND |
| 21      | AOUT07   | AGND         | AOUT08 | AGND   |        | GND |
| 20      |          |              |        |        |        | GND |
| 19      |          |              |        |        |        | GND |
| 18      |          |              |        |        |        | GND |
| 17      |          |              |        |        |        | GND |
| 16      |          |              |        |        |        | GND |
| 15      | +3.3     | +3.3         | +3.3   | +5     | +5     | GND |
| 12 - 14 | KEY AREA |              |        |        |        |     |
| 11      | RXD0     | TXD0         | RTS0   | CTS0   | PA_04  | GND |
| 10      | PA_06    |              | PA_02  | PB_02  |        | GND |
| 9       | PB_04    | PB_06        | PB_00  | SCK    | SLD    | GND |
| 8       | EXT INT  | FAULT        |        |        |        | GND |
| 7       | LIMIT    | NULL<br>PACE |        |        |        | GND |
| 6       |          | PA_01        | PA_03  |        | PA_05  | GND |
| 5       | PA_07    |              | PB_01  | PB_03  |        | GND |
| 4       | PB_05    | PB_07        |        |        | SRST   | GND |
| 3       | TXD1-    | RTS1+        | RTS1-  | CTS1+  | CTS1-  | GND |
| 2       | PA_00    | RXD1+        | RXD1-  | SDI    | TXD1+  | GND |
| 1       | +3.3     | +3.3         | +3.3   | +5     | +5     | GND |

**Table 5.20: Analog Outputs and Digital Connection to Rear Panel I/O Module (J4)**

**Analog Inputs Connection to Rear Panel I/O Module (J5)**

Note that channels 09-16 and channels 17-24 are swapped from the RPIO documentation, in order to match correctly with the RPIO modules.

Channels 01-08 will be located on the Primary RPIO Module.

Channels 09-16 will be located on the Secondary RPIO Module.

Channels 17-24 will be located on the Primary RPIO Module's Daughter Board.

Channels 25-32 will be located on the Secondary RPIO Module's Daughter Board.

| PIN | A      | B      | C      | D      | E      | F   |
|-----|--------|--------|--------|--------|--------|-----|
| 22  |        |        | AIN17+ | AIN01+ | AIN18+ | GND |
| 21  | AIN02+ |        |        | AIN19+ | AIN03+ | GND |
| 20  | AIN20+ | AIN04+ |        |        | AIN21+ | GND |
| 19  | AIN05+ | AIN22+ | AIN06+ |        |        | GND |
| 18  | AIN23+ | AIN07+ | AIN24+ | AIN08+ |        | GND |
| 17  |        | AIN17- | AIN01- | AIN18- | AIN02- | GND |
| 16  |        |        | AIN19- | AIN03- | AIN20- | GND |
| 15  | AIN04- |        |        | AIN21- | AIN05- | GND |
| 14  | AIN22- | AIN06- |        |        | AIN23- | GND |
| 13  | AIN07- | AIN24- | AIN08- |        |        | GND |
| 12  | +3.3   | +3.3   | +3.3   | +5     | +5     | GND |
| 11  |        |        | AIN25+ | AIN09+ | AIN26+ | GND |
| 10  | AIN10+ |        |        | AIN27+ | AIN11+ | GND |
| 9   | AIN28+ | AIN12+ |        |        | AIN29+ | GND |
| 8   | AIN13+ | AIN30+ | AIN14+ |        |        | GND |
| 7   | AIN31+ | AIN15+ | AIN32+ | AIN16+ |        | GND |
| 6   |        | AIN25- | AIN09- | AIN26- | AIN10- | GND |
| 5   |        |        | AIN27- | AIN11- | AIN28- | GND |
| 4   | AIN12- |        |        | AIN29- | AIN13- | GND |
| 3   | AIN30- | AIN14- |        |        | AIN31- | GND |
| 2   | AIN15- | AIN32- | AIN16- |        |        | GND |
| 1   | +3.3   | +3.3   | +3.3   | +5     | +5     | GND |

**Table 5.21: Analog Inputs Connection to Rear Panel I/O Module (J5)**

**5.6.4 CONNECTORS ON COMPONENT SIDE DESCRIPTION**

**Emulator Connector (P9)**

This connector is used to connect the emulator to the C32 DSP.

**Factory Use (P8)**

This connector is used at the factory for programming the FPGA.