CPCI-RPIO-HDR

Rear I/O Panel
Up to Four IndustryPack® Modules

REFERENCE MANUAL

740-13-002-4000
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ALPHI TECHNOLOGY CORPORATION

6202 S. Maple Avenue #120
Tempe, AZ 85283 USA
Tel: (480) 838-2428
Fax: (480) 838-4477

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Part Number : 740-13-002-4000

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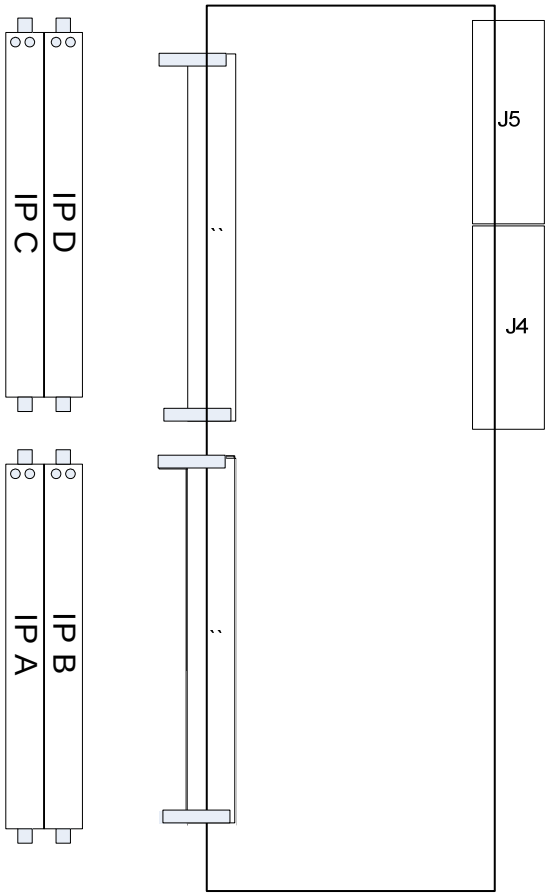
1. GENERAL DESCRIPTION

1.1 INTRODUCTION

The CPCI-RPIO-HDR is a 6U rear I/O inter-connect panel that match PICMG 2.4 R10 Standard CPCI industry pack carrier. The CPCI-RPIO-HDR plugs into the read of a 6U CPCI chassis and routes all four (A, B, C, D) of the IPs I/O line to four 50 pin IDE Header connectors. The connection is 1 to 1, 2 to 2, 3 to 3 and so on for all 50 lines for each of the IP's.



2. Industry Pack A pinout

IP I/O Line	HDR Pin	J4 Backplane and Pin
IP_A:1	1	A11
IP_A:2	2	B11
IP_A:3	3	C11
IP_A:4	4	D11
IP_A:5	5	E11
IP_A:6	6	A10
IP_A:7	7	B10
IP_A:8	8	C10
IP_A:9	9	D10
IP_A:10	10	E10
IP_A:11	11	A9
IP_A:12	12	B9
IP_A:13	13	C9
IP_A:14	14	D9
IP_A:15	15	E9
IP_A:16	16	A8
IP_A:17	17	B8
IP_A:18	18	C8
IP_A:19	19	D8
IP_A:20	20	E8
IP_A:21	21	A7
IP_A:22	22	B7
IP_A:23	23	C7
IP_A:24	24	D7
IP_A:25	25	E7
IP_A:26	26	A6
IP_A:27	27	B6
IP_A:28	28	C6
IP_A:29	29	D6
IP_A:30	30	E6
IP_A:31	31	A5
IP_A:32	32	B5
IP_A:33	33	C5
IP_A:34	34	D5
IP_A:35	35	E5
IP_A:36	36	A4
IP_A:37	37	B4
IP_A:38	38	C4
IP_A:39	39	D4
IP_A:40	40	E4
IP_A:41	41	A3
IP_A:42	42	B3
IP_A:43	43	C3
IP_A:44	44	D3
IP_A:45	45	E3
IP_A:46	46	A2
IP_A:47	47	B2
IP_A:48	48	C2
IP_A:49	49	D2
IP_A:50	50	E2

3. Industry Pack B pinout

IP I/O Line	HDR Pin	J4 Backplane and Pin
IP_B:1	1	A25
IP_B:2	2	B25
IP_B:3	3	C25
IP_B:4	4	D25
IP_B:5	5	E25
IP_B:6	6	A24
IP_B:7	7	B24
IP_B:8	8	C24
IP_B:9	9	D24
IP_B:10	10	E24
IP_B:11	11	A23
IP_B:12	12	B23
IP_B:13	13	C23
IP_B:14	14	D23
IP_B:15	15	E23
IP_B:16	16	A22
IP_B:17	17	B22
IP_B:18	18	C22
IP_B:19	19	D22
IP_B:20	20	E22
IP_B:21	21	A21
IP_B:22	22	B21
IP_B:23	23	C21
IP_B:24	24	D21
IP_B:25	25	E21
IP_B:26	26	A20
IP_B:27	27	B20
IP_B:28	28	C20
IP_B:29	29	D20
IP_B:30	30	E20
IP_B:31	31	A19
IP_B:32	32	B19
IP_B:33	33	C19
IP_B:34	34	D19
IP_B:35	35	E19
IP_B:36	36	A18
IP_B:37	37	B18
IP_B:38	38	C18
IP_B:39	39	D18
IP_B:40	40	E18
IP_B:41	41	A17
IP_B:42	42	B17
IP_B:43	43	C17
IP_B:44	44	D17
IP_B:45	45	E17
IP_B:46	46	A16
IP_B:47	47	B16
IP_B:48	48	C16
IP_B:49	49	D16
IP_B:50	50	E16

4. Industry Pack C pinout

IP I/O Line	HDR Pin	J5 Backplane and Pin
IP_C:1	1	A11
IP_C:2	2	B11
IP_C:3	3	C11
IP_C:4	4	D11
IP_C:5	5	E11
IP_C:6	6	A10
IP_C:7	7	B10
IP_C:8	8	C10
IP_C:9	9	D10
IP_C:10	10	E10
IP_C:11	11	A9
IP_C:12	12	B9
IP_C:13	13	C9
IP_C:14	14	D9
IP_C:15	15	E9
IP_C:16	16	A8
IP_C:17	17	B8
IP_C:18	18	C8
IP_C:19	19	D8
IP_C:20	20	E8
IP_C:21	21	A7
IP_C:22	22	B7
IP_C:23	23	C7
IP_C:24	24	D7
IP_C:25	25	E7
IP_C:26	26	A6
IP_C:27	27	B6
IP_C:28	28	C6
IP_C:29	29	D6
IP_C:30	30	E6
IP_C:31	31	A5
IP_C:32	32	B5
IP_C:33	33	C5
IP_C:34	34	D5
IP_C:35	35	E5
IP_C:36	36	A4
IP_C:37	37	B4
IP_C:38	38	C4
IP_C:39	39	D4
IP_C:40	40	E4
IP_C:41	41	A3
IP_C:42	42	B3
IP_C:43	43	C3
IP_C:44	44	D3
IP_C:45	45	E3
IP_C:46	46	A2
IP_C:47	47	B2
IP_C:48	48	C2
IP_C:49	49	D2
IP_C:50	50	E2

5. Industry Pack D pinout

IP I/O Line	HDR Pin	J5 Backplane and Pin
IP_D:1	1	A22
IP_D:2	2	B22
IP_D:3	3	C22
IP_D:4	4	D22
IP_D:5	5	E22
IP_D:6	6	A21
IP_D:7	7	B21
IP_D:8	8	C21
IP_D:9	9	D21
IP_D:10	10	E21
IP_D:11	11	A20
IP_D:12	12	B20
IP_D:13	13	C20
IP_D:14	14	D20
IP_D:15	15	E20
IP_D:16	16	A19
IP_D:17	17	B19
IP_D:18	18	C19
IP_D:19	19	D19
IP_D:20	20	E19
IP_D:21	21	A18
IP_D:22	22	B18
IP_D:23	23	C18
IP_D:24	24	D18
IP_D:25	25	E18
IP_D:26	26	A17
IP_D:27	27	B17
IP_D:28	28	C17
IP_D:29	29	D17
IP_D:30	30	E17
IP_D:31	31	A16
IP_D:32	32	B16
IP_D:33	33	C16
IP_D:34	34	D16
IP_D:35	35	E16
IP_D:36	36	A15
IP_D:37	37	B15
IP_D:38	38	C15
IP_D:39	39	D15
IP_D:40	40	E15
IP_D:41	41	A14
IP_D:42	42	B14
IP_D:43	43	C14
IP_D:44	44	D14
IP_D:45	45	E14
IP_D:46	46	A13
IP_D:47	47	B13
IP_D:48	48	C13
IP_D:49	49	D13
IP_D:50	50	E13