ATC-SYNC

Dual channel Synchro/Resolver to Digital Industry Pack Module

REFERENCE MANUAL

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1. INTRODUCTION

The ATC-SYNC IP module of ALPHI TECHNOLOGY is a dual Resolver/Synchro to Digital Converter (RDC) compatible with the VITA –4 specification. This module work with two independently RDC. All RDC have three different input configurations (direct, differential, (resolver) or synchro). The tracking rate and bandwidth are user defined when ordered .

The ATC-SYNC module can generated interrupts from two different sources for each channel.

2. DESCRIPTION

2.1 SUMMARY OF FEATURES

- Single-size IP module (type I).
- Compatible with the ANSI/VITA-4 1995 specification.
- 2 Resolver/Synchro to digital converters for channel A and B
- Resolution at 10, 12, 14 and up to 16-bit.
- Tracking up to 1152 rps.
- For channel A and B you have 2 RDC :

Direct input for 2V resolver Differential

(resolver) input (predefined : 11.8V or 90V) Synchro input

(predefined :11.8V or 90V).

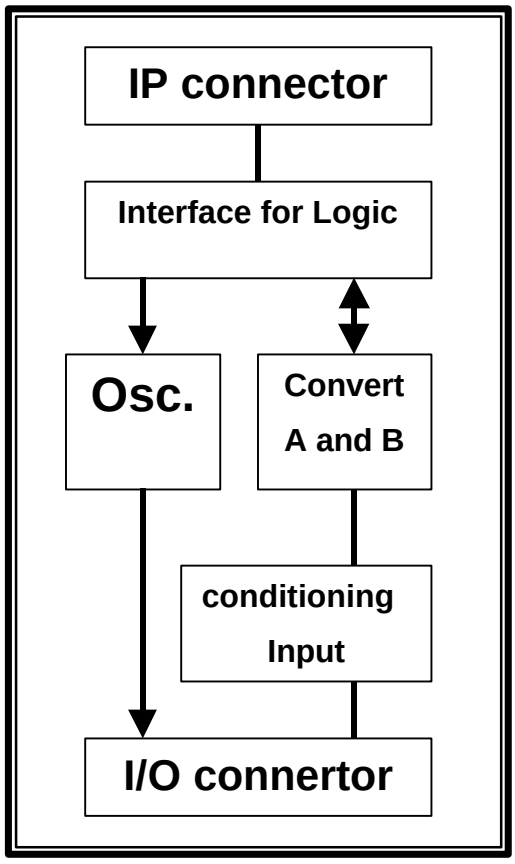
- Memorization for simultaneous reading of the two converters.
- Vectored interrupts for channel A and B:

Position matches

Converter error conditions

- On board synthesized reference.
- User-define excitation output voltage (2.2, 2.5, 4, 4.4 Vrms)
- Commercial and industrial temperature range available.

2.2 BLOCK DIAGRAM



ATC-SYNC Block diagram

3. ATC-SYNC CHARACTERISTICS

These RDC's specifications apply over the rated power supply, temperature and reference frequency ranges, and 10% signal amplitude variation and harmonic distortion.

3.1 CONVERTER CHARACTERISTICS

Parameters	Value			Unit
Resolution	10, 12, 14, 16			bits
Frequency Range	47-1k	1k-4k	4k-10k	Hz
Accuracy 4min	4+1 LSB	4+1 LSB	5+1 LSB	Min
2min	2+1 LSB	2+1 LSB	3+1 LSB	Min
Repeatability	±1	±1	±2	LSB
Differential Linearity	±1	±1	±2	LSB
Reference	(+REF, -REF)			
Type	Direct, Resolver or Differential			V
Voltage: differential	+/- 10 max			V
Single ended	+/- 5 max			V
Overload	+/- 25 continous			V
Frequency	DC to 10k			Hz
Inut impedance	10M min //20pF			Ohm

Signal Input	(S1, S2, S3, S4)				
Type	Direct, Resolver or Differential				V
Voltage operating	2 +/- 15%				V
Overload	+/- 25 continuous				V
Input Impedance	10M min //20pF				Ohm
Dynamic Characteristics	(At maximum bandwidth)				
Resolution	10	12	14	16	Bits
Tracking Rate-min	1152	288	72	18	Rps
Bandwidth (Closed Loop) max	1200	1200	600	600	Hz
Acceration (1 LSB lag)	2M	500K	30K	2K	Deg/s
Setting Time (179 step)	2	8	20	50	ms
Velocity Characteristics					
Polarity	Positive for increasing angle				
Voltage Range (Full Scale)	+/- 3.5 V (at normal ps)				V
Scale Factor Error	10 typ		20 max		%
Scale Factor TC	100 typ		200 max		ppm/c
Reversal Error	0.75 typ		1.3 max		%
Linearity	0.25 typ		0.50 max		%
Zero offset	5 typ		10 max		%
Zero offset TC	15 typ		30 max		%
Load			8 max		k
Noise	1 typ		0.125 min, 2 max		Vp/V

3.2. CHARACTERISTICS FOR IP MODULE

Parameters	Value		Unit
Supply current			
+5 V +/- 5%	TBD		mA
+12 V +/- 5%	TBD		mA
-12 V +/- 5%	TBD		mA
Temperature Range	**Commercial**	**Industrial**	
Operating	0 to 70	-40 to +85	C
Storage	-40 to +85		C

4. REGISTER SPACES

Space	Description	Access
ID	IP module identification	Read only
I/O	IP module I/O register	Read/Write
INT	IP module interrupt acknowledge	Read only

The base address depends of IP carrier board.

4.1 WAIT STATE CYCLES

Space	Wait state	
	Read	Write
ID space	1	-
I/O space		
CONTROL,VECTOR,ACOMP,BCOMP,STATUS2	1	1
RESET IP	-	1
CLRCOMPA,CLRCOMPB,CLRBIT_A,CLRBIT_B, CDRA,CDRB	1	-
Interrupt Acknowledge	1	-

Wait state cycles

4.2 ID REGISTER

These values are read only.

ID space add.	Description	Value
$01	Ascii “I”	$49
$03	Ascii “P”	$50
$05	Ascii “A”	$41
$07	Ascii “C”	$43
$09	Manufacturer identification	$11
$0B	Module type	$12
$0D	Revision type	$0A
$0F	Reserved	$00

Correct reading of the first four bytes that contain the ASCII text "IPAC" can be used to identifie the presence of an Industries Pack module.

Location $09 provide the Manufacturer identities (ALPHI TECHNOLOGY INDUSTRY PACKs $11).

The next two locations identify the module type and revision.

A 8-bit CHECKSUM (CRC) provide data integrity of the valid ID code set by the manufacturer.

The next bytes $ 19 to $ 3F are free for user data storage.

4.3 I/O REGISTER

The following register control and configure part of the ATC-SYNC IP module.

IO offset	Register	Register description	RD/WR	Wide
$00	CONTROL	General Control Register	RD/WR	16-bit
$02	INT_VECT	Interrupt vector value	RD/WR	16-bit
$0A	COMPA	Channel A position compare	RD/WR	16-bit
$0C	COMPB	Channel B position compare	RD/WR	16-bit
$0E	STATUS	Status register	Read	16-bit
$10	RESET IP	Reset IP module	Write	16-bit
$12	CLRCOMPA	Clear interrupt COMP_A	Read	16-bit
$14	CLRCOMPB	Clear interrupt COMP_B	Read	16-bit
$18	CLRBIT_A	Clear interrupt BIT_A	Read	16-bit
$1A	CLRBIT_B	Clear interrupt BIT_B	Read	16-bit
$1C	CDRA	Conversion data register channel A	Read	16-bit
$1E	CDRB	Conversion data register channel B	Read	16-bit

I/O register map

4.3.1 CONTROL REGISTER

This Read/Write register contains the configuration parameters and functions of the IP module:

- Function “Memorization” (MEM)
- the resolution for channel A & B (SLB1, SLB0, SLA1, SLA0)
- Interrupt enable and masks (IRQ_EN, BIT_EN, COMPA_MSK, COMPB_MSK)

Register	D15	D14	D13	D12	D11	D10	D9	D8
Control	-	-	-	-	MEM	-	SLB1	SLB0
	-	-	-	-	R/W	-	R/W	R/W

D7	D6	D5	D4	D3	D2	D1	D0
SLA1	SLA0	-	IRQ_EN	BIT_EN	COMPB-MSK	COMPA-MSK	-
R/W	R/W	-	R/W	R/W	R/W	R/W	-

After reset, $0000.

Bit	Name	Description
D15..D13	-	**Reserved**
D12	-	**Reserved**.
D11	MEM	**Memorization.** Stop reading automatically new values from both converters. It can be used to read both channel values “at the same time”. For clear this bit to start again acquisition again.
D10	-	**Reserved**
D9 D8	SLB1 SLB0	**Resolution selection for RDC A.**
D7 D6	SLA1 SLA0	**Resolution selection for RDC B.**
D5	-	**Reserved**
D4	IRQ_EN	**General interrupts enable.** Set to allow general interrupt (BIT and COMPARE). No interrupt will be generated until this bit is set.

D3	BIT_EN	**BIT interruption enable.** Enable BIT interrupt from channel A and B. Selection of bit mask can be made in STATUS register
D2 D1	COMPB-MSK COMPA-MSK	**Compare interrupt mask channel A and B.**
D0	-	**Reserved**

Control register description

Resolution	SLx1	SLx0
16 bits	1	1
14 bits	1	0
12 bits	0	1
10 bits	0	0

Resolution CH A & B.

4.3.2 INTERRUPT VECTOR REGISTER

This 16-bit Read/Write register contains the value of the vector that will be return during interrupt acknowledge cycle. D7 is the Most Significant Bit (MSB).

Register	D15..D8	D7	D6	D5	D4	D3	D2	D1	D0
INT_VECT	Reserved	Interrupt vector value							
	-	Read/Write							

After reset, $0000.

4.3.3 POSITION COMPARE REGISTER

There Read/Write registers contain the value to be compare with the converter value. This value is user defined. An interrupt can be generated on position match if enable in CONTROL register. Compared value is on 12-bit (D15..D4).

Register	D15..D4	D3..D0
COMPA	Position compare channel A	Reserved
	Read/Write	-

After reset, $0000.

Register	D15..D4	D3..D0
COMPB	Position compare channel B	Reserved
	Read/Write	-

After reset, $0000.

4.3.4 STATUS REGISTER

This Read/Write register can mask BIT interrupt sources and shows pending interrupt condition.

Register	D15..D14	D13	D12	D11..D4	D3	D2	D1	D0
Status	Reserved	BITMSK_B	BITMSK_A	Reserved	BIT_B	BIT_A	COMP_B	COMP_A
	-	RD/WR	RD/WR	-	RD	RD	RD	RD

After reset, &000X.

X depend of state of converters. If no signal is applied to converters, BIT flags will be set. If cleared, those flags will rise again until BIT condition is removed.

Bits	Name	Description
D15..D14	-	**Reserved**
D13 D12	BITMSK_B BITMSK_A	**Build-in-test interrupt mask, channel A & B** Will can mask BIT interrupt for selected converter. By defaut no interrupt source are masked. Set those bits to mask BIT signal from one converter.
D11..D4	-	**Reserved**
D3 D2	BIT_B BIT_A	**Build-in-test interrupt flag, channel A & B** Those bits are set when the converter (A or B) activates his BIT signal. Read CLRBITA or CLRBITB for clearing the corresponding flag.
D1 D0	COMP_B COMP_A	**Position compare interrupt flag ,channel A &B** This bit is set when the position compare register mach the current position of the converter A or B. Read CLRCOMPA or CLRCOMPB for clearing the corresponding flag.

STATUS register description

4.3.5 RESET IP MODULE

Write at this address for make a software reset on the IP module.

For used Interrupts you need to generated a software reset to clear All flag.

4.3.6 CLEAR COMPARE INTERRUPT REGISTER

The two read only registers can be use for clearing the compare interrupt flag in STATUS.

Register	D15..D0
CLRCOMPA	Clear COMP_A
	Read only

After reset, &0000.

Register	D15..D0
CLRCOMPB	Clear COMP_B
	Read only

After reset, &0000.

4.3.7 CLEAR BIT INTERRUPT REGISTER

The read only registers can be use for clearing the compare interrupt flag in STATUS.

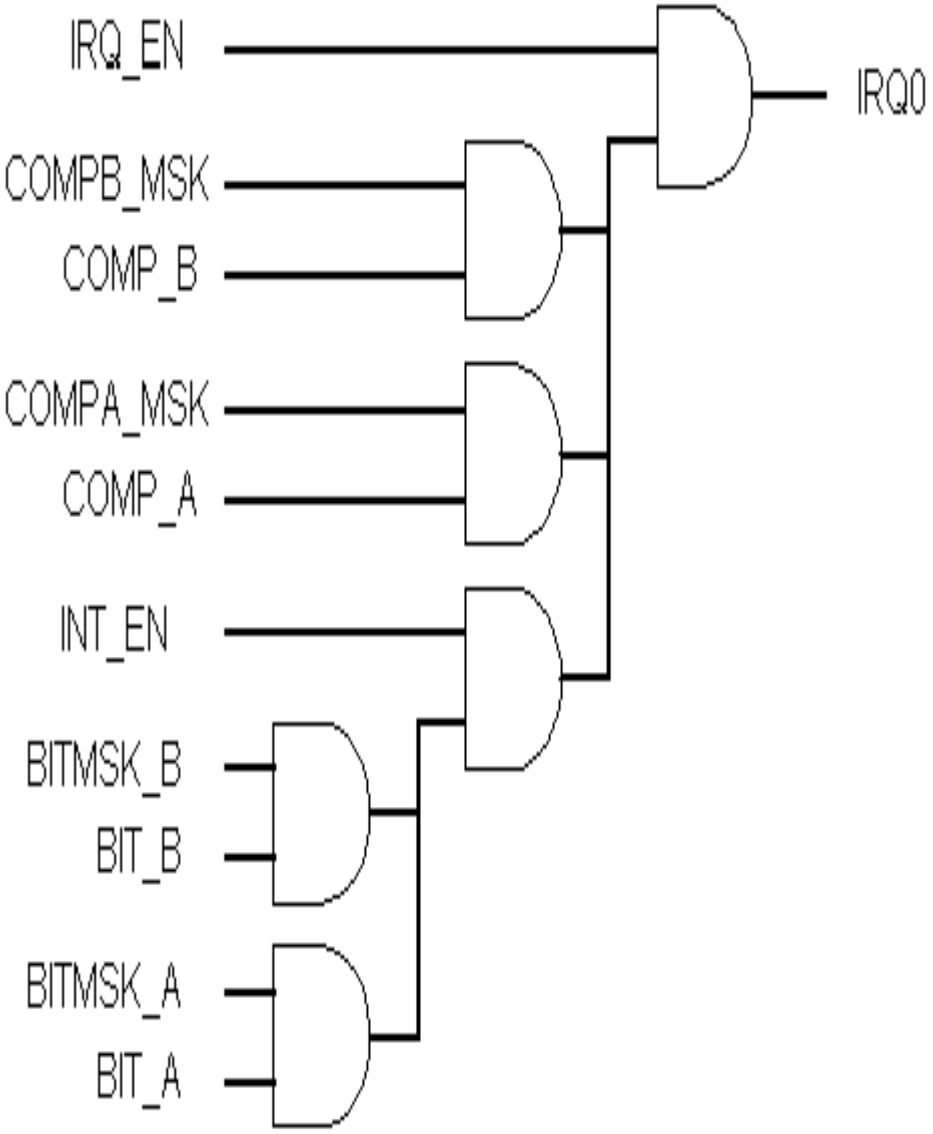
Register	D15..D0
CLRBITA	Clear BIT_A flag
	Read only

After reset, &0000.

Register	D15..D0
CLRBITB	Clear BIT_B flag
	Read only

After reset, &0000.

4.3.8 INTERRUPTS DIAGRAMM



Interrupt source diagram.

DATA REGISTER

The read only registers contain the conversion results. The Less Significant Bit (LSB) depends on the resolution (see table below). The value are automatically updated when converters change. This automatically updated value can be frizzed with MEM bit in CONTROL register.

Register	D15..D0
CDRA	Converter value, channel A
	Read only

After reset, &0000.

Register	D15..D0
CDRB	Converter value, channel B
	Read only

After reset, &0000.

Position of LSB

Depending of converter resolution. It have 2 independent channels. After reset is set to 10-bit for both converters.

Resolution	D15	D14..D6	D6	D5	D4	D3	D2	D1	D0
10 bits	MSB	X	LSB	-	-	-	-	-	-
12 bits	MSB	X	X	X	LSB	-	-	-	-
14 bits	MSB	X	X	X	X	X	LSB	-	-
16 bits	MSB	X	X	X	X	X	X	X	LSB

LSB position function of the resolution

Conversion formula

In degree :

Angle = 360 . (x / 65536)

x : value read from converter in decimal.

In radian :

Angle = 6.28 . (x / 65536)

x : value read from converter in decimal.

5. SYNCHRO TO DIGITAL CONVERTER

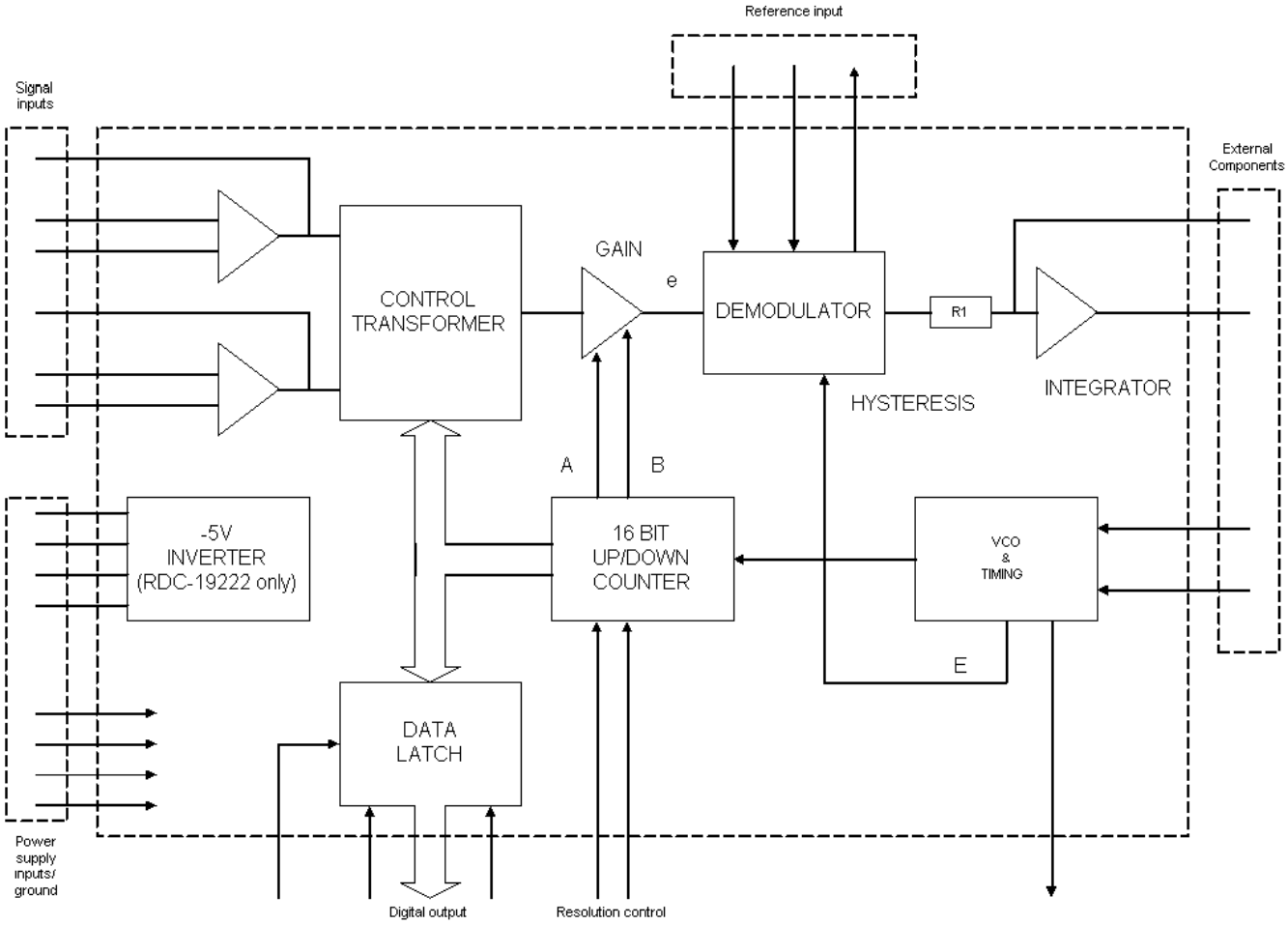
The ATC-SYNC IP module used two RDC-19222S devices (one per channel).

5.1 DESCRIPTION

The RDC-19222S is a 16 bits monolithic state-of-art Resolver-to-Digital Converter with programming Resolution (10, 12, 14 16 bits).

This chip combines the high-tracking rate (10 bits) with the precision (16 bits).

The converter bandwidth, dynamics and velocity are externally set with passive components.



5.2 GENERAL SET-UP CONSIDERATION

Six external components define the set up converter and carrier frequency, bandwidth, tracking rate and resolution define the components values.

Resolution	16 bits	14 bits	12 bits	10 bits	Unit
Max Tracking Rate	18	72	288	1152	Rps
Max Carrier Frequency	5	5	10	10	KHz
Max Bandwidth	300	600	1200	1200	Hz
Acceleration (1lsb lag)	2k	30k	500k	2M	Deg/s''
Setting Time (179° step)	2	8	20	50	ms

5.3 BUILT IN TEST (BIT SIGNAL)

The built-in test is an output flag that can be used to indicate a fault condition. This signal is allowed in CONTROL register and BIT can generate an interrupt.

6. INPUT CONFIG

Three input modes are available on the ATC-SYNC.

- Direct input (2 V resolver)
- Differential resolver input (11.8 V or 90 V)
- Synchro input (11.8 V or 90 V)

6.1 INPUT RESISTOR CONFIGURATION

Resistor(49590) on	Description
DP3 and DP5 socket	Synchro input
DP4 and DP6 socket	Differential resolver input

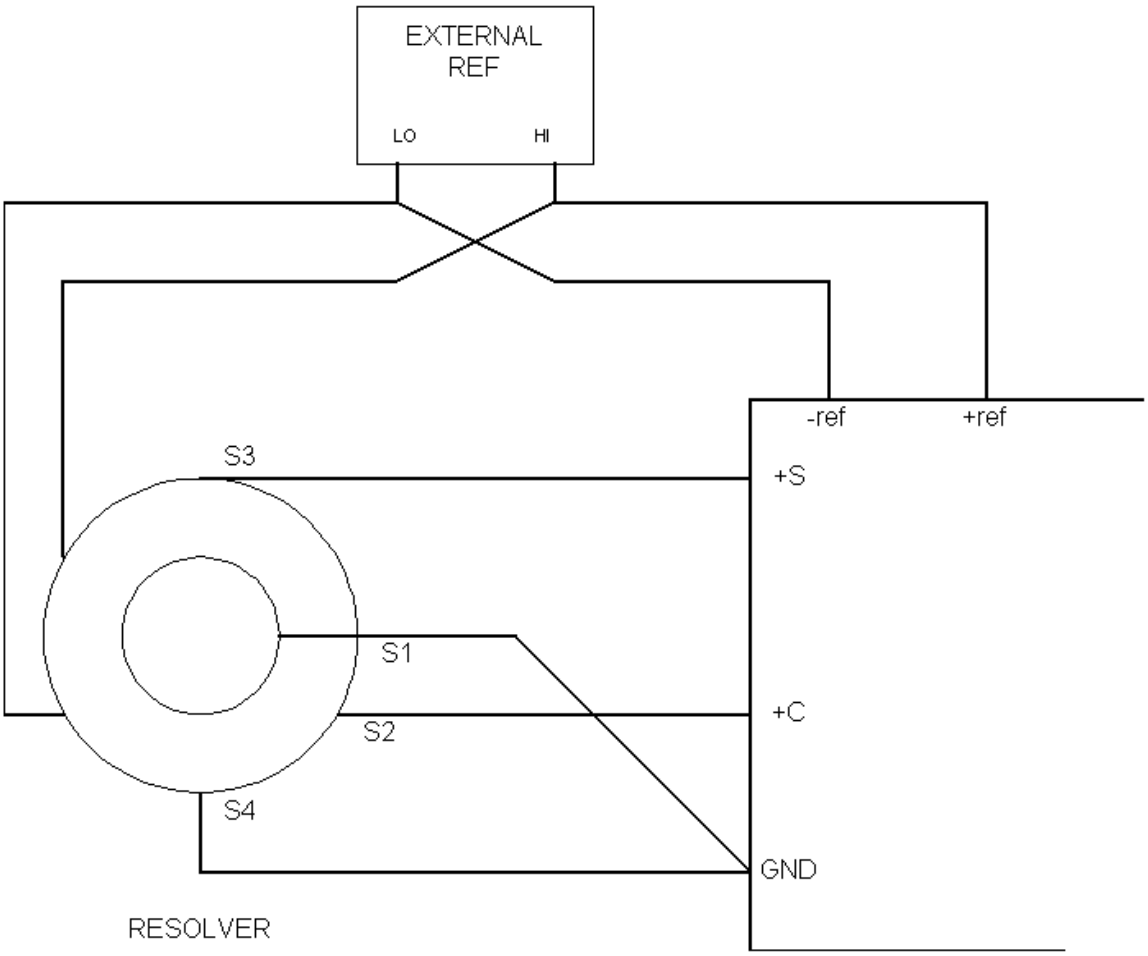
6.2 JUMPER CONFIGURATION

Jumper J2 and J3	Description
All jumper ON	Direct input (2 V Resolver)
All jumper OFF	Resistor Network (resolver or synchro)

6.3 DIRECT INPUT (2 V RESOLVER)

Configuration:

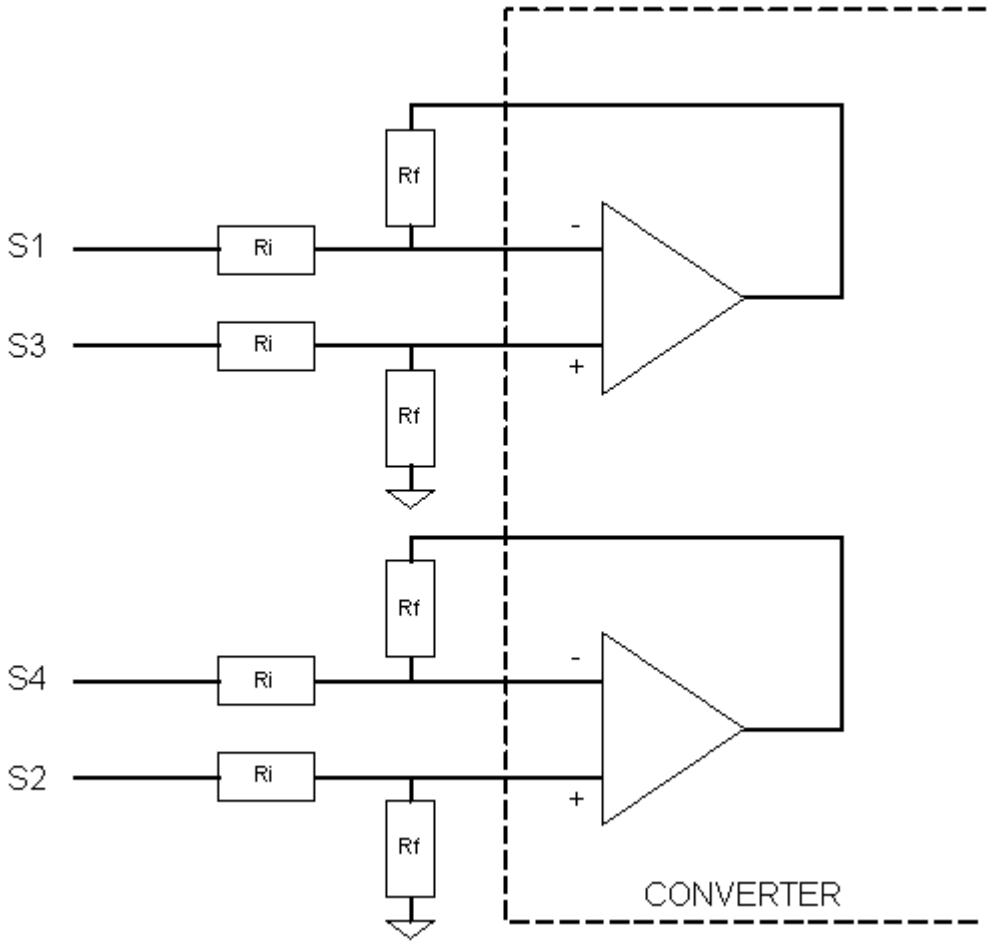
- All jumpers are ON.
- No resistor on DP3, DP4, DP5 and PD6.



6.4 DIFFERENTIAL (RESOLVER) INPUT

Configuration:

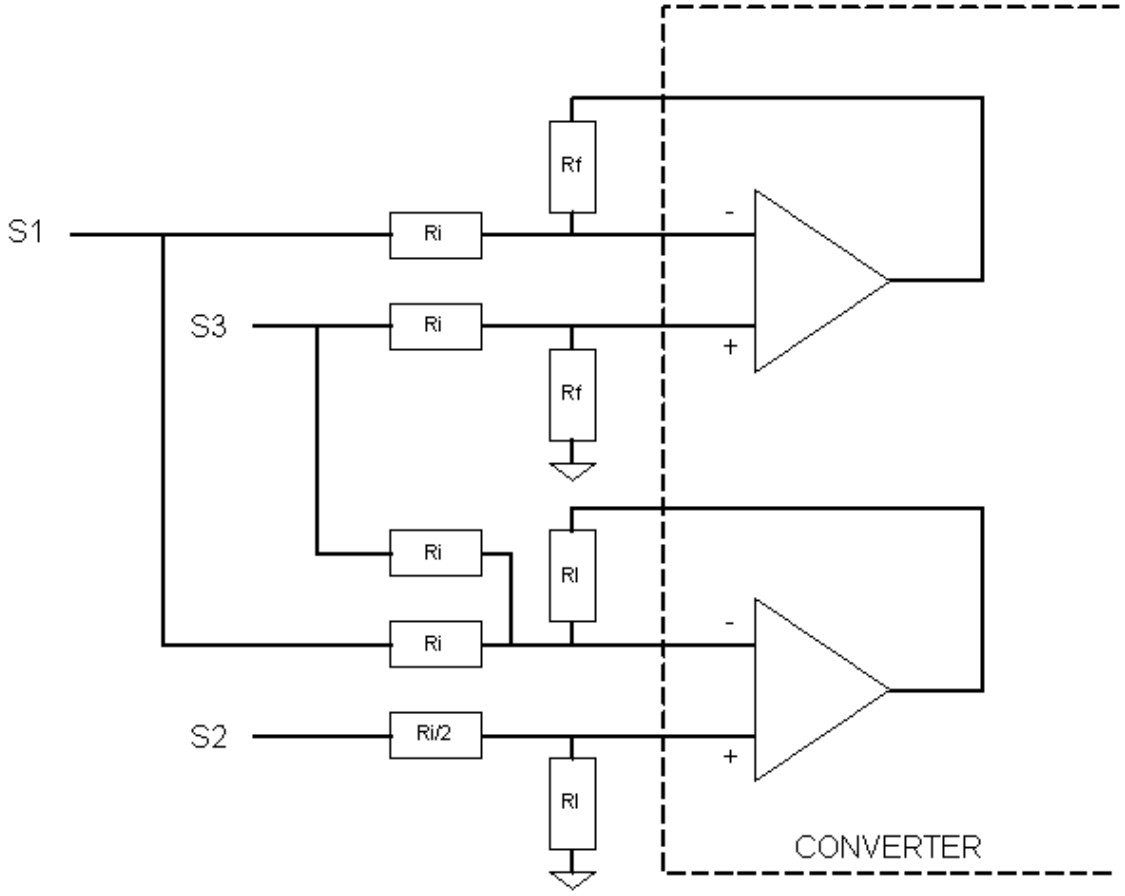
- All jumpers are OFF.
- Need resistor on DP4 and PD6.



6.5 SYNCHRO INPUT

Configuration:

- All jumpers are OFF.
- Need resistor on DP3 and PD5.



7. CONNECTOR

PIN	NAME	Description
1	+REFA	Input reference channel A
2	-REFA	Input reference channel A
4	SA1	Input S1 channel A
5	SA3	Input S3 channel A
7	SA2	Input S2 channel A
8	SA4	Input S4 channel A
3,6,9,12,15,18	AGND	Analog Ground
10	+REFB	Input reference channel B
11	-REFB	Input reference channel B
13	SB1	Input S1 channel B
14	SB3	Input S3 channel B
16	SB2	Input S2 channel B
17	SB4	Input S4 channel B
21	VEL_A	Output velocity signal channel A
23	VEL_B	Output velocity signal channel B
25	BITA*	Output signal BITA
33	BITB*	Output signal BITB
35	+12V	+12V Power
40	-12V	-12V Power
37,39,41,43	+5V	+5V Power
45,46,48,49	+5V	+5V Power
20,22,24,26	GND	Digital Ground
32,34,36,42	GND	Digital Ground
44,47,50	GND	Digital Ground
27,38	NC	No Connected
28,29,30	RES2..RES0	Reserved