ALPHI Technology

ATC-1553-DDC

MIL-STD-1553 BC/ RT/ BM Industry Pack Module

REFERENCE MANUAL

801-10-000-4000

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ALPHI TECHNOLOGY CORPORATION
6202 S. Maple Avenue #120
Tempe, AZ 85283 USA
Tel : (480) 838-2428
Fax: (480) 838-4477

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GENERAL DESCRIPTION

INTRODUCTION

The ATC-1553-DDC module provides Bus Controller (BC), Remote Terminal (RT) and Bus Monitor (BM) dual-redundant operations on the MIL-STD-1553 bus. The IP form factor provides easy installation.

- DDC BU-61865G4 1553 processor unit
- 64 k-word of dual-ported on-board RAM.
- 5 V only supply.
- Supports MIL-STD-1553A, MIL-STD-1553B Notice 2, STANAG 3838, and
- McAir A3818, A5232 and A5690 protocols.
- Single wide Industry Pack form factor, VITA 4 compliant
- Transformers on-board.
- Supports Bus Controller, Remote Terminal and Bus Monitor mode
- RT address and operational modes are programmable or jumper selectable
- 1553 bus long or short stub, jumper selectable option

FUNCTIONAL DESCRIPTION

A functional block diagram of the IP module is depicted below in Figure 1. The ATC-1553-DDC is designed around the DDC BU-61865 that is used to manage the 1553 BUS protocol.

The ATC-1553-DDC IP module is built around the EN-MiniACE BU-61865G4 controller from DDC. This module can be a Bus Controller (BC), Remote Terminal (RT) or in Bus Monitor (BM).
The EN-MiniACE RT mode is multi-protocol, supporting MIL-STD-1553A, MIL-STD-1553B Notice2, STANAG 3838, and the McAir 13838, A5232 and A5690 protocols.

The transceiver is integrated in the EN-MiniACE.

Block Diagram

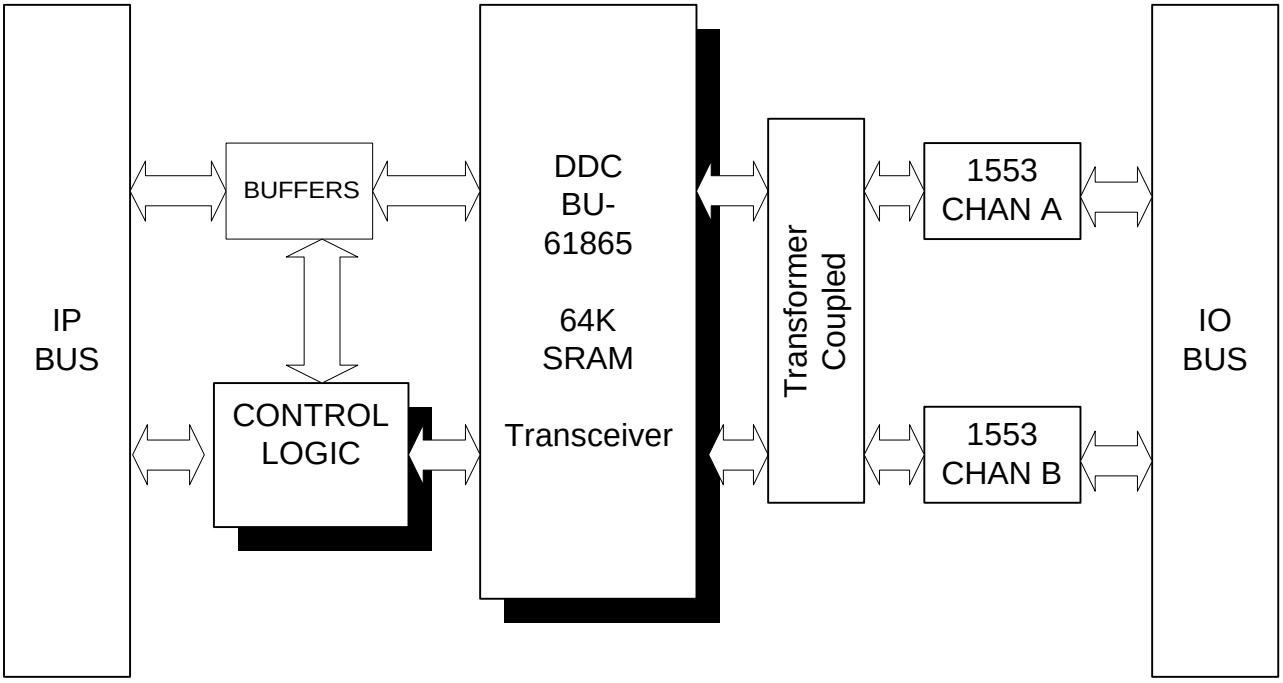


Figure 1

REFERENCE MATERIALS LIST

DDC Corporation:

105 Wilbur Place
Bohemia, NY 11716
(631) 567-5600
(800) DDC-5757

WWW Home Page:
http://www.ddc-web.com

Users manual and data sheet are on line, go to ddc-web.com
Part number DDC BU-61865G4

The reader is also referred to the IP Modules Draft Standard:

VITA standards Organization
10229 North Scottsdale Road, Suite B
Scottsdale AZ 85253
Voice : 480-951-8866
Fax : 480-951-0720

DDC REGISTERS I/O Address Space

Address	Registers	Read/Write
$00	Interrupt Mask Register	Read/Write
$02	Configuration Register #1	Read/Write
$04	Configuration Register #2	Read/Write
$06	Start / Reset Register	Write
$06	BC/RT Command Stack Pointer register	Read
$08	BC Control Word/ RT Sub-address Control Word Register	Read/Write
$0A	Time Tag Register	Read/Write
$0C	Interrupt status Register #1	Read
$0E	Configuration Register #3	Read/Write
$10	Configuration Register #4	Read/Write
$12	Configuration Register #5	Read/Write
$14	RT Data Stack Address Register	Read/Write
$16	BC Frame Time Remaining Register	Read
$18	BC Time Remaining to Next Message Register	Read
$1A	Non Enhanced BC Frame Time Reg. RT Last Command Reg. MT Trigger Word Register	Read/Write
$1C	RT Status Word Register	Read
$1E	RT Bit Word Register	Read
$20	Test Mode Register 0	
$22	Test Mode Register 1	
$24	Test Mode Register 2	
$26	Test Mode Register 3	
$28	Test Mode Register 4	
$2A	Test Mode Register 5	
$2C	Test Mode Register 6	
$2E	Test Mode Register 7	
$30	Configuration Register #6	
$32	Configuration Register #7	
$34	RESERVED	
$36	BC General Purpose Flag / Condition Code Register	Read/Write
$38	Bit Test Register	Read
$3A	Interrupt Mask Register #2	Read/Write
$3C	Interrupt Status Register #2	Read
$3E	BC General Purpose Queue Ptr/ RTMT Interrupt Status queue	Read/Write

Local REGISTERS I/O Address Space

Address	Registers	Read/Write
$40	Interrupt Vector Register	Read/Write
$42	Status Register	Read/Write

MEMORY SRAM SHARED

The ATC-1553-DDC has a 64K x 16-bit Shared Memory. The base address of the SRAM is located in the IP Memory Space of the Host. Only 16-bit accesses are allowed. Arbitration between the EN-MiniACE and the IP Bus is made by the local hardware. EN-MiniACE access to the SRAM takes priority over any pending host access. Therefore, the host access will be held off until the EN-MiniACE access completes.

ID SPACE

The ATC-1553-DDC conforms to the IP Bus Specification and has a 32 byte EEPROM that can be read to identify the IP module Manufacturer, type, revision, etc. The base address of the EEPROM is in the IP ID Space of the Host. The EEPROM is built in the FPGA on board for protection. The ID can not be overwritten.
The Manufacturer ID identifies ALPHI as the manufacturer of the ATC-1553-DDC module. When the ID space is accessed in 16 Bit, the Low bytes have the valid Data.

ID space address	Description	Value
$00	ASCII “I”	$XX49
$02	ASCII “P”	$XX50
$04	ASCII “A”	$XX41
$06	ASCII “C”	$XX43
$08	Manufacturer identification	$XX11
$0A	Module type	$XX15
$0C	Revision module	$XX0A
$0E	Reserved	$XX00
$10	Driver ID,low byte	$XX00
$12	Driver ID,high byte	$XX00
$14	Number of bytes used	$XX0A
$16	CRC	$XX00
$18-$3E	User space	$XX00

Table 1 ATC-1553-DDC ID

IP INTERFACE:

IP MEM SPACE

NAME	OFFSET	DATA	R/W	COMMENTS
MEM SPACE	$0 - $1FFFF	D00-D15	R/W	Shared / Static RAM 64K x 16-bit (128Kbytes)

IP I/O SPACE

NAME	OFFSET	DATA	R/W	COMMENTS
DDC REGISTERS	$00-$3F	D00-D15	R/W	DDC Registers
INTERRUPT VECTOR	$40-$41	D00-D07	R/W	Interrupt Vector Registers
IP STATUS	$42-$43	D00-D07	R	Status Register

IP ID SPACE

NAME	OFFSET	DATA	R/W	COMMENTS
ID EEPROM	$00-$7F	D00-D07	R/W	IP EEPROM Identification

STATUS REGISTER

The IP STATUS register is used to determine the status of ATC-1553-DDC jumper settings. The Status Register provides the following status bits:

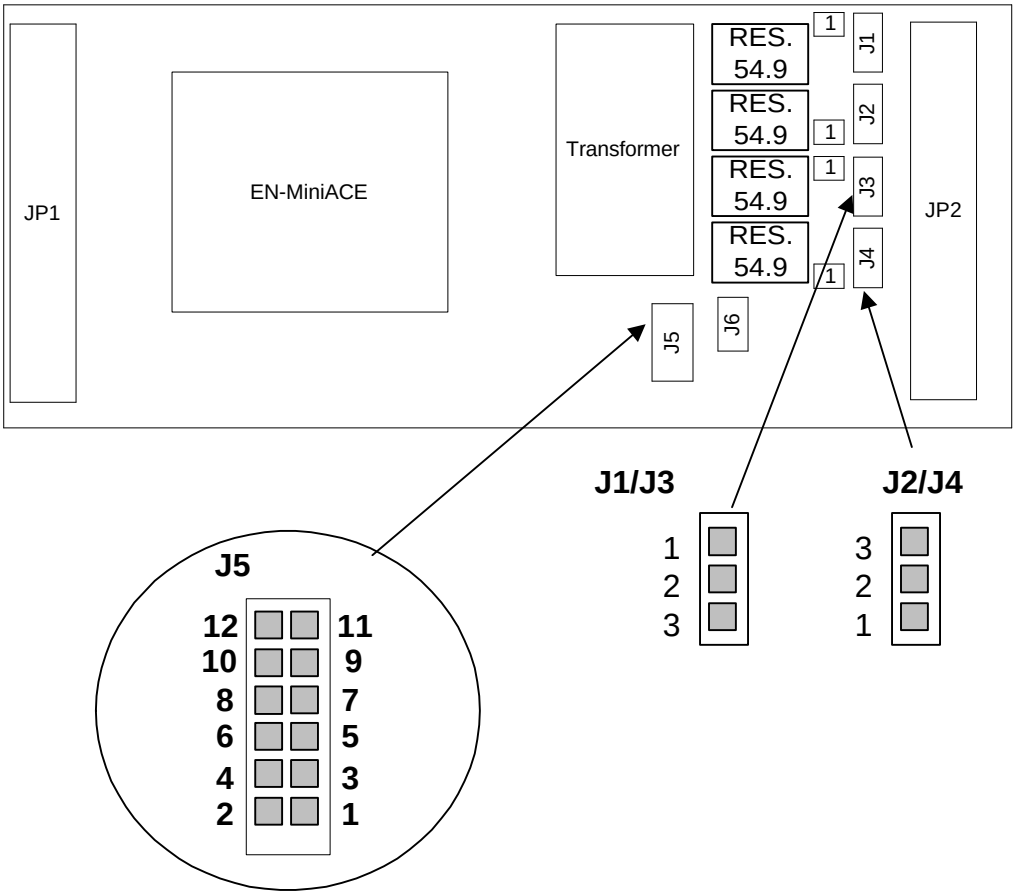
Bit	Name	Function
0	RTA0	RT ADDRESS 0
1	RTA1	RT ADDRESS 1
2	RTA2	RT ADDRESS 2
3	RTA3	RT ADDRESS 3
4	RTA4	RT ADDRESS 4
5	RTPT	RT PARITY
6	INT_A	ACE INTERRUPT

Table 2 Status register

LOCAL INTERRUPT SOURCES

The EN-MiniACE has one (1) interrupt line INT.
A local IVR (interrupt Vector Register) is available.
Upon an active interrupt, (INTREQ0 is Low) a read access to the INT select space, will provide a vector (Byte) on Lower byte LD[7..0] .
The IVR can be R/W in Word at: IOspace address + $40

JUMPER LOCATION DIAGRAM



JUMPER SETUP AND DESCRIPTION:

JUMPER	FACTORY SETTING	DESCRIPTION
J1	1-2	Short Stub Output channel B +
J2	2-3	Short Stub Output channel B -
J3	1-2	Short Stub Output channel A +
J4	2-3	Short Stub Output channel A -
J5	none	Remote terminal address RTA4-RTA0, RTPT
J6	1-2	External Trigger
JP1		IP Bus Interface
JP2	Factory	In Circuit PGM for FPGA
JP3		I/O Bus Interface

Table 3

J5 RT Address Selection

Signal	Jumper set	Description
RTA0	11-12 ON OFF	 RT Address BIT 0 set to Logic “0” RT Address BIT 0 set to Logic “1”
RTA1	9-10 ON OFF	 RT Address BIT 1 set to Logic “0” RT Address BIT 1 set to Logic “1”
RTA2	7-8 ON OFF	 RT Address BIT 2 set to Logic “0” RT Address BIT 2 set to Logic “1”
RTA3	5-6 ON OFF	 RT Address BIT 3 set to Logic “0” RT Address BIT 3 set to Logic “1”
RTA4	3-4 ON OFF	 RT Address BIT 4 set to Logic “0” RT Address BIT 4 set to Logic “1”
RTPT	1-2 ON OFF	 RT Parity set to Logic “0” RT Parity set to Logic “1”

Table 4

INTERFACE TO A MIL-STD-1553:

The 1553 bus can be interfaced either in Transformer (LONG STUB) or DIRECT (SHORT STUB). Jumper selectable.
In the LONG STUB Coupled, the length between the buses can be between 1-20Feet.
In the SHORT STUB Coupled, the length should not exceed 1 Foot.
For further explanation and description on the Coupling method, refer to DDC web page, to the document labeled as: 1553 design Guide.

J3 & J4 1553 Output Channel A Configuration

Signal	Jumper set J3	Jumper set J4	Description
CH A	1-2 ON 2-3 ON	2-3 ON 1-2 ON	Short Stub Output channel A Long Stub Output channel A

Table 13

J1& J2 1553 Output Channel B Configuration

Signal	Jumper set J1	Jumper set J2	Description
CH B	1-2 ON 2-3 ON	2-3 ON 1-2 ON	Short Stub Output channel B Long Stub Output channel B

Table 12

DDC I/O CONNECTIONS

I/O PIN	SIGNAL DESCRIPTION
1	LED_A+ (Anode Pin)
2	INCMD*
3	LED_B+ (Anode Pin)
4	DGRT*
5	SSFLG_IN
6	GND
7	
8	GND
9	
10	
11	
12	
13	
14	
15	
16	
17	
18	
19	
20	
21	
22	
23	
24	
25	

I/O PIN	SIGNAL DESCRIPTION
26	GND_CHA
27	OUT_CH A+
28	
29	OUT_CH A-
30	
31	
32	
33	
34	
35	
36	
37	
38	
39	
40	
41	
42	
43	
44	
45	
46	
47	OUT_CH B+
48	
49	OUT_CH B-
50	GND_CHB

I/O Pin Description:

1- PIN (1) LEDA+ AND PIN (2) INCMD* for an external LED use. That pin is controlled by bit 0 in of configuration register # 7. That pin is asserted low whenever a message is being processed by the En-MiniAce. This pin is used only if external indicator is required.

2- PIN (3) LEDB+ and PIN (4) DGRT* for an external LED use. That pin is asserted low in response to a DTREQ output: to indicate that control of the external processor/RAM bus has been transferred from the host processor to the En-MiniAce. This pin is used only if external indicator is required.

3- Pin (5) SSFLG_IN: Subsystem Flag (RT) or External Trigger.

See En-MiniAce programming manual for further details and use.

4- Pin 26 (GND Ch A), 27 (OUT_Ch A+) and 29 (OUT_Ch A-) are the designated pin for Ch A of the EN-MiniACE
5- Pin 50 (GND Ch B), 49 (OUT_Ch B-) and 47 (OUT_Ch B+) are the designated pin for Ch B of the EN-MiniACE