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ALPHI TECHNOLOGY CORPORATION

MPCI-1553-DDC

MIL-STD-1553
Mini-PCI Type III B Module

REFERENCE MANUAL

Revision 1.0
February 2009

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1. GENERAL DESCRIPTION

1.1. INTRODUCTION

The MPCI-1553-DDC module provides Bus Controller (BC), Remote Terminal (RT) and Bus Monitor (BM) dual-redundant operations on the MIL-STD-1553 bus. The MPCI form factor provides easy installation.

The ***MPCI-1553-DDC*** is installed with the following resources:

- DDC µACE RISC based processor unit
- 64K x 16 bit dual ported SRAM
- Supports Bus Controller, Remote Terminal and Bus Monitor mode
- RT address and operational modes are program or jumper selectable
- 1553 bus long or short stub jumper option

1.2. FUNCTIONAL DESCRIPTION

A functional block diagram of the MPCI module is depicted below in Figure 1. The MPCI-1553-DDC is designed around the µACE that is used to manage the 1553 BUS.

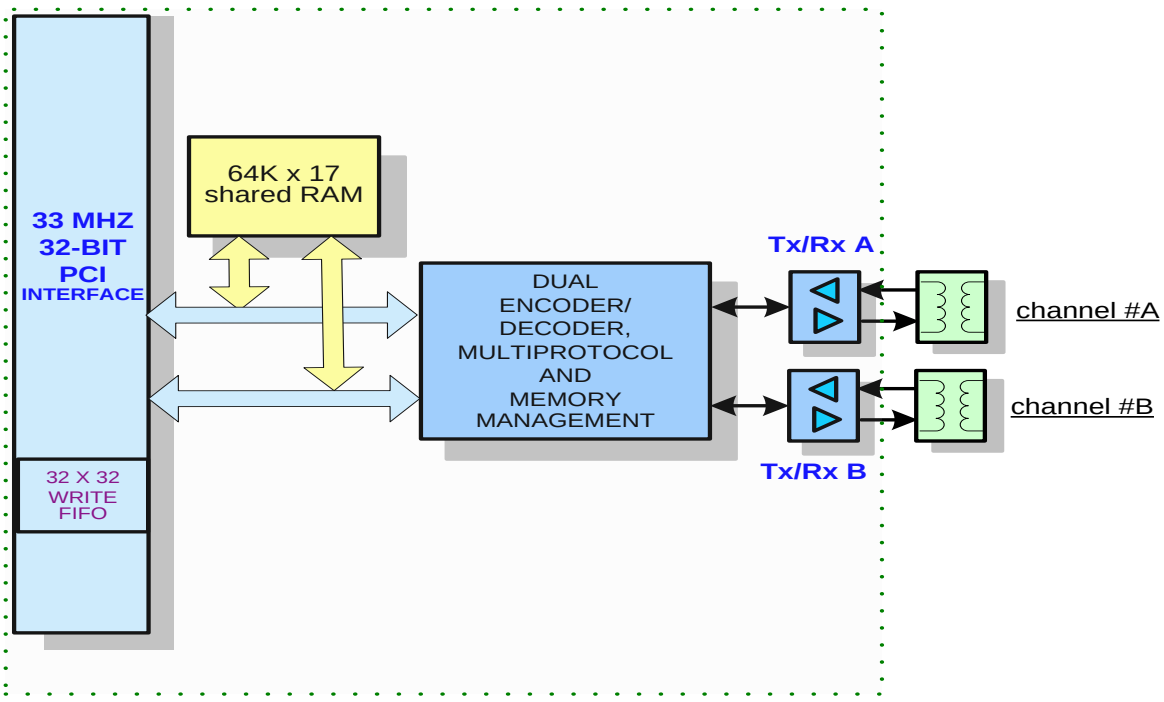

Figure 1.1: **MPCI-1553 Block Diagram**

1.3. REFERENCE MATERIALS LIST

The reader should refer to the “µACE USER’S GUIDE”, from DDC, that provides detailed descriptions about the ACE registers.

DDC
105 Wilbur Place
Bohemia, New York 11716-2482

Technical Information:
1-800-DDC-5757 ext. 7257 or 7381
Literature Requests:

WWW Home Page:
http://www.ddc-web.com

The reader should refer to the PCI Local Bus Specification for a detailed explanation of the PCI bus architecture and timing requirements. This specification is available from the following source:

PCI Special Interest Group
PO Box 14070
Portland, OR 97214
Tel: (800) 433-5177
Tel: (503) 797-4207
Fax: (503) 234-6762

2. HOST (Mini-PCI) SIDE

2.1. Interface to HOST (Mini-PCI)

All Mini-PCI devices contain a set of registers in Configuration Space which allow for determining the manufacturer and model of the device, determining the resources necessary for the correct operation of the device, and other configuration information. Configuration space is decoded on a per slot / device basis via a mechanism described in the Mini-PCI specification.

All Mini-PCI devices can be relocated in physical memory by means of several Base Address Registers. These registers contain the high address bits, which must be matched for any access to the card to be successful. Part of the protocol of programming the Base Address Registers allows for the transfer of information regarding the size of the regions.

The actual Base Address Registers are located in Configuration Space. Normally, configuring the card is performed by the system controller and some form of firmware or BIOS. Unfortunately, determining Base Addresses and other configuration information in Configuration Space is operating system dependent. One of the primary functions of the device driver under Windows NT is to map these resources to the user application.

The card is actually accessed through the decoded base address registers.

2.2. Mini-PCI Configuration Space

PCI Address: *CONFIG:0x00 – 0x3C*
Mode of Access: *Read/Write*
Reset By *Mini-PCI Hardware Reset*

The card has the following registers available to Mini-PCI Configuration Space. They are implemented in the DDC chip.

Offset Into PCI CFG	31 – 24	23 – 16	15 – 8	7 – 0
0x00	Device ID		Vendor ID	
0x04	Status		Command	
0x08	Class Code			Revision ID
0x0C	BIST	Header Type	PCI Latency Timer	Cache Line Size
0x10	PCI Base Address 0 (Memory Access to PLX Registers)			
0x14	PCI Base Address 1 (I/O Access to PLX Registers)			
0x18	PCI Base Address 2 (Memory Access to DSP SRAM and card registers)			
0x1C	PCI Base Address 3 (Not Used for this card)			
0x20	Unused PCI Base Address 4			
0x24	Unused PCI Base Address 5			
0x28	Cardbus CIS Pointer (Not Supported)			
0x2C	Subsystem ID		Subsystem Vendor ID	
0x30	PCI Base Address for Expansion ROM			
0x34	Reserved			
0x38	Reserved			
0x3C	Max Latency	Min Grant	Interrupt Pin	Interrupt Line

Table 2.1: Mini-PCI Configuration Space

The card presents the following initial configuration values to the Mini-PCI system, based on the values stored in the device.

Register	Value (Meaning)
Vendor ID	0x4DDC (DDC)
Device ID	0x0402 (MPCI-1553-DDC)
Revision ID	0x00
Class Code	0xff0000 (Device does not fit into defined class codes)
Interrupt Line	0xff
Interrupt Pin	A
Multifunction Device	No
Build In Self Test	No
Latency Timer	0x00
Minimum Grant	0x00
Maximum Latency	0x00
Base Address 0 Size	64Kwords Allocated
Base Address 1 Size	0x4k Bytes Allocated
Base Address 2 Size	No used
Base Address 3 Size	No used
Expansion ROM Size	None

Table 2.2: Mini-PCI-1553 Default Configuration

2.3. Mini-PCI Base Address Regions

HOST Address	WIDTH USED	Description	TYPE
BAR0	64KWords	DUAL PORTED SRAM	MEM
BAR1	64K BYTES	EN-MINI-ACE IO Space	I/O
BAR2	No used		
BAR3	No used		
BAR4	No used		
BAR5	No used		

Table 2.3: Mini-PCI-1553 Base Address Regions

3. JUMPERS AND CONNECTORS LOCATION

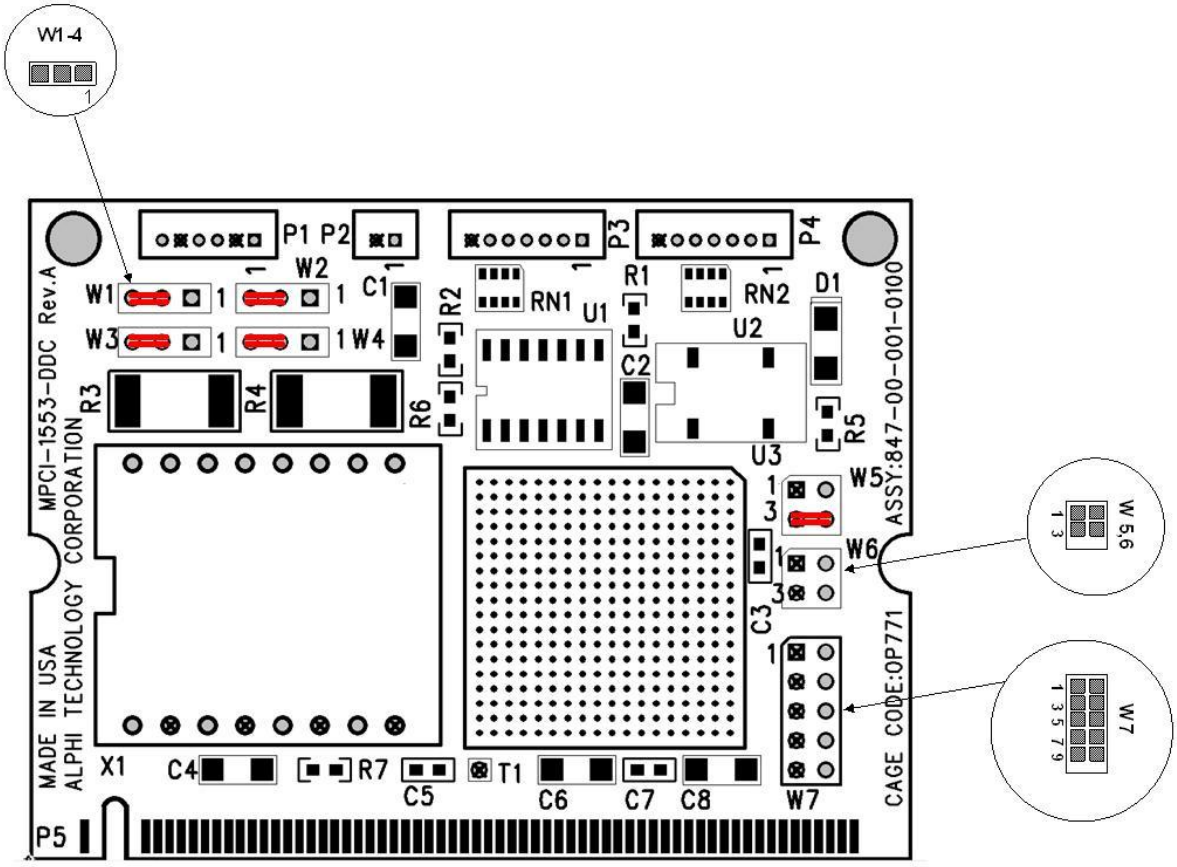

Figure 2.1: **JUMPERS LOCATION**

3.1. Jumpers Description

Signal	Jumper set	Description
Out Ch A / B	W1 - W4 1-2 2-3	1553 Stub Selection: Short Stub less then 1 feet Long Stub from 1 – 20ft
RT_Boot	W5 1-2	RT to automatically initialize as an active remote terminal with the Busy status word bit set to logic "1" immediately following power turn-on
TX Inhibit	W5 3-4	To inhibit 1553 Transmission
RTPT	W6 3-4	RT Address Parity
RT_AD_LAT	W6 1-2	RT address Latch
RTA4	W7 1-2	RT Address Bit 4
RTA3	W7 3-4	RT Address Bit 3
RTA2	W7 5-6	RT Address Bit 2
RTA1	W7 7-8	RT Address Bit 1
RTA0	W7 9-10	RT Address Bit 0

Table 3.1: Mini-PCI-1553 Jumper Description

3.2. Jumpers Default Setup

JUMPER	FACTORY SETTING	DESCRIPTION
W1	2-3	Long Stub/Short Stub Output channel 1A – (Long Stub)
W3	2-3	Long Stub/Short Stub Output channel 1A + (Long Stub)
W2	2-3	Long Stub/Short Stub Output channel 1B - (Long Stub)
W4	2-3	Long Stub/Short Stub Output channel 1B + (Long Stub)
W5	3-4	TX Inhibit - Disable
W6	None	Remote terminal parity (Software Programmable)
W7	None	Remote terminal address (Software Programmable)

Table 3.2: Mini-PCI-1553 Jumper Default

3.3. Connectors Description

Connector	FACTORY SETTING	DESCRIPTION
P1		1553 Connection
P2	None	External Tag Clock
P3	None	External Clock, Trigger and Control – Used for RT latching
P4	None	Remote terminal address – Used for RT latching

Table 3.3: I/O Connector Description

3.4. 1553 Connection

P1	Signal
1	Ch B +
2	GND Ch B
3	Ch B -
4	Ch A +
5	GND Ch A
6	Ch A -

Table 3.4: 1553 Connection

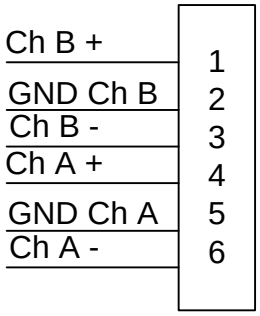

***Figure 2.2:* 1553 Pinout**

Connectors are manufactured by Molex and the style is PicoBlade.

Use	Model
On PC Board	53048-0610
Suggested Plug	51021-0600
Suggested Contact	50125-8100

Table 3.5: I/O Connector Model Numbers

