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ALPHI TECHNOLOGY CORPORATION

IP-DIO-48

48 CHANNEL INPUT/OUTPUT
Industry Pack Module
REFERENCE MANUAL

Revision 1.0
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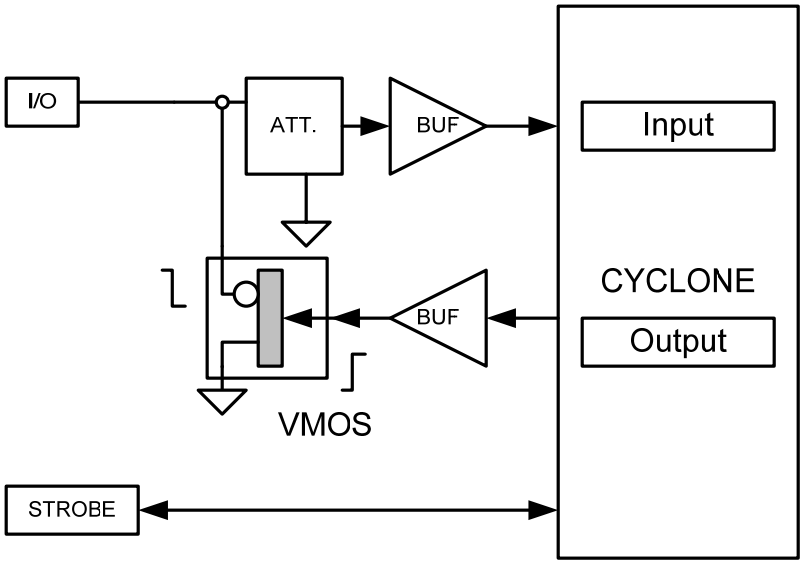
1 INTRODUCTION

1.1 Functional description

The IP_DIO48 module has 48 INPUT/OUTPUT channels that can be programmed as Input or Output independently.

Key Features are:

- Up to 48 I/O Pins available
- Output with two-stage latches allowing synchronous output change possibilities with multiples modules
- Output toggling possible at different clock frequencies
- Direct read-back outputs
- Open drain VMOS that can sink up to 100mA at voltages up to 40V.
- Very low R_{on} (0.3Ω) for low heat dissipation
- Wide input range from 0V to 30V with threshold adapted to a TTL input logic.
- Programmable debouncer clock for each channel
- Multiple interruption sources
  - Change of state
  - Edge
- Bi-directional IPstrobe for multiple module synchronization
- Self-test of any channel independently of the other channels
- 8 or 32 MHz IPCLK



2 MAP ADDRESS

The IP_DIO48 module uses only the IDspace and IOspace.

2.1 IDSPACE

Up to 48 bytes of registered data provide information about the module to the user. The lower address contains data related to the type of module, revision, etc...
Only even address data are valid.

ID space address	Description	Value
$00	ASCII “I”	$49
$02	ASCII “P”	$50
$04	ASCII “A”	$41
$06	ASCII “C”	$43
$08	Manufacturer identification	$11
$0A	Module type	$32
$0C	Revision module	$0A
$0E	Reserved	$00
$10	Driver ID, low byte	
$12	Driver ID, high byte	
$14	Number of bytes used	$0A
$16	CRC	
$18-$3E	User space	

Table 2-1 IDSEL0 SPACE byte content

2.2 IOSPACE

IP_DIO48 uses the IOSPACE for the following registers.
Access can be word or byte access with even address being the lower byte and odd address being the upper byte.

Slave Address	NAME	REGISTER	TYPE	R/W
$00-$01	Port [15..0] I/O Configuration	CNFG0		R/W
$02-$03	Port [31..16] I/O Configuration	CNFG1		R/W
$04-$05	Port [47..32] I/O Configuration	CNFG2		R/W
$06-$07	Output Port [15..0] ON/OFF	OUT0_P		R/W
$08-$09	Output Port [31..16] ON/OFF	OUT1_P		R/W
$0A-$0B	Output Port [47..32] ON/OFF	OUT2_P		R/W
$0C-$0D	Output Port [15..0] status (cyclone)	OUT0_S		R
$0E-$0F	Output Port [31..16] status (cyclone)	OUT1_S		R
$10-$11	Output Port [47..32] status (cyclone)	OUT2_S		R
$12-$13	Output configuration selection	OUT_CONF		R/W
$14-$15	Host_strobe_out	HOST_STRB_OUT		W
$16-$17	Toggle clock # 0	TOOGLE_0L		R/W
$18-$19	Toggle clock # 0	TOOGLE_0H		R/W
$1A-$1B	Toggle clock # 1	TOOGLE_1L		R/W
$1C-$1D	Toggle clock # 1	TOOGLE_1H		R/W
$20-$21	Input Port [15..0] debounced	RD_INP0_D		R
$22-$23	Input Port [31..16] debounced	RD_INP1_D		R
$24-$25	Input Port [47..32] debounced	RD_INP2_D		R
$26-$27	Input Port [15..0] strobed	RD_INP0_S		R
$28-$29	Input Port [31..16] strobed	RD_INP1_S		R
$2A-$2B	Input Port [47..32] strobed	RD_INP2_S		R
				W
$2C-$2D	Input Port [15..0] latched	RD_INP0_L		R
$2E-$2F	Input Port [31..16] latched	RD_INP1_L		R
$30-$31	Input Port [47..32] latched	RD_INP2_L		R
$32-$33	Input Port [15..0] interrupt pending and reset	RD_INTPEND_RST_0		R/W

$34-$35	Input Port [31..16] interrupt pending and reset	RD_INTPEND_RST_1		R/W
$36-$37	Input Port [47..32] interrupt pending and reset	RD_INTPEND_RST_2		R/W
$38-$39	Input Port Mask [15..0] latched	MASK0		R/W
$3A-$3B	Input Port Mask [31..16] latched	MASK1		R/W
$3C-$3D	Input Port Mask [47..32] latched	MASK2		R/W
$38-$39	Input Port Mask [15..0] latched	MASK0		R/W
$3A-$3B	Input Port Mask [31..16] latched	MASK1		R/W
$3C-$3D	Input Port Mask [47..32] latched	MASK2		R/W
$40	IVR0 for INTREQ0	IVR0		R/W
$42	IVR1 for INTREQ1	IVR1		R/W
$44-$45	Global Interrupt reset [47..0]	GLOBAL_INT_RST		W
$46	Interrupt Group (byte) pending	INT_GROUP_PEND		R
$48-$49	INPUT LATCH pulse SOURCE	INPUT_LATCH_SOURCE		W
$4A	HOST_STROBE_LATCH_IN	HOST_STRB_IN		W
$4C-$4D	CONFIGURATION REGISTER_0	CTRL0		R/W
$4E-$4F				W
$50-$51	INPUT_CONFIGURATION CH #0- CH#1	INPUT_CONF_0_1		R/W
$52-$53	INPUT_CONFIGURATION	INPUT_CONF_2_3		R/W
$54-$55	INPUT_CONFIGURATION	INPUT_CONF_4_5		R/W
$56-$57	INPUT_CONFIGURATION	INPUT_CONF_6_7		R/W
$58-$59	INPUT_CONFIGURATION	INPUT_CONF_8_9		R/W
$5A-$5B	INPUT_CONFIGURATION	INPUT_CONF_10_11		R/W
$5C-$5D	INPUT_CONFIGURATION	INPUT_CONF_12_13		R/W
$5E-$5F	INPUT_CONFIGURATION	INPUT_CONF_14_15		R/W
$60-$61	INPUT_CONFIGURATION CH #16- CH#31	INPUT_CONF_16_17		R/W
$62-$63	INPUT_CONFIGURATION	INPUT_CONF_18_19		R/W
$64-$65	INPUT_CONFIGURATION	INPUT_CONF_20_21		R/W
$66-$67	INPUT_CONFIGURATION	INPUT_CONF_22_23		R/W
$68-$69	INPUT_CONFIGURATION	INPUT_CONF_24_25		R/W
$6A-$6B	INPUT_CONFIGURATION	INPUT_CONF_26_27		R/W

$6C-$6D	INPUT_CONFIGURATION	INPUT_CONF_28_29		R/W
$6E-$6F	INPUT_CONFIGURATION	INPUT_CONF_30_31		R/W
$70-$71	INPUT_CONFIGURATION CH #32- CH#47	INPUT_CONF_32_33		R/W
$72-$73	INPUT_CONFIGURATION	INPUT_CONF_34_35		R/W
$74-$75	INPUT_CONFIGURATION	INPUT_CONF_36_37		R/W
$76-$77	INPUT_CONFIGURATION	INPUT_CONF_38_39		R/W
$78-$79	INPUT_CONFIGURATION	INPUT_CONF_40_41		R/W
$7A-$7B	INPUT_CONFIGURATION	INPUT_CONF_42_43		R/W
$7C-$7D	INPUT_CONFIGURATION	INPUT_CONF_44_45		R/W
$7E-$7F	INPUT_CONFIGURATION	INPUT_CONF_46_47		R/W

3 Registers description

3.1 I/O PORT Configuration

Register	I/O channel	Iospace address +
CNFG_0	I/O #15 – 0	$00-$01
CNFG_1	I/O #31 – 16	$02-$03
CNFG_2	I/O #47 – 32	$04-$05

A”0” selects the I/O pins as INPUT.
A”1” selects the I/O pins as OUTPUT.
Register is cleared upon POWER-ON RESET.

3.2 I/O AS OUTPUT PORT

The output channels have a two level register.

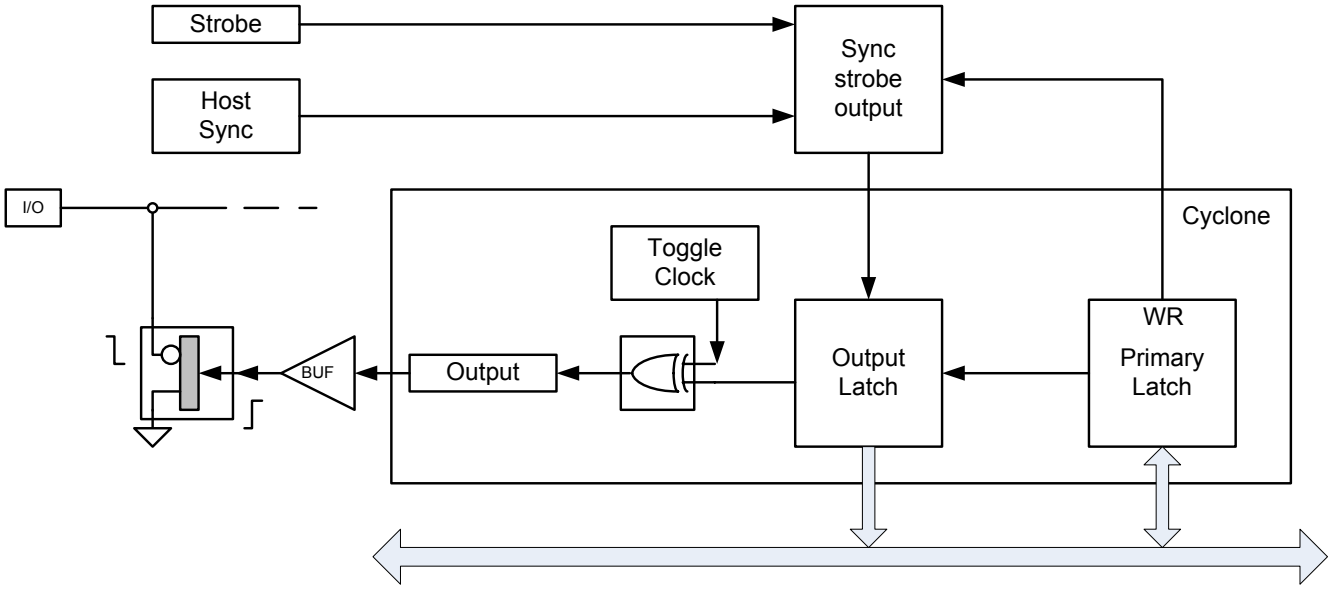
- The primary register that contains the data written at the output address by the processor.
- The secondary register or output register.

The output register controls the behavior of the VMOS. The data from the primary register are transfer in two different way:
By default the output register is updated immediately at the end of a write into the primary register, but it is possible to synchronize the output register update by enabling the corresponding bit and having the host or an external signal generating a synchronization pulse.

The status of the output channel can be read-back at each register level.

- Primary register IOSPACE + $06-$0B
- Output register (pin-out of the cyclone F.P.G.A.) IOSPACE + $0C-$11
- Connector (VMOS drain, Read-back input) IOSPACE + $20-$25

A ”0” open drain is “OFF” means NON conductive.
A ”1” open drain is “ON” means conductive. R_{on} is 0.3Ω.
Writing a “1” or a “0” to a port defined as INPUT has no effect.
IF PORT is selected as an Output, read-back of the register provides the status of the bit written. Writing a “1” will read-back a “1”. This bit controls the VMOS Gate. The VMOS behaves as an inverter. When Gate is “1”, it is conductive and the Drain is close to analog GND or “”0”. A read-back of the Input Status Register will provide the level of the Drain Output which will appear as a “0”.
Register is cleared upon IP RESET.



3.2.1 PRIMARY REGISTER

Register	I/O channel	Iospace address +
OUT_0_P	I/O #15 – 0	$06-$07
OUT_1_P	I/O #31 – 16	$08-$09
OUT_2_P	I/O #47 – 32	$0A-$0B

3.2.2 OUTPUT REGISTER

Structure of the output register is the same as above. They are read only registers. The output register control the gate of the VMOS through a non inverting buffer.

Register	I/O channel	Iospace address +
OUT_0_S	I/O #15 – 0	$0C-$0D
OUT_1_S	I/O #31 – 16	$0E-$0F
OUT_2_S	I/O #47 – 32	$10-$11

3.2.3 OUT_SYNC_STROBE_EN REGISTER

IOSPACE + $12-$13

Each group of 8 channel can have they output register update in a synchronous fashion by a synchronization pulse . It can be host write cycle at location $1E-$1F or an external IP_strobe signal.

BD07	BD06	BD05	BD04	BD03	BD02	BD01	BD00
		Group_40	Group_32	Group_24	Group_16	Group_8	Group_0

This register is also use to enable the output of a group to be toggle by Toggle_clk_0 or Toggle_clk_1

BD15	BD14	BD13	BD12	BD11	BD10	BD09	BD08
	Toggle_swap	Toggle_clk_1	Toggle_clk_0	Toggle_clk_1	Toggle_clk_0	Toggle_clk_1	Toggle_clk_0
		Group_40	Group_32	Group_24	Group_16	Group_8	Group_0

3.2.4 HOST SYNCRO PULSE

IOSPACE + $14-$15

A host write cycle at this location will transfer the data from the primary register to the Output register for the channel group that have been programmed to have output update synchronously.
The source of the pulse needs to be already selected by programming the *OUT_SYNC_STROBE_EN* register.

Also the HOST SYNCRO PULSE signal can be output to the pin IPSTROBE of the IPBUS. See Control register_0.

3.2.5 TOGGLE CLOCK

IOSPACE + $16-$17, $18 TOGGLE_0
IOSPACE + $1A-$1B, $1C TOGGLE_1

Two independent Toggle_ clock can be use to toggle the output of a group (8) .
Each clock is 24 bit counters. It require three bytes for programmation.
For each group Toggle_output is enable by a bit located into the ***OUT_SYNC_STROBE_EN*** **register**.
Even group are allocated the Toggle_0 clock,
Odd group are allocated Toggle_1 clock or Toggle_0 clock if bit # 14 of the ***OUT_SYNC_STROBE_EN*** **register** is set to “1”.

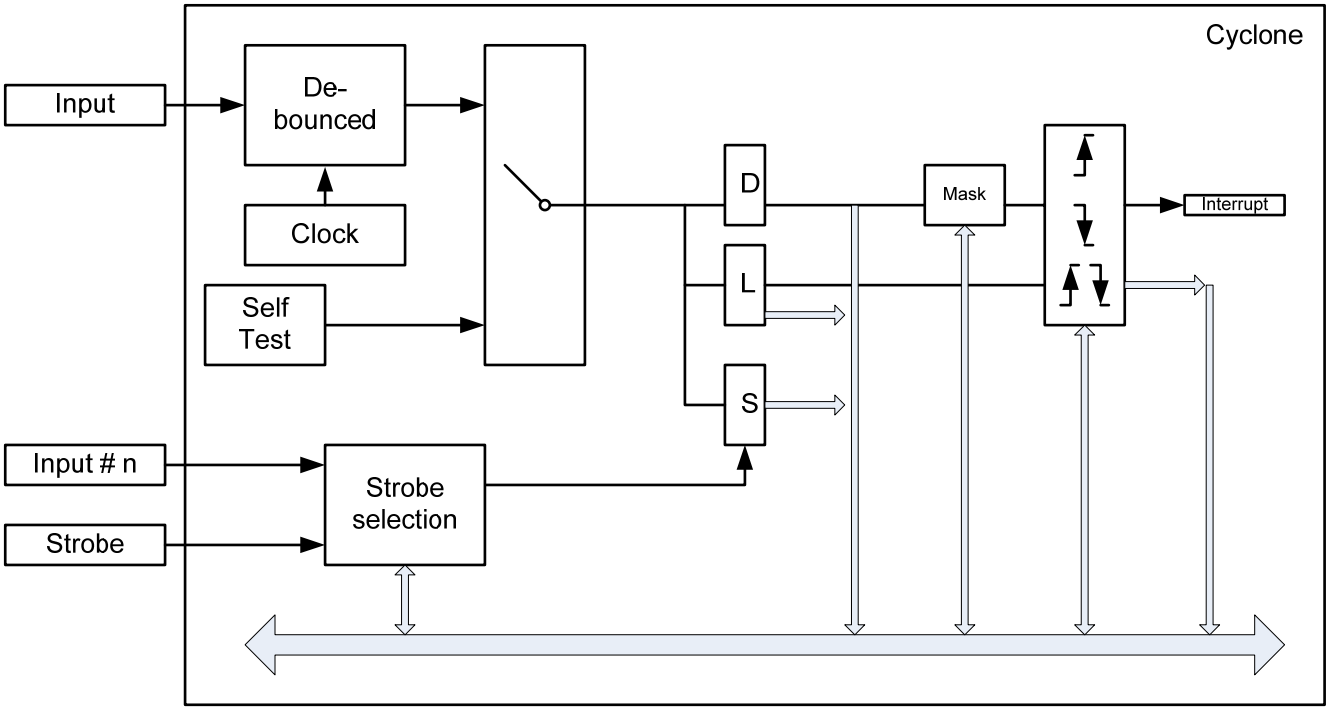
3.3 I/O AS INPUT PORT

All I/O pin are defined as input upon power-on.
Each input can be the source of interrupt upon:

- a positive transition and/or a negative transition
- a change of sign in comparison with a precedent input status latched.

Each input signal is de-bounced by using a separate 24 bit clock.
The debouncing time is from 1 µS up to 16 seconds. The input clock is 2 MHz and the filter uses 4 clocks to be valid.
Each I/O pin use a byte for configuration, even byte is for even channel and odd byte for odd channel.
Each channel has an independent setting.
The status of the input can then be read at different level of the internal logic.

- Input de-bounced
- Input strobed by an external signal
- Input latched when input is source of an enable interrupt.



3.3.1 INPUT PORT CONFIGURATION

IOSPACE + $50-$7F

Each I/O line selected as input need to be configured to extract the best use of the input signal.
De-bounce clock is set to 1 µS upon power-on reset.

BD07	BD06	BD05	BD04-BD00
SELF_TEST	NEG_EDGE	POS_EDGE	DE-BOUNCE CLOCK SELECTION CH _0

BD15	BD14	BD13	BD12-BD08
SELF_TEST	NEG_EDGE	POS_EDGE	DE-BOUNCE CLOCK SELECTION CH _1

Register is cleared upon IP RESET. All interrupt are disable, de-bounce clock is set to 1 uS. Binary increment of the clock frequency is use, 1 µS,2 µS,4 µS,8 µS, etc…

3.3.2 INPUT DE-BOUNCED

Each register reading will use three words address and will have the same structure as below.
Registers are cleared upon power-on reset.
If port is selected as an Output, a Read to the location will return the status of the I/O pin de-bounced.

Register	I/O channel	Iospace address +
RD_INP0_D	I/O #15 – 0	$20-$21
RD_INP1_D	I/O #31 – 16	$22-$23
RD_INP2_D	I/O #47 – 32	$24-$25

3.3.3 INPUT STROBED

Each group of I/O can be written into a register by a strobe signal which source is selected by 2 bits.

Register	I/O channel	Iospace address +
RD_INP0_S	I/O #15 – 0	$26-$27
RD_INP1_S	I/O #31 – 16	$28-$29
RD_INP2_S	I/O #47 – 32	$2A-$2B

3.3.4 INPUT STROBE SOURCE PULSE REGISTER

IOSPACE + $48 (byte access)

Each group of I/O can be strobed ed into a register by a signal which source is selected with 2 (two) bits by group.

BD07	BD06	BD05	BD04	BD03	BD02	BD01	BD00
Group_24_1	Group_24_0	Group_16_1	Group_16_0	Group_8_1	Group_8_0	Group_0_1	Group_0_0

BD15	BD14	BD13	BD12	BD11	BD10	BD09	BD08
				Group_40_1	Group_40_0	Group_32_1	Group_32_0

GROUP_X_1	GROUP_X_0	SOURCE
0	0	None
0	1	/WR_HOST_LATCH_IN IOSPACE+$4A
1	0	EXTERNAL IPSTROBE
1	1	ONE OF THE INPUT DEFINE BY CTRL_[13..8]

3.3.5 INPUT LATCHED

De-bounced Inputs can be latched upon a read of the Input de-bounced register or at the end of an interrupt cycle.
Data latched can be use for detection of a Change Of sign C.O.S. of one or more input.
If enabled an interrupt is generated.

Register	I/O channel	Iospace address +
RD_INP0_L	I/O #15 – 0	$2C-$2D
RD_INP1_L	I/O #31 – 16	$2E-$2F
RD_INP2_L	I/O #47 – 32	$30-$31

3.3.6 HOST LATCH PULSE

IOSPACE + $4A

A host write-cycle at this location will latch the input line value into a register.
This signal can also be output to the pin IPSTROBE of the IPBUS.

3.4 INTERRUPTS

3.4.1 INPUT PORT INTERRUPT PENDING AND RESET

Upon receiving an interrupt the host can check the interrupt source:

- At the level of the INTERRUPT GROUP PENDING REGISTER IOSPACE + $4A

Each bit is use to identifier which group has generated an interrupt.
Group # 0 use bit #0 and so on.

- At the level of each group to identifies the channel(s) source of interrupt reading registers INTPEND_0 to 2.

A bit read as a "1" will signify that the associated input has change of sign.
The COS (Change Of State) is latched.

To clear the interrupt write a"1" at the same location with the corresponding bit associated with the interrupt source. This will clear the interrupt source.

Register	I/O channel	Iospace address +
RD_INTPEND0_L	I/O #15 – 0	$32-$33
RD_INTPEND1_L	I/O #31 – 16	$34-$35
RD_INTPEND2_L	I/O #47 – 32	$36-$37

3.4.2 INPUT PORT MASK

Each bit set to "1" enables the corresponding input line to be active for interrupt purpose.

Register	I/O channel	Iospace address +
MASK_0	I/O #15 – 0	$38-$39
MASK_1	I/O #31 – 16	$3A-$3B
MASK_2	I/O #47 – 32	$3C-$3D

3.4.3 INTERRUPT VECTOR REGISTER

3.4.3.1 IVR0 Interrupt Vector Register
IOSPACE + $40 (byte access)
Interrupt Vector register can be accessed in byte only.

This eight-bit register can be read and written to by the host carrier module. The vector is automatically provided upon INTSPACE cycle performed by the Host.

3.4.3.2 IVR1 Interrupt Vector Register
IOSPACE + $42 (byte access)
Interrupt Vector register can be accessed in byte only.

This eight-bit register can be read and written to by the host carrier module. The vector is automatically provided upon INTSPACE cycle performed by the Host.

3.4.4 GLOBAL INTERRUPT RESET

IOSPACE + $44 (byte access)

A host write-cycle at this location will clear all the board pending interrupt.

3.4.5 INTERRUPT GROUP PENDING

IOSPACE + $46 (byte access)

Any bit set to “1” in this register indicates which group has one or more interrupt pending.

BD07	BD06	BD05	BD04	BD03	BD02	BD01	BD00
		Int_Group_40	Int_Group_32	Int_Group_24	Int_Group_16	Int_Group_8	Int_Group_0

3.4.6 CONTROL REGISTER CTRL0

IOSPACE + $4C

BD07	BD06	BD05	BD04	BD03	BD02	BD01	BD00
				POS_IPSTROBE	32MHZ	INTREQ#1 ENABLE	INTREQ#0 ENABLE

BD15	BD14	BD13	BD12	BD11	BD10	BD09	BD08
CTRL_[15]	CTRL_[14]	CTRL_[13]	CTRL_[12]	CTRL_[11]	CTRL_[10]	CTRL_[9]	CTRL_[8]

Another possibility to latch the present input status is to select one of the 48 input as an input strobe.
Bit [13..8] select the I/O line.

4 CONNECTORS

4.1 IP BUS INTERFACE

		P4		
Pin 1	GND		Pin 26	GND
Pin 2	+5V		Pin 27	+5V
Pin 3	IPRESET*		Pin 28	IPRW*
Pin 4	XLD00		Pin 29	IDSEL0*
Pin 5	XLD01		Pin 30	DMAREQ0*
Pin 6	XLD02		Pin 31	MEMSEL0*
Pin 7	XLD03		Pin 48	DMAREQ1*
Pin 8	XLD04		Pin 33	INTESEL0*
Pin 9	XLD05		Pin 34	DMACK*
Pin 10	XLD06		Pin 35	IOSEL0*
Pin 11	XLD07		Pin 36	
Pin 12	XLD08		Pin 37	XLA01
Pin 13	XLD09		Pin 38	DMAEND*
Pin 14	XLD10		Pin 39	XLA02
Pin 15	XLD11		Pin 40	ERROR*
Pin 16	XLD12		Pin 41	XLA03
Pin 17	XLD13		Pin 42	INTREQ0*
Pin 18	XLD14		Pin 43	XLA04
Pin 19	XLD15		Pin 44	INTREQ1*
Pin 20	IPBS0*		Pin 45	XLA05
Pin 21	IPBS1*		Pin 46	STROBE*
Pin 22			Pin 47	XLA06
Pin 23			Pin 48	IPACK*
Pin 24	+5V		Pin 49	+5V
Pin 25	GND		Pin 50	GND

Table 4 IPBUS connector

4.2 I/O PORT

PIN	I/O	PIN	I/O
Pin 1	I/O 01	Pin 26	I/O 05
Pin 2	I/O 02	Pin 27	I/O06
Pin 3	I/O 03	Pin 28	I/O 07
Pin 4	I/O 04	Pin 29	I/O 08
Pin 5	GND	Pin 30	GND
Pin 6	REF0108	Pin 31	P_0108
Pin 7	I/O 09	Pin 48	I/O 13
Pin 8	I/O 10	Pin 33	I/O 14
Pin 9	I/O 11	Pin 34	I/O 15
Pin 10	I/O 12	Pin 35	I/O 16
Pin 11	GND	Pin 36	GND
Pin 12	REF0916	Pin 37	P_0916
Pin 13	I/O 17	Pin 38	I/O 21
Pin 14	I/O 18	Pin 39	I/O 22
Pin 15	I/O 19	Pin 40	I/O 23
Pin 16	I/O 20	Pin 41	I/O 24
Pin 17	GND	Pin 42	GND
Pin 18	REF1724	Pin 43	P_1724
Pin 19	I/O 25	Pin 44	I/O 29
Pin 20	I/O 26	Pin 45	I/O 30
Pin 21	I/O 27	Pin 46	I/O 31
Pin 22	I/O 28	Pin 47	I/O 48
Pin 23	GND	Pin 48	GND
Pin 24	REF2548	Pin 49	P_2548
Pin 25	GND	Pin 50	GND

Table 2 I/O PORT

5 SOFTWARE INFORMATION

5.1 DIO48_DetectBoards

short DIO48_DetectBoards (UINT16 *nbrOfBoards)

This function detects the number of DIO48 cards present in the chassis

Error Codes
DIO48_INTERNAL_ERROR

5.2 DIO48_ Open

short DIO48_Open (
    UINT16 brdNbr,
    dio48handle *dio48
)

This function initializes the board control structure and returns a handle to it.

Error Codes
DIO48_INTERNAL_ERROR
DIO48_INVALID_BOARD_NUM

5.3 DIO48_ ResetBoard

short DIO48_ ResetBoard (
    dio48handle dio48
)

This function resets the board.

Error Codes
DIO48_INVALID_HANDLE

5.4 DIO48_ Close

short DIO48_ Close(
    dio48handle dio48
)

This function frees the resources for the specified board and releases the handle.

Error Codes
DIO48_INVALID_HANDLE

5.5 DIO48_ ConfigOutputMode

short DIO48_ConfigOutputMode(
    dio48handle dio48,


```
        UINT16 chanNbr
)
```
This function configures a channel in the output mode. The IO channel number is a value between 1 and 48.

Error Codes
DIO48_INVALID_HANDLE
DIO48_INVALID_CHANNEL_NUM

5.6 DIO48_ WriteChannelData

```
short DIO48_WriteChannelData (
        dio48handle dio48,
        UINT16 chanNbr,
        UINT16 data
)
```

This function writes the data to the output for the specified channel, in the primary register. Data must be 0 or 1. The IO channel number is a value between 1 and 48.

Error Codes
DIO48_INVALID_HANDLE
DIO48_INVALID_CHANNEL_NUM
DIO48_INPUT_MODE

5.7 DIO48_ EnableOutput

```
short DIO48_EnableOutput (
        dio48handle dio48,
        UINT16 chanNbr
)
```

The function is used to bypass channel data to the output. If the channel number is 0, it enables all the channels.

Error Codes
DIO48_INVALID_HANDLE
DIO48_INVALID_CHANNEL_NUM
DIO48_INPUT_MODE

5.8 DIO48_ ReadOutputData

```
short DIO48_ReadOutputData (
        dio48handle dio48,
        UINT16 chanNbr,
        UINT16 outputType,
        UINT16 *data
)
```

The function is used to read back the output latch data for a specified channel. The IO channel number is a value between 1 and 48. The outputType is 0 for primary output, and 1 for secondary output.

Error Codes
DIO48_INVALID_HANDLE

DIO48_INVALID_CHANNEL_NUM
DIO48_INVALID_VALUE
DIO48_INPUT_MODE

5.9 DIO48_ ConfigInputMode

```
short DIO48_ConfigInputMode (
        dio48handle dio48,
        UINT16 chanNbr,
        UINT16 selfTestEnable,
        UINT16 inputMode,
        UINT16 logicSelection,
        UINT16 strobe
)
```

The function is used to configure a channel in Input mode and enable/disable the self-test for it. The IO channel number is a value between 1 and 48. selfTestEnable is 0 for self-test disabled, and 1 for self-test enabled. inputMode is 1 for input interrupt mode, 2 for state-change mode, and 3 for strobe-in mode. logicSelection is 0 for rising edge triggering, and 1 for falling edge triggering. selfTestEnable is 0 for self-test disabled, and 1 for self-test enabled. strobe is used only when inputMode = 3 (strobe-in mode) and is 1 for software trigger, 2 for backplane strobe trigger mode, and 3 for master software strobe trigger.

Error Codes
DIO48_INVALID_HANDLE
DIO48_INVALID_CHANNEL_NUM
DIO48_INVALID_SELF_TEST_ENABLE_VAL
DIO48_INVALID_INPUT_MODE
DIO48_INVALID_LOGIC_SEL
DIO48_INVALID_STROBE_MODE

5.10 DIO48_ ReadInputData

```
short DIO48_ReadInputData (
        dio48handle dio48,
        UINT16 chanNbr,
        UINT16 mode,
        UINT16 *data
)
```

The function is used to read back the output latch data for a specified channel. The IO channel number is a value between 1 and 48. The data returned is either 0 or 1. The mode is a value from 0 to 3:
0 – Before mask status for the channel
1 – Input Interrupt for the channel
2 – Previous data status for the channel
3 – Strobe data input for the channel

Error Codes
DIO48_INVALID_HANDLE
DIO48_INVALID_CHANNEL_NUM
DIO48_INVALID_VALUE
DIO48_INPUT_MODE

5.11 DIO48_ EnableSelfTest

short DIO48_ EnableSelfTest (
dio48handle dio48,
UINT16 chanNbr,
UINT16 selfTestEnable
)

The function is used to bypass enable or disable the test mode on a given channel. The IO channel number is a value between 1 and 48. selfTestEnable is 0 for self-test disabled, and 1 for self-test enabled.

Error Codes
DIO48_INVALID_HANDLE
DIO48_INVALID_CHANNEL_NUM
DIO48_INVALID_SELFTEST_ENABLE_VAL

5.12 DIO48_ ConfigToggleMode

short DIO48_ ConfigToggleMode (
dio48handle dio48,
UINT16 group,
float frequency
)

The function is used to configure the frequency of the clock output for the required group of channels. The programmable toggle frequency range is 1Hz to 3kHz. The frequency resolution is +/-1Hz. The channel number is a value between 1 and 16. The group 1 is from channel 1 to channel 8, the group 2 is from channel 9 to channel 16.

Error Codes
DIO48_INVALID_HANDLE
DIO48_INVALID_CHANNEL_NUM
DIO48_INVALID_FREQUENCY

5.13 DIO48_ StartToggleMode

short DIO48_ StartToggleMode (
dio48handle dio48,
UINT16 chanNbr
)

The function is used to start toggling the specified output channel. The toggling frequency is common to all the channels in a group. The channel number is a value between 1 and 16.

Error Codes
DIO48_INVALID_HANDLE
DIO48_INVALID_CHANNEL_NUM

5.14 DIO48_ StopToggleMode

short DIO48_ StopToggleMode (
dio48handle dio48,
UINT16 chanNbr
)

The function is used to stop toggling the specified output channel. The output state on the board after successful completion is as selected by the secondary latch.

Error Codes
DIO48_INVALID_HANDLE
DIO48_INVALID_CHANNEL_NUM

5.15 DIO48_ GetErrorMsg

void DIO48_GetErrorMsg (
short errCode,
char **ErrMsg
)
This function returns a string corresponding to the error code.

Error Codes as input
DIO48_INTERNAL_ERROR
DIO48_INVALID_BOARD_NUM
DIO48_INVALID_HANDLE
DIO48_INVALID_CHANNEL_NUM
DIO48_INVALID_SELF_TEST_ENABLE_VAL
DIO48_INVALID_VALUE
DIO48_INPUT_MODE
DIO48_OUTPUT_MODE
DIO48_INVALID_LOGIC_SEL
DIO48_INVALID_STROBE_MODE
DIO48_INVALID_GROUP
DIO48_INVALID_FREQUENCY

