

# **IP-48ADM16TH**

**High Density 48-channel, 16-bit A/D Converter**

## **REFERENCE MANUAL**

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## ***IP-48ADM16TH HARDWARE REFERENCE MANUAL***

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History :

Rev 1.3:

Correct input jumper Table.

Rev 1.4 :

Correct Acquisition Control register.

Rev 1.5 :

Correct Address map base address. 3.2.1,3.2.3

Table2.1.3.1, table 3.3 IO

Internal clock divisor

Rev 1.6:

Modified the clock divisor section and added in sampling period calculation (3.3.2).

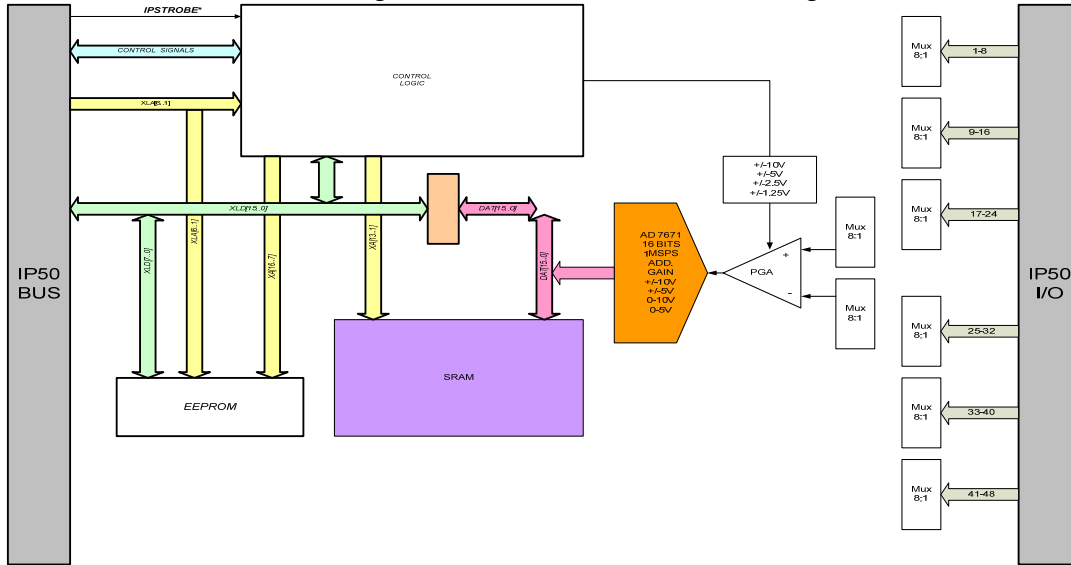
## **1. GENERAL DESCRIPTION**

### **1.1 INTRODUCTION**

The IP-48ADM16 is a 16 bit single width IP module designed for high speed burst A/D data acquisition in 16 bits. The primary features of the IP-48ADM16 are:

- Mix of up to 48 single-ended or 24 differential channels
- On-board voltage reference ( +2.5v, -2.5v )
- Fault and Over-voltage Protected (-40 V, + 55 V) multiplexer
- 1 MSPS 16-bit A/D converter
- Software programmable single-ended (SE) or differential (DIFF) input and gain for each channel
- Input Ranges:-  $\pm 10V$ ,  $\pm 5V$ ,  $\pm 2.5V$ ,  $\pm 1.25V$  using a software programmable gain amplifier
- Additional jumper selectable gain from A/D converter(1-2-4-8)
- Acquisition time  $\leq 1.3 \mu S$  without gain and channel change
- Internal sequencer with channel list for acquisition of selected channels
- 64k x 16 DATARAM dual ported storage
- Channel list in RAM.
- Programmable Interrupt
- Flash EEPROM for gain/offset correction data
- On board input switches for offset or gain calibration
- Dual threshold level detection for each channel with interrupt possibilities
- Analog trigger with any channel and level selection
- 32 MHz IP clock

Figure 1.1 : Data Flow Block Diagram



## 1.2 FUNCTIONAL DESCRIPTION

A data flow block diagram of the IP-48ADM16 is presented in Figure 1-1.

The IP-48ADM16 has 6 fault-protected CMOS analog multiplexers. Each multiplexer has 8 inputs and one common output. These outputs are acquired by differential multiplexers. The differential inputs can then be configured for single-ended, differential, or calibration modes. These outputs go then to a PGA where the gain can be set for 1, 2, 4, or 8

After the conversion, the data is stored in a 64k by 16 dual ported Data RAM. Memory pointers can be selected to limit the number of scan gathered, as well as used to control the generation of interrupts. Continuous acquisition and transfers can be performed.

Two different threshold levels can be selected for each channel. When enabled the result of the A/D acquisition is compared with one or both of the thresholds and will generate a programmable interrupt to the host if the channel is out of the defined band gap or into the defined band gap.

The board can also be set to monitor one channel and start the acquisition on all the Channel List whenever the first channel in the channel list is inside or outside a pre-programmed range.

A programmable digital filter selects the minimum number of consecutive values before the interrupt is generated, or the acquisition starts.

## **2. THEORY OF OPERATION**

### **2.1 ANALOG INPUTS**

There are two groups of 24-channel analog inputs that are multiplexed using two eight-channel multiplexers.

A state machine scans a Channel List, acquires the data and stores them into the DATARAM memory.

Each multiplexers output goes respectively to a second level of multiplexers that determines whether the data is in single-ended, differential or in calibration mode, using the data from the Channel List for that particular acquisition. The output of these multiplexers is then fed into an instrument amplifier which gain is programmed on the fly, also from the Channel List. This configuration allows the user to have a mix of single ended or differential inputs selected on the fly from the Channel List.

While a 1 MSPS A/D converter convert the selected channel, it is possible to select the next channel to reduce settling time. The channel list of up to 64 location is used for this purpose.

Also, it is possible to inject a reference signal at the level of the switch upstream of the PGA amplifier and A/D converter to get a data reference.

The software programmable PGA allows selecting an input range of +/-10v, +/-5v, +/-2.5v, or +/-1.25v, based on a gain of 1, 2, 4, or 8, when the A/D is selected with a +/-10V range by jumper.

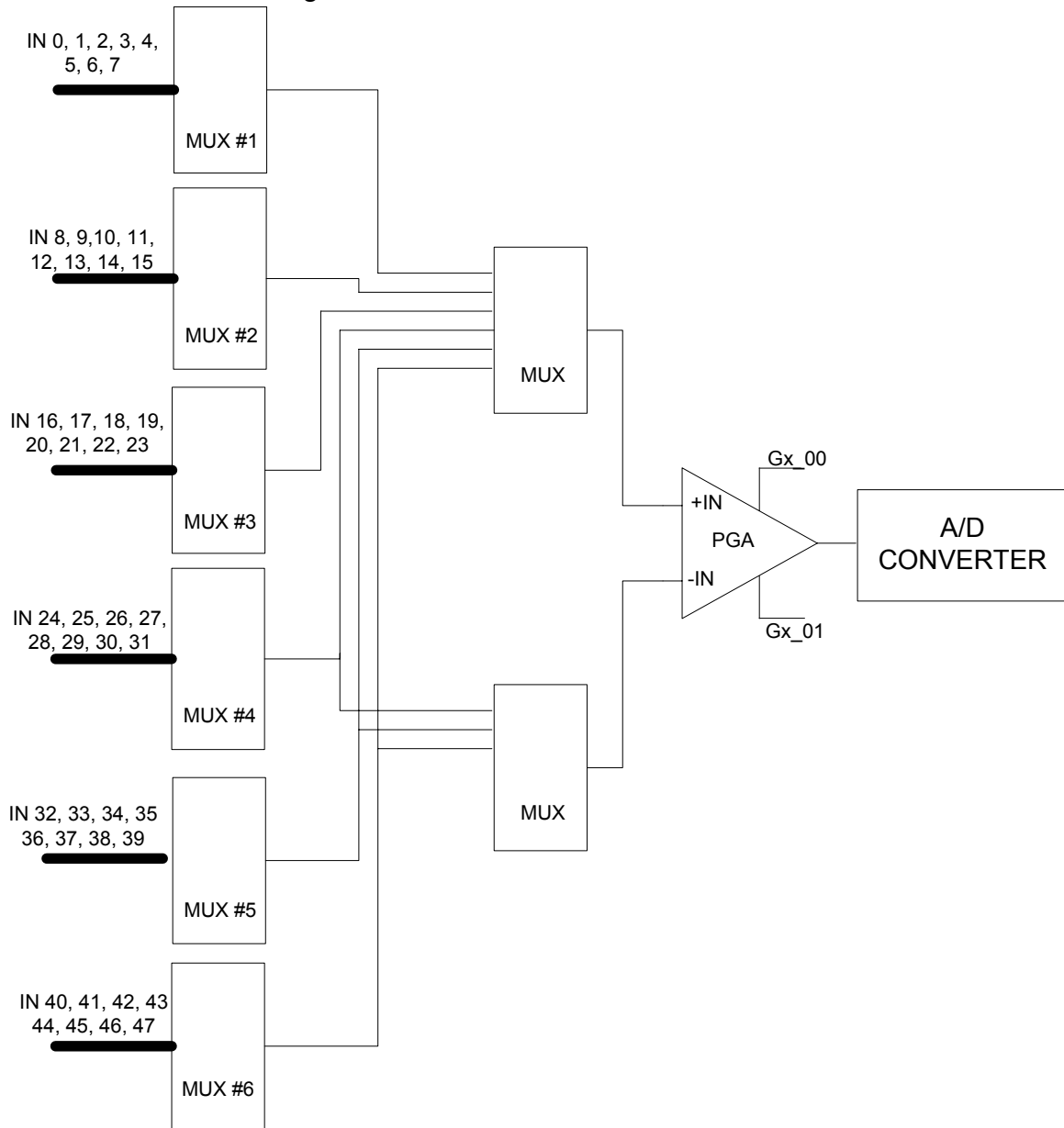
Additional jumper selectable input range can be selected by modifying the A/D input level section.

The A/D has a jumper selected programmable gain. The selection applies to all the inputs of the A/D.

| <b>Input level</b> | <b>W1</b>      | <b>J3</b> |
|--------------------|----------------|-----------|
| +/-10v             | 1-3, 4-6, 8-10 | 1-2       |
| +/-5v              | 1-2, 4-6, 8-10 | 1-2       |
| +/-2.5v            | 1-2, 4-6, 9-10 | 1-2       |
| 0 -+10v            | 1-2, 3-5, 8-10 | 1-2       |
| 0 -+5v             | 1-2, 3-5, 9-10 | 1-2       |
| 0 -+2.5v           | 1-2, 5-7, 9-10 | 1-2       |

Note: J3 is factory use, do not change.

Below is a simple block diagram to show how the data is processed from the input to the A/D conversion in single-ended and differential modes.



**2.1.1 Single-Ended Mode**

**2.1.2 Differential Mode**

In differential mode channel #0 is associated with channel #24 and so on, until the channel #23 being associated with channel #47.



## **2.2 A/D Converter**

The converter used is an Analog Device AD7671. The A/D converter operates continuously at the selected sampling rate. The A/D is a 1-MSPS 16-bit A/D converter.

More information is available at [www.analogdevices.com](http://www.analogdevices.com).

### **2.2.1 Acquisition Mode**

Setting up the IP-48ADM16 for acquisition is done in several steps:

- 1) select the Scan clock source:
  - Internal with the internal timer (the scan clock divisor needs to be programmed as well.
  - Host writing to the Start Acquisition register.
  - Using the signal IPstrobe selected as input.
- 2) Initializing the Channel Ram list with the channels to acquire:

The A/D result of each channel is stored into the DATARAM in incrementing order. One to N scan can be stored. Setting the DATARAM pointer to N scan list will store N scan then the DATARAM re-start to address zero.
- 3) Next select the trigger source that will start the acquisition
  - Host write to the Start Acquisition address (any write will start).
  - Input corresponding to channel #47 uses as an external Event Trigger (need to set-up jumper xx )
  - Threshold A/D converter
- 4) Different possibilities of auto-triggering are available to get automatically more acquisitions:
  - a) Nibble scan. One or N Scan are processed and the state machine stops until a new trigger is generated
  - b) Continuous scan is performed filling the DATARAM up to the DATARAM pointer and automatic restart from beginning, using the internal timer.
  - c) Host can stop the State machine by writing at address Stop acquisition. The last address written is then available at the DATARAM SM ADDRESS location register.
  - d) If using the Threshold A/D converter acquisition can be stopped every timer the signal is back into the defined zone. Bit # need to be set to "1"
- 5) Program the interrupts as needed

### **2.2.2 CONTINUOUS MODE**

If continuous acquisition is desired, then the following procedure is used. Remember that in a real world scenario, it is not possible to read the data at the maximum rate that the IP is capable of. There is no way to predict the exact performance as it depends on the carrier board and the application.

Setting the DATARAM pointer with a desired address lower than the End address or a number of scan lower than the total scan and enabling an interrupt, the host can “throttle” the read of A/D data.

### **3. INTERFACE TO THE IP CARRIER**

The IP carrier controls this IP via a set of registers in the IOSPACE and MEMORY space.

#### **3.1 IDSPACE**

Each IP has a set of register allowing the local Host to identifies the IP module Manufacturer, type , revision,etc.

Base Address is located in the IP Identification Base address.

These registers are read only.

| <b>ID space address</b> | <b>Description</b>          | <b>Value</b> |
|-------------------------|-----------------------------|--------------|
| \$01                    | Ascii "I"                   | \$49         |
| \$03                    | Ascii "P"                   | \$50         |
| \$05                    | Ascii "A"                   | \$41         |
| \$07                    | Ascii "H"                   | \$48         |
| \$09                    | Manufacturer identification | \$11         |
| \$0B                    | Module type                 | \$30         |
| \$0D                    | Revision module             | \$0A         |
| \$0F                    | Reserved                    | \$00         |
| \$11                    | Driver ID,low byte          | \$00         |
| \$13                    | Driver ID,high byte         | \$00         |
| \$15                    | Number of bytes used        | \$0A         |
| \$17                    | CRC                         | \$00         |
| \$19-\$3F               | User space                  | \$00         |

**Table 3.1: IDSPACE Registers contents**

#### **3.2 MEMSPACE**

##### **3.2.1 Address Map**

| <b>MEMORY +</b> | <b>R/W</b> | <b>BITS</b> | <b>Register</b>       |
|-----------------|------------|-------------|-----------------------|
| 0x00000-1FFFF   | R/W        | 16          | DATARAM 128k bytes    |
| 0x20000-27FFF   | R/W        | 8           | FLASH memory 4k bytes |
| 0x28000-2807F   | R/W        | 12          | Channel List RAM      |
| 0x28080-280FF   | R/W        | 16          | Threshold High RAM    |
| 0x28100-2817F   | R/W        | 16          | Threshold Low RAM     |

**Table 3.2: Memory Map**

**3.2.2 DATARAM**

Address: MEMspace + 0x000000

The DATARAM is a memory area of 65536 16-bit locations, mapped within the IP memory space.

**3.2.3 Channel List**

Address: MEMspace + 0x028000

The Channel List is a memory area of 64 12-bit locations, mapped within the IP memory space. It allows for the setup of calibration, gain and differential / single ended mode selection on a per channel basis.

| BIT 11           | BIT10         | BIT9           | BIT 8   | BIT 7-6 | BIT 5-0 |
|------------------|---------------|----------------|---------|---------|---------|
| EXT/INT BAND GAP | THRESHOLD LOW | THRESHOLD HIGH | SE/DIFF | Gain    | Channel |

**Channel**

Channel number from 0 to 47

**Gain Selection**

Input gains are selected on a per channel basis according to the following table.

| Gx_7 | Gx_6 | Gain Selected          |
|------|------|------------------------|
| 0    | 0    | The gain selected is 1 |
| 0    | 1    | The gain selected is 2 |
| 1    | 0    | The gain selected is 4 |
| 1    | 1    | The gain selected is 8 |

**Table 2.2.1: Gain Selection**

**SE/DIFF Single-Ended/Differential mode selection**

This bit selects whether the channels are in single ended or differential mode. If the bit is set to 0, then the channels are in single-ended mode and when the bits are set to 1 the channels are in differential mode.

**Threshold high**

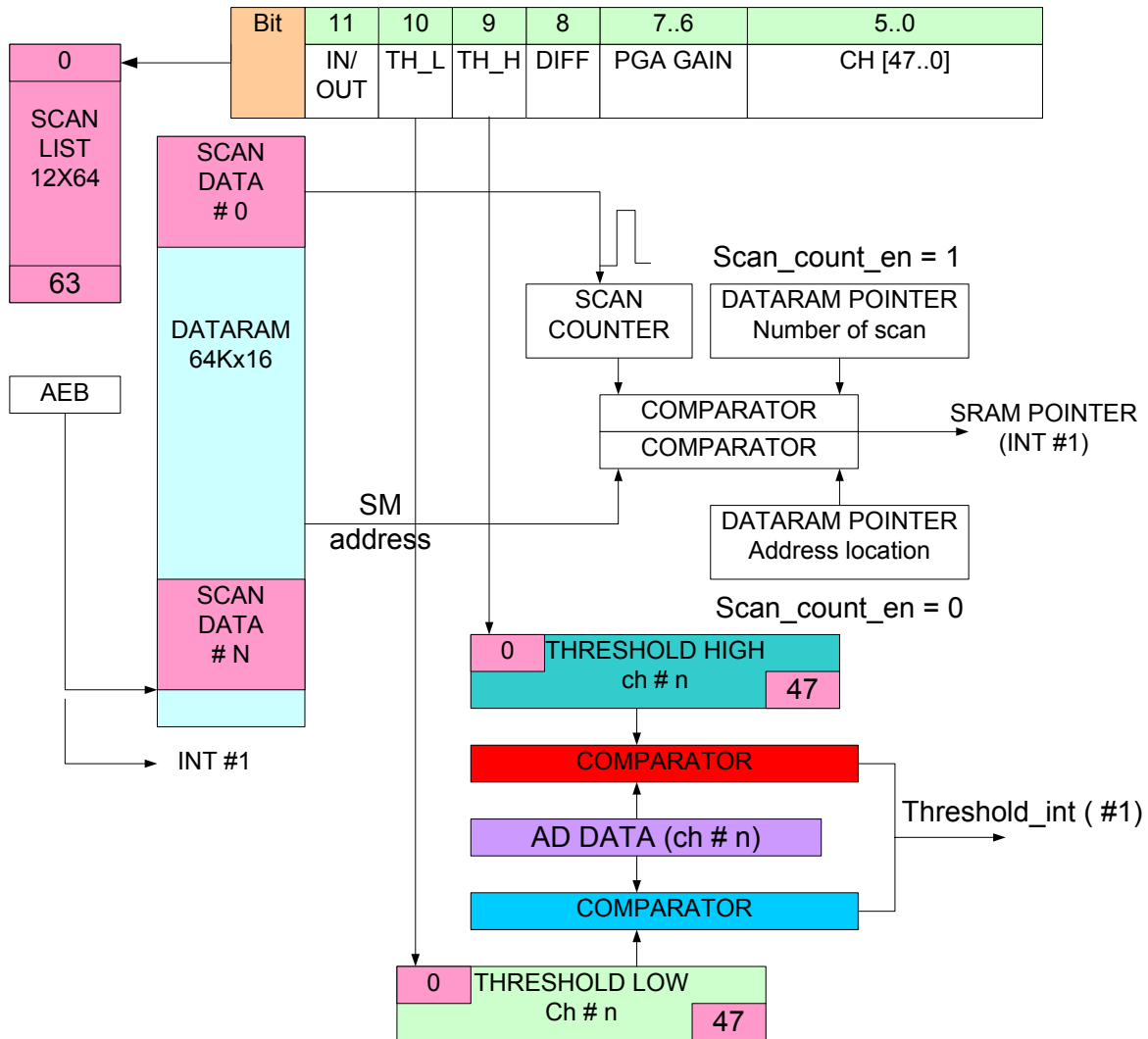
Allow interrupts in relation with the "Threshold High" value. See Table 2.2.2 for bit selection.

**Threshold low**

Allow interrupts in relation with the "Threshold High" value. See Table 2.2.2 for bit selection.

| Ext/Int | Thresh. high | Thresh. low | Interrupt  |
|---------|--------------|-------------|--|
| x       | 0            | 0           | No interrupt is selected                         |
| 0       | 0            | 1           | Selected when value is lower than Threshold Low  |
| 0       | 1            | 0           | Selected when value is lower than Threshold High |
| 0       | 1            | 1           | Selected when value is outside the range         |
| 1       | 0            | 1           | Selected when value is lower than Threshold High |
| 1       | 1            | 0           | Selected when value is lower than Threshold Low  |
| 1       | 1            | 1           | Selected when value is inside the range          |

Table 3.2.2: Threshold Selection



**Calibration source**

Calibration can be done by switching the two inputs of the differential amplifier to: GND OR +2.5V TO INPUT+ OR -2.5V TO Input, using pre-defined channels:

| Channel number (hex) | Input + PGA   | Input - PGA   |
|----------------------|---------------|---------------|
| 52 (0x34)            | GND           | GND           |
| 56 (0x38)            | VREF (+2.5 V) | GND           |
| 60 (0x3C)            | GND           | VREF (-2.5 V) |

Table 2.1.3.1: Calibration Sources

**End of List**

Selecting the channel number 63 (0x3F) in a location of the channel list signals to the state machine that the channel list is finished. Depending on other control bits, the state machine will either start over from the location 0 in the channel list, or stop.

| Channel number (hex) |                  |
|----------------------|------------------|
| 63 (0x3F)            | End channel list |

**3.2.4 Threshold High RAM**

*Address: MEMspace + 0x028080*

The Threshold High RAM is a memory area of 64 12-bit locations, mapped within the IP memory space. It is used for specifying a threshold high value used by the system to take specific actions, in relation with the Channel List. The position 0 of this table gives the value for the channel #0, and so on, until the position 47 corresponding to channel #47. The locations 48 to 63 are not used.

**3.2.5 Threshold Low RAM**

*Address: MEMspace + 0x028100*

The Threshold Low RAM is a memory area of 64 12-bit locations, mapped within the IP memory space. It is used for specifying a threshold high value used by the system to take specific actions, in relation with the Channel List. The position 0 of this table gives the value for the channel #0, and so on, until the position 47 corresponding to channel #47. The locations 48 to 63 are not used.

**3.3 IOSPACE**

**3.3.1 Address Map**

The registers are accessed in 16-bit mode. The addresses are as an offset to the IOspace base address.

| <b>Iospace +</b> | <b>R/W</b> | <b>Register</b>  |
|------------------|------------|--|
| 0x00             | R/W        | Internal Clock Divisor Low (bit 0-15)                          |
| 0x02             | R/W        | Internal Clock Divisor High (bit 16-23)                        |
|                  |            |  |
| 0x04             | R/W        | Scan delay counter   |
|                  |            |  |
| 0X06             | R          | State Machine Current Address Pointer                          |
|                  |            |  |
| 0X06             | W          | Reset Scan counter, Scan delay counter ,S.M. address generator |
| 0x08             | R/W        | Scan counter register(end memory address pointer)              |
| 0x0A             | R          | Scan_counter present position                                  |
|                  |            |  |
| 0X0C             | W          | Host Stop Acquisition  |
|                  |            |  |
| 0x0E             | R/W        | Acquisition Control register                                   |
|                  |            |  |
| 0x10             | R/W        | Trigger register   |
| 0x12             | W          | Host Start Acquisition pulse                                   |
|                  |            |  |
| 0x16             | R/W        | Digital Filter Register  |
|                  |            |  |
| 0x18             | R/W        | Channel Interrupt Register #0 (bit 0-15)                       |
| 0x1A             | R/W        | Channel Interrupt Register #1 (bit 16-31)                      |
| 0x1C             | R/W        | Channel Interrupt Register #2 (bit 32-47)                      |
|                  |            |  |
| 0x1E             | R          | Status register #1   |
|                  |            |  |
| 0x22             | W          | Source of interrupt #0 and # 1                                 |
| 0x24             | R          | A/D Register   |
| 0x26             | R/W        | Interrupt Vector Register # 0                                  |
| 0x28             | R/W        | Interrupt Vector Register # 1                                  |
| 0x2A             | W          | Reset interrupt #0   |
| 0x2C             | W          | Reset interrupt # 1  |

**Table 3.3 IO Registers**

### **3.3.2 Internal Clock Divisor (ICDH, ICDL)**

Addresses: *IOspace + 0x00* (ICDL)  
*IOspace + 0x02* (ICDH)

This 24-bit register serves as a divisor on the IP clock when Internal Sampling Clock is selected in the Acquisition Control Register.

#### **Program the Internal sample clock**

$$\text{minimum\_sampling\_Rate} = \frac{\text{IPClockFreq(in\_hertz)} * 1.3 * (N + 1)}{10^6(\text{in\_Seconds})}$$

$$\text{SamplingRate(in\_micro seconds)} = 1.3(\text{micro seconds}) * (N + 1)$$

Each channel is acquired in 1.3 μS.

For 48 channels sampling rate is every (48 + 1) \* 1.35 = 66 μS.

Clock divider will be: 32000000 / (1/66\*10<sup>-6</sup>) = 2112 ( \$840 Hex).

- \$00 - ICDL: Internal clock divisor low word, write 0x0840.
- \$02 - ICDH: Internal clock divisor high word, write 0x00.

For 4 channels sampling rate is every (4 + 1) \* 1.35 = 6.75 μS.

Clock divider will be : 32000000 / 1/6.75 10 E -6 = 216 ( \$D8 Hex).

- \$00 - ICDL: Internal clock divisor low word, write 0x00D8.
- \$02 - ICDH: Internal clock divisor high word, write 0x00.

$$\text{Sampling\_period(in\_seconds)} = 1 / 32(\text{Hz}) * (x(\text{decimal}) + 1)$$

Where x is the number that will be written into the clock divisor.

For a sampling period of 100us you would write 3199d because

$$.0001 * 32000000 = x + 1, x = 3200 - 1, x = 3199$$

### **3.3.3 Scan\_delay\_counter register**

Address: *IOspace + 0x04*

This 16 bit register provides the number of scans the State machine will acquire after receiving an external Event signal. When the count is reached a pulse is generated to stop the Acquisition.

### **3.3.4 State Machine Current Address Pointer**

Address: *IOspace + 0x06* (read)

This register contains the position of the DATARAM address currently written to by the State machine.

Address: *IOspace + 0x06* (write)



A host write will reset the Address Ram generator, the Scan\_counter and the Scan\_delay\_counter.

### **3.3.5 Scan\_counter register**

*Address: IOspace + 0x08*

This register contains the number of scans the state machine will go through before stopping or re-starting to zero. The address counter will be reset when the count is re-started. An interrupt can be issue. The Scan\_counter position can be read at address *IOspace + 0x0A*

### **3.3.6 Scan\_counter status**

*Address: IOspace + 0x0A*

The Scan\_counter position can be read at address *IOspace + 0x0A*

### **3.3.7 Scan\_counter status**

*Address: IOspace + 0x0A*

The Scan\_counter position can be read at address *IOspace + 0x0A*

### 3.3.8 Stop Acquisition Register

Address: *IOspace + 0x0C*

A write to this register will stop acquisition at the end of the current Channel List. The module will not do anymore acquisitions until a write to the Start Acquisition Register.

### 3.3.9 Acquisition Control Register

Address: *IOspace + 0x0E*

| Bits 7-5              | Bit 4          | Bit 3         | Bits 2-0              |
|-----------------------|----------------|---------------|-----------------------|
| Sampling Clock Source | Reserved = "0" | Continue scan | Trigger Enable Source |

| Bit 15   | Bits 14..12                  | Bits 11 | Bit 10                  | Bit 9     | Bit 8   |
|----------|------------------------------|---------|-------------------------|-----------|---------|
| Not used | Memory block size allocation | WARP    | Binary /~2's complement | BYTE_SWAP | IMPULSE |

This register allows configuring the acquisition state machine.

#### **Trigger Clock Source**

These 3 bits determine the signal used as a trigger to start the acquisition.

| Trigger Clock Source | Meaning  |
|----------------------|--|
| 000                  | Host Start Acquisition pulse (write) <i>IOspace + 0x12</i> |
| 001                  | External event pulse                                       |
| 010                  | Threshold int. A/D   |
| 011                  | IPStrobe   |
| 100                  | Internal clock Tclk0                                       |

#### **Continue scan**

When set to "1", acquisition will be done continuously. The S.M. will go through the Scan\_counter than start again. The address memory generator will also start at "0".

#### **Sampling Clock Source**

These 3 bits determine the signal used for the scan clock. This clock indicates when the next entry in the Channel List should be executed.

| Sampling Clock Source | Meaning  |
|-----------------------|--|
| 000                   | Host Start Acquisition pulse (write) <i>IOspace + 0x12</i> |
| 001                   | External event pulse                                       |
| 010                   | Threshold int. A/D   |
| 011                   | IPStrobe   |
| 100                   | Internal clock Tclk0                                       |

**WARP, IMPULSE**

These 2 bits are directly connected to the corresponding input of the A/D chip. They should both be left to “0”.

**Binary /~2’s complement**

This bit is directly connected to the corresponding input of the A/D chip. A “1” directs the A/D chip to output straight binary (0 is the smallest value, 0xffff is the largest). A “0” directs the chip to use 2’s complement (0x8000 is the smallest value, 0x7fff is the largest)

**BYTE\_SWAP**

When “0”, the LSB is output on D [7:0] and the MSB is output on D [15:8]. When “1”, the LSB is output on D [15:8] and the MSB is output on D [7:0].

**Memory block size allocation**

Programming of these three bits defines the size of the memory block allocated to each channel.

| BIT 14 | BIT 13 | BIT 12 | Block size(words) | Maximum channels |
|--------|--------|--------|-------------------|------------------|
| 0      | 0      | 0      | 400               | 48 up to 64      |
| 0      | 0      | 1      | 800               | 32               |
| 0      | 1      | 0      | 1000              | 16               |
| 0      | 1      | 1      | 2000              | 8                |
| 1      | 0      | 0      | 4000              | 4                |
| 1      | 0      | 1      | 8000              | 2                |

**3.3.10 Trigger Register**

Address: IOspace + 0x\$10

| BIT 7           | BIT 6               | BIT 5  | BIT 4         | BIT 3        | BIT 2    | BIT 1           | BIT 0            |
|-----------------|---------------------|--------|---------------|--------------|----------|-----------------|------------------|
| Threshold_ad_en | Event Enable output | Master | Event_stop_en | Scat_scan_en | Not_used | Post_trigger_en | Multiple_scan_en |

| Bit 15   | Bit 14    | Bit 13      | Bit 12         | Bit 11             | Bit 10        | Bit 9       | Bit 8       |
|----------|-----------|-------------|----------------|--------------------|---------------|-------------|-------------|
| Not used | Int_pulse | IPstrobe_en | Event_polarity | Event_threshold_en | Reserved =”0” | Intrequ1_en | Intrequ0_en |

All the bits are set to “0” upon Reset.

**Multiple scan enable**

When set to “0” (default) the State Machine goes through the scan list once then stops.

When set to “1” the State Machine will go through the scan list “n” times then stop. “n” is the number of scans loaded into the Scan counter register.

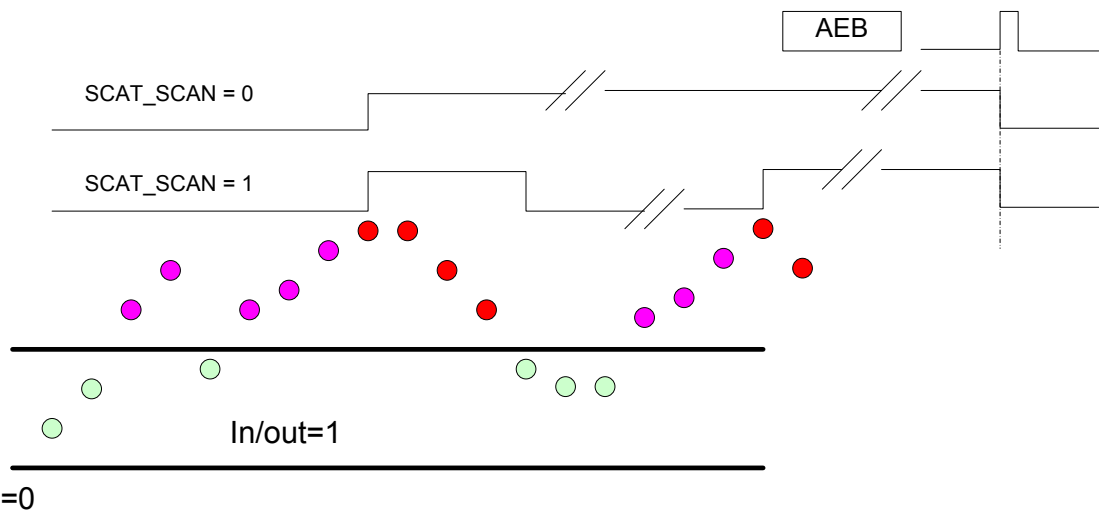
**Post trigger enable**

When set to “1” the State Machine will stop when the Scan\_delay\_counter has reached the number of scans loaded into it after receiving a trigger.

**Scat\_scan (nibble)**

When the THRESHOLD\_AD\_EN bit is set there are TWO (2) possible behaviors depending on the state of the SCAT\_SCAN bit:

- If “0”, the scan list is activated and acquisition stops only at the end of the Scan\_counter register.
- If “1”, the scan list is activated but stops when the condition that started the scan disappears.



*The example above is with a filter of 4 values*

**Event stop Enable**

When set to “1”, the input corresponding to the channel #47 is used as an external EVENT line.

**Master**

This bit, when set to 1, will make the IP module the source for the sample clock, the signal will be output on IP-STROBE signal on the IP bus. The MASTER bit allows the synchronization of multiple IP’s.

**Event Enable output**

When set to “1”, the input pin corresponding to the channel #47 is used as an external OUTPUT EVENT line for multiple boards.

Jumper J1 should be set between 2-3.

***Threshold\_ad\_en***

When set to “1”, it enables the acquisition to start /stop when a channel designated as threshold is going in range or out of range.

The Threshold Counter Register defines how many acquisitions have to satisfy the condition for the acquisition to really start.

***Intrequ0\_enable***

When set to “1”, the interrupt #0 is enabled.

***Intrequ1\_enable***

When set to “1”, the interrupt #0 is enabled.

***Event\_threshold\_en***

When set to “1”, it allows acquisitions if a channel designated as threshold is active.

The Threshold Counter Register defines how many acquisitions have to satisfy the condition for threshold to be active.

***Interrupt\_pulse***

When set to “1”, the Intrequ#0 and Intrequ#1 are not latched.

**3.3.11 Host Start Acquisition**

*Address: IOspace + 0x12*

A write to this write-only register will start acquisition immediately.

**3.3.12 Digital Filter Register**

*Address: IOspace + 0x16*

The 4 lower bits of this 8-bit register select the number of samples that must be in the threshold interrupt range before actually generating an interrupt. It acts as a digital filter

| BIT 7     | BIT 6     | BIT 5     | BIT 4     | BIT 3   | BIT 2   | BIT 1   | BIT 0   |
|-----------|-----------|-----------|-----------|---------|---------|---------|---------|
| Ad_trig_3 | Ad_trig_2 | Ad_trig_1 | Ad_trig_0 | Thres_3 | Thres_2 | Thres_1 | Thres_0 |

The higher 4 bits of this 8-bit register select the number of times the channel selected as AD trigger need to be in range before actually starting the acquisition.

**3.3.13 Channel Interrupt Register #0 [15~0]**

*Address: IOspace + 0x18*

This 16 bit register reflects the status of the interrupt generated by each channel (15~0) if activated for level threshold detection.

Each bit can be reset by writing a “1” to the corresponding bit. Writing a “0” does not change the state of the bit.

**3.3.14 Channel Interrupt Register #1 [31~16]**

*Address: IOspace + 0x1A*

This 16 bit register reflects the status of the interrupt generate by each channel (31~16) if activated for level threshold detection.

Each bit can be reset by writing a “1” to the corresponding bit. Writing a “0” does not change the state of the bit.

**3.3.15 Channel Interrupt Register #1 [47~32]**

*Address: IOspace + 0x1C*

This 16 bit register reflect the status of the interrupt generate by each channel (47~32) if activated for level threshold detection.

Each bit can be reset by writing a “1” to the corresponding bit. Writing a “0” does not change the state of the bit.

**3.3.16 Status register #1**

*Address: IOspace + 0x1E*

A read of the Status register # 1 at address *IOspace + 0x1E* will also reset the interrupt #0 line.

| BIT 3            | BIT 2            | BIT 1  | BIT 0      |
|------------------|------------------|--------|------------|
| Intreq# 1 status | Intreq# 0 status | BUSYIN | ACQUIRE_EN |

**ACQUIRE\_EN**

This signal enables the state machine and is set to “1” by the rising edge of the Start acquisition signal. Some of the reasons for reset are:

- IPRESET signal
- Stop acquisition signal command
- End pointer DATARAM
- End SCAN block

**BUSYIN**

This signal is “1” when the A/D converter is active. It is “0” after the conversion has finished

**INTREQ # 0 line**

This bit shows the state of the interrupt line # 0.

**INTREQ # 1 line**

This bit shows the state of the interrupt line # 1.

**3.3.17 Source Interrupt #0 and #1**

*Address: IOspace + 0x22*

| BIT 7                   | BIT 6                | BIT 5       | BIT 4             | BIT 3                      | BIT 2                | BIT 1        | BIT 0            |
|-------------------------|----------------------|-------------|-------------------|----------------------------|----------------------|--------------|------------------|
| Threshold interrupt A/D | External Event pulse | A/D trigger | Start acquisition | Thres hold interrupt pulse | External Event pulse | Sample pulse | Scan_cnt_pointer |

**Interrupt # 0**

Reset of the interrupt request #0 is made by:

- a write to the location *IOspace + 0x2A*
- *Read IVR#0 at address IOspace + \$26 using an Interrupt cycle with INTREQ#0 pending*
- *Read of the status register #1 at address IOspace + \$1E*

A read of the Status register # 1 at address *IOspace + 0x1E* will reset the interrupt #0 line.

**Interrupt # 1**

Reset of the interrupt request #1 is made by:

- a write to the location *IOspace + 0x2C*
- *Read IVR#1 at address IOspace + \$28 using an Interrupt cycle with INTREQ#1 pending*

**3.3.18 Direct A/D Read**

*Address: IOspace + 0x24*

This register contains the result of the latest A/D acquisition.

**3.3.19 Reset Interrupt Request # 1**

*Address: IOspace + 0x2C*

A write to this location will reset the interrupt request # 1.

### **3.3.20 Interrupt Vector Register # 0**

*Address: IOspace + 0x26*

This 8-bit Interrupt Vector Register can be programmed by the host. It will be output during an interrupt acknowledge IP INTESELA cycle.

### **3.3.21 Interrupt Vector Register # 1**

*Address: IOspace + 0x28*

This 8-bit Interrupt Vector Register can be programmed by the host. It will be output during an interrupt acknowledge IP INTESELA cycle.

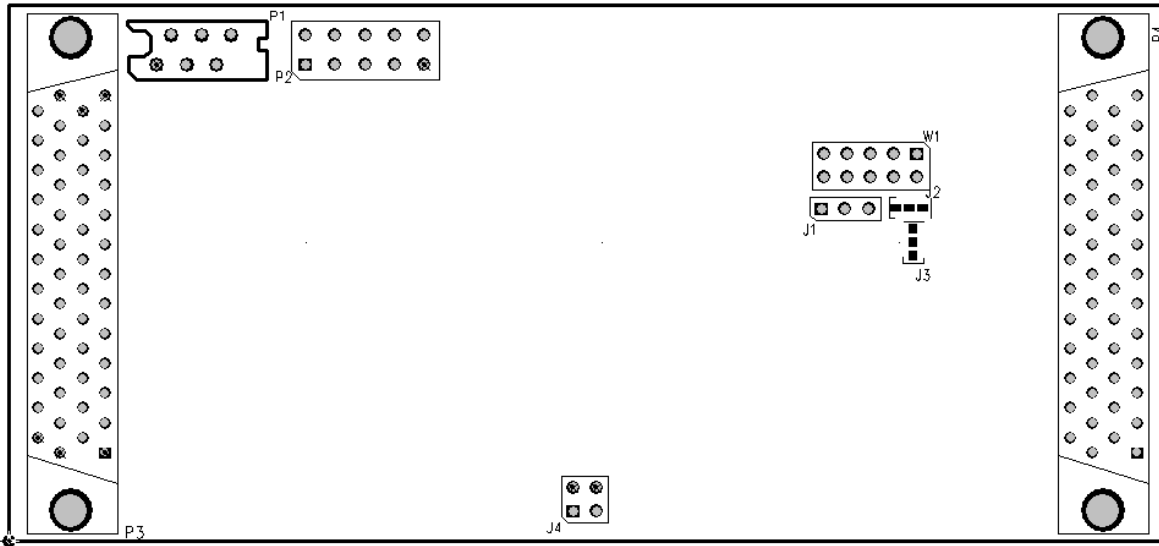
## **3.4 RESET**

All the local registers are cleared when the IP carrier issues a reset.



Connectors

The connector placement is depicted below. There are no configuration jumpers.



**Figure 3.1: Connector Locations**

**4. JUMPER DESCRIPTIONS**

| JUMPER | FACTORY SETTING                               | DESCRIPTION   |
|--------|---|---|
| P1     | Programming Header                            | Header for programming Cyclone EP1C12Q240.  |
| P2     | Factory Use                                   | Header used for debugging purpose.  |
| W1     | A/D Input settings ( see page 3 for settings) | The software programmable PGA allows selecting an input range of +/-10v, +/-5v, +/-2.5v, or +/-1.25v, based on a gain of 1, 2, 4, or 8, when the A/D is selected with a +/-10V range by jumper. |
| J1     | 1-2   | 1-2 sets IN-48 on I/O P2 pin 49 and 2-3 setup Ex-Event on pin 49  |
| J2     | 2-3   | Factory Use   |
| J3     | 1-2   | Factory Use   |
| J4     | 1-2 3-4                                       | MSEL0 and MSEL1 for programming Cyclone EP1C12Q240.   |

**Table 4.1 Jumper Descriptions**

**4.1 CONNECTOR DESCRIPTIONS**

***IP External I/O Connector (P4)***

A 50 pin subminiature D shelled connector is used to route the analog signals to the IP. The IP carrier then takes these signals and presents them for customer use. See the documentation for the IP carrier for more details.

The signals are routed as follows.

| Pin | Connection |  | Pin | Connection |
|-----|------------|--|-----|------------|
| 1   | IN00/IN00+ |  | 26  | IN24/IN00- |
| 2   | IN01/IN01+ |  | 27  | IN25/IN01- |
| 3   | IN02/IN02+ |  | 28  | IN26/IN02- |
| 4   | IN03/IN03+ |  | 29  | IN27/IN03- |
| 5   | IN04/IN04+ |  | 30  | IN28/IN04- |
| 6   | IN05/IN05+ |  | 31  | IN29/IN05- |
| 7   | IN06/IN06+ |  | 32  | IN30/IN06- |
| 8   | IN07/IN07+ |  | 33  | IN31/IN07- |
| 9   | IN08/IN08+ |  | 34  | IN32/IN08- |
| 10  | IN09/IN09+ |  | 35  | IN33/IN09- |
| 11  | IN10/IN10+ |  | 36  | IN34/IN10- |
| 12  | IN11/IN11+ |  | 37  | IN35/IN11- |
| 13  | IN12/IN12+ |  | 38  | IN36/IN12- |
| 14  | IN13/IN13+ |  | 39  | IN37/IN13- |
| 15  | IN14/IN14+ |  | 40  | IN38/IN14- |
| 16  | IN15/IN15+ |  | 41  | IN39/IN15- |
| 17  | IN16/IN16+ |  | 42  | IN40/IN16- |
| 18  | IN17/IN17+ |  | 43  | IN41/IN17- |
| 19  | IN18/IN18+ |  | 44  | IN42/IN18- |
| 20  | IN19/IN19+ |  | 45  | IN43/IN19- |
| 21  | IN20/IN20+ |  | 46  | IN44/IN20- |
| 22  | IN21/IN21+ |  | 47  | IN45/IN21- |
| 23  | IN22/IN22+ |  | 48  | IN46/IN22- |
| 24  | IN23/IN23+ |  | 49  | IN47/IN23- |
| 25  | GND        |  | 50  | GND        |

**Table 4.2: IP External I/O Connector (P4)**

## 5. APPLICATION EXAMPLE

### 5.1 HOW TO SET A CHANNEL AS AD TRIGGER.

1-Write selected channel number at location zero of the scan-list ram

2-Enable the desired threshold

3-Program the threshold level into the two-threshold ram

4-Program the threshold AD counter to the desired count before the threshold AD signal is generated.

5-Select the trigger source as the Threshold ad signal

6-Select a continuous scan when threshold is set once or a scattered scan when the threshold is active.

7- Enable conversion by writing at address Start conversion.

The state machine will continuously convert the selected channel until a threshold\_ad signal is generated.

Then the SM will continue through the scan list.

8-A/D conversion result is available at address zero of the DATARAM.

### 5.2 SINGLE CHANNEL CONVERSION CONTROLLED BY HOST

1-Write selected channel number at location zero of the scan-list ram

2-Write at next location channel number \$ FF. The SM will recognize it as the end of the scan list.

5-Select the trigger source as the Host Start conversion

7- Enable conversion by writing at address Start conversion.

The state machine will convert the selected channel once.

8-A/D conversion result is available at address zero of the DATARAM.

### 5.3 SCAN LIST CONVERTED ONCE CONTROLLED BY HOST OR EXTERNAL TRIGGER

Same as above but generate a scan-list with at the end channel \$3F

Post trigger ad48th

### 5.4 POST TRIGGER ACQUISITION WITH EVENT SIGNAL

Acquisition is made continuously.

