VDSPSCM

HIGH PERFORMANCE
DIGITAL SERVO CONTROL MODULE
4 CHANNEL CARRIER

REFERENCE MANUAL

730-17-001-4000

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ALPHI TECHNOLOGY CORPORATION
6202 S. Maple Avenue #120
Tempe, AZ 85283 USA
Tel : (602) 838-2428
Fax: (602) 838-4477

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1. GENERAL DESCRIPTION

The VDSPSCM module is part of the VDSP control system. The VDSPSCM is normally connected to a VDSP431 control module via the VMEbus P2 connector. Up to 3 VDSPSCM modules can be connected to a single VDSP431 control module. This yields up to six channels of control capability.

1.1 VDSPSCM Description

The VDSPSCM module is a servant carrier that is populated with :

- Two Strain Gauge/Bridge channels
- Two LVDT channels
- Two Valve driver channels
- Four A/D converters to digitize DC and AC parameters
- Up to 20 Digital I/O channels
- Four channel D/A monitors
- Two A/D channels for monitoring valve and excitation current
- Calibration resistance for software controlled “shunt calibration”
- DC/DC converter for the analog circuitry.

1.2 VDSPSCM Base Addresses

Each VDSPSCM occupies 256 TMS320C31 locations. Local DSP access is made in 32-bit mode. However, only the lower 16 bits are used . Up to three (3) VDSPSCM modules can be connected together using a VSB overlay on the VMEbus P2 connector. Each VSB is identified by a set of three jumpers located on the back of each VSB Overlay. Slot “0” is normally reserved for the VSB controller, which in this case, is the VDPS431M module. Using this identification, every VDSPSCM module recognizes its own location and will respond to the address placed on the P2 connector.

Address decoding by the VDSPSCM is made by comparing the SLOT location identified with GA0-GA3 with the P2 address VSAD10 to VSAD12 which corresponds to address lines LA08 to LA10 for the DSP. In Addition, two other jumpers compare the type of P2 transfer (I/O space ,System space or Alternate space), driven by the lines SPACE0 and SPACE1 on P2. These jumper settings are shown below:

W3 jumper	Description
none	System space Factory setting
3-4	I/O space
1-2	Alternate space

1.3 SCAN CLOCK

The VDSP_SCM can receive the SCANCLK for the A/D converter through two sources.
Jumper W2 determines the source.

W2	SOURCE SCAN CLOCK
3-4	P2 line Pin C31 (VBUSY*) Factory setting
1-2	P1 line Pin B21 (Serclk)

Note: Selecting W2 pins 1-2 enables Serclk. The VDSP431 modules use this reserved VMEbus line. This may be incompatable with other manufacturers' VMEbus modules. Currently, we are not aware of any VMEbus modules that make use of Serclk.

1.4 OTHER JUMPERS

Jumpers W1, W4 and P3 are factory installed and should not be changed.
They are documented here for completeness.

Jumpers	Description
W1	Input voltage source for the DC/DC converter Factory set 1-2 Input +5v
W4	Enable programming of the MACH 445
P3	Pod for MACH445 programming

1.5 Front Panel LEDS

Front panel LED's provide information as to the status of the VDSPSCM module:

LED's	Description	LED "ON"	LED "OFF"
L1	+5 V Power supply	+5V OK	5V Fail
L2	+ 12V Power supply	+12V OK	+12V Fail
L3	- 12V Power supply	-12V OK	-12V Fail
L4	+ 15V DC/DC converter	+15V OK	+15V Fail
L5	- 15V DC/DC converter	-15V OK	-15V Fail
L6	VDSP_SCAN module is accessed	Module Active	Module InActive
L7	SCANCLK Active	Scan Active	Scan InActive
CAL1	Calibration Relay #1	Relay Closed	Relay Open
CAL2	Calibration Relay #2	Relay Closed	Relay Open
CAL3	Calibration Relay #3	Relay Closed	Relay Open
CAL4	Calibration Relay #4	Relay Closed	Relay Open

1.6 Calibration Resistors

This resistance can be connected externally to any of the arm of the Bridge or Load Cell. The resistance is switched 'On' by a software controlled relay. At reset, all of the relay contacts are open. Calibration resistance values are typically 87.6KΩ .1% and located on a socket. Users that wish to use another calibration resistance value can short the internal resistance using the internal switch SW1. The new resistance will have to be connected externally. Refer to the table below for switch settings:

SW1	OFF	ON
1-2	CALD = 87.6K	CALD = SHORTED
3-4	CALC = 87.6K	CALC = SHORTED
5-6	CALB = 87.6K	CALB = SHORTED
7-8	CALA = 87.6K	CALA = SHORTED

1.7 DIGITAL Inputs

An 8536 device is used to provide up to 20 digital TTL Inputs / Outputs available on a subminiature 25 Pin connector. Two groups of 8 channels can be selected for input or output by jumper. They correspond to Ports A and B of the 8536. Refer to the table below for port direction settings:

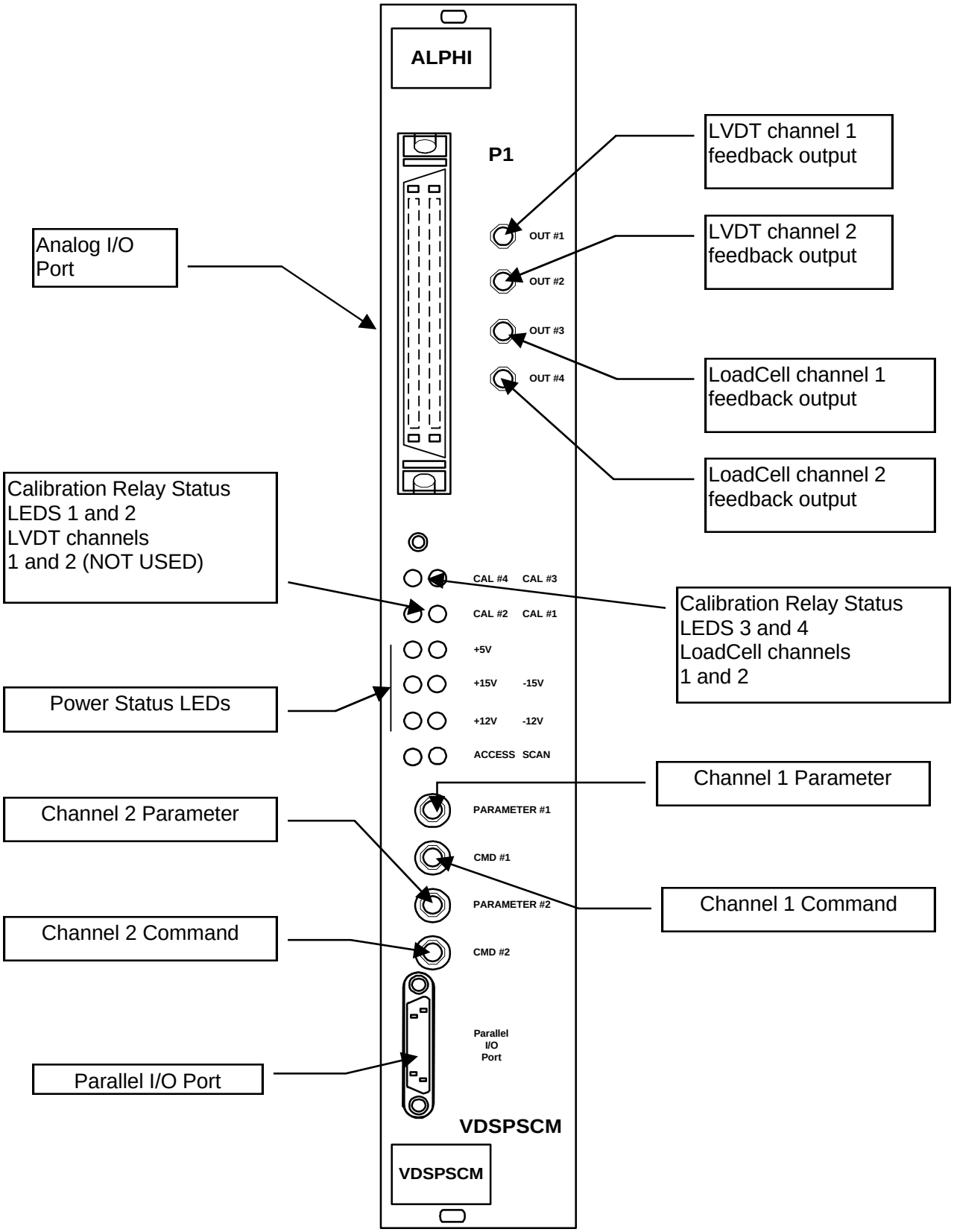
W5	NONE	INSTALLED
1-2	PA00-PA07 OUTPUT	PA00-PA07 INPUT
3-4	PB00-PB07 OUTPUT	PB00-PB07 INPUT

The four remaining channels, (Port C), can be selected separately as input or output by the following set of jumpers:

W6	**PC0**	**W6**	**PC0**
1-3 2-4	INPUT	1-2 3-4	OUTPUT
W6	**PC1**	**W6**	**PC1**
5-7 6-8	INPUT	5-6 7-8	OUTPUT
W6	**PC2**	**W6**	**PC2**
9-11 10-12	INPUT	9-10 11-12	OUTPUT
W6	**PC3**	**W6**	**PC3**
13-15 14-16	INPUT	13-14 15-16	OUTPUT

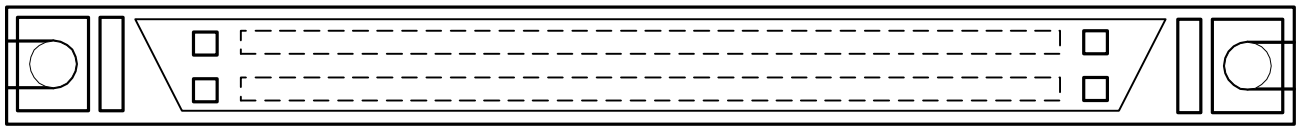
For more information about how to program the 8536, please refer to the manufacturers' data sheet.

1.8 Front Panel



1.9 ANALOG I/O CONNECTOR

Pin 40 Pin 1

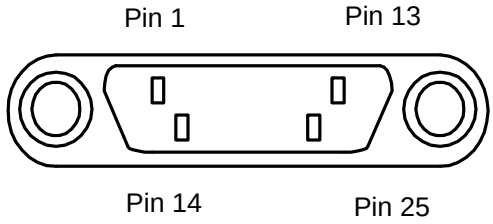


Pin 80 Pin 41

		P1		
Pin 1	I/O PC2		Pin 41	I/O PC3
Pin 2	I/O PC0		Pin 42	I/O PC1
Pin 3	GND		Pin 43	GND
Pin 4	Not Used		Pin 44	Not Used
Pin 5	CALA_I		Pin 45	CALA_O
Pin 6	EXSA+		Pin 46	EXSA-
Pin 7	EXA+		Pin 47	EXA-
Pin 8	GNDA		Pin 48	
Pin 9	CALB_I		Pin 49	CALB_O
Pin 10	EXSB+		Pin 50	EXSB-
Pin 11	EXB+		Pin 51	EXB-
Pin 12	GNDA		Pin 52	
Pin 13	CALC_I		Pin 53	CALC_O
Pin 14	EXSC+		Pin 54	EXSC-
Pin 15	EXC+		Pin 55	EXC-
Pin 16	GNDA		Pin 56	
Pin 17	CALD_I		Pin 57	CALD_O
Pin 18	EXSD+		Pin 58	EXSD-
Pin 19	EXD+		Pin 59	EXD-
Pin 20	GNDA		Pin 60	
Pin 21	GNDA		Pin 61	GNDA
Pin 22	OUTMON#2		Pin 62	OUTMON#4
Pin 23	OUTMON#1		Pin 63	OUTMON#3
Pin 24	GNDA		Pin 64	GNDA
Pin 25	PGOUTSC		Pin 65	PGOUTSD
Pin 26	PGOUTSA		Pin 66	PGOUTSB
Pin 27	VALVED+		Pin 67	VALVED-
Pin 28	GND_VDC		Pin 68	GND_VDD
Pin 29	VALVEC+		Pin 69	VALVEC-
Pin 30	VALVEB+		Pin 70	VALVEB-
Pin 31	GND_VDA		Pin 71	GND_VDB
Pin 32	VALVEA+		Pin 72	VALVEA-
Pin 33	GUARDD		Pin 73	GNDA
Pin 34	IND+		Pin 74	IND-
Pin 35	GUARDC		Pin 75	GNDA
Pin 36	INC+		Pin 76	INC-
Pin 37	GUARDB		Pin 77	GNDA
Pin 38	INB+		Pin 78	INB-
Pin 39	GUARDA		Pin 79	GNDA
Pin 40	INA+		Pin 80	INA-

1.10 PARALLEL I/O CONNECTOR

The Parallel I/O Port utilizes a 25 Pin Subminiature female connector



	PIN		PIN		PIN
Pin 1	PA07	Pin 10	PB00	Pin 19	PB07
Pin 2	PA05	Pin 11	Not used	Pin 20	PB05
Pin 3	PA03	Pin 12	FP_PC2	Pin 21	PB03
Pin 4	PA01	Pin 13	FP_PC0	Pin 22	PB01
Pin 5	GND	Pin 14	PA06	Pin 23	GND
Pin 6	GND	Pin 15	PA04	Pin 24	FP_PC3
Pin 7	PB06	Pin 16	PA02	Pin 25	FP_PC1
Pin 8	PB04	Pin 17	PA00		
Pin 9	PB02	Pin 18	Not used		

2. VDSP431 Memory Mapped Registers

The SCM registers are documented in the table below. The addresses are from the DSP point of view. The information provided in this section is intended to be used as a reference guide for developing VDSP431 firmware.

P2 Address Offset	Register Name	Description	R/W
$00-$0F	PGA1	DC or AC module installed in channel 1	W
$10-$1F	PGA2	DC or AC module installed in channel 2	W
$20-$2F	PGA3	DC or AC module installed in channel 3	W
$30-$3F	PGA4	DC or AC module installed in channel 4	W
$40-$4F	VD1	Valve Driver for Channel 1	W
$50-$5F	VD2	Valve Driver for Channel 2	W
$60-$6F	VD3	Valve Driver for Channel 3	W
$70-$7F	VD4	Valve Driver for Channel 4	W
$80	OE 1	A/D Data conversion result channel 1	R
$81	OE 2	A/D Data conversion result channel 2	R
$82	OE 3	A/D Data conversion result channel 3	R
$83	OE 4	A/D Data conversion result channel 4	R
$84	OE 5	A/D Data conversion result channel 5	R
$86	CSMUXA	Multiplexer for analog parameters monitoring	W
$87	CSMUXB	Multiplexer for digitized parameters monitoring	W
$88	CS_CAL	Calibration Relay	W
$89	CS_STAT	Status Register SCM	R
$8A	CS_RSTDA	A write reset the D/A converter	W
$90	CS_MON1	D/A Monitor Output #1	W
$94	CS_MON2	D/A Monitor Output #2	W
$98	CS_MON3	D/A Monitor Output #3	W
$9C	CS_MON4	D/A Monitor Output #4	W
$A0-$A3	CS_8536	Parallel Digital I/O port	R/W

2.1 ANALOG MONITORING PARAMETERS

Base address = Slot + $86

The VDSPSCM can monitor two different analog signals at the Front Panel level. The signals are multiplexed before being buffered. There are two multiplexers, each of them uses the 3 lower bits of 4-bit field. Bits #3 and #7 are not used. Bits # 0-2 control analog channel #1 and Bits # 4-6 control analog channel #2. For example, if you want to monitor Excitation voltage from channel #3 and Excitation current from channel #2 you have to write the value $03. It is possible, at the level of the VDSPSCM module, to select either the PGAOUTx signal or the D/A OUTx signal. The jumpers below determine this selection.

W10	**Signal**	**W11**	**Signal**
1-2	PGAOUTA	1-2	PGAOUTB
2-3	OUTMON1	2-3	OUTMON2
W8	**Signal**	**W9**	**Signal**
1-2	PGAOUTC	1-2	PGAOUTD
2-3	OUTMON3	2-3	OUTMON4

DATA BITS #0-2 BITS #4-6	ANALOG CHANNEL	PARAMETER SELECTED
0X	Analog #1	Excitation current from channel #1
1X	Analog #1	Excitation voltage from channel #1
2X	Analog #1	Valve current from channel #1
3X	Analog #1	Excitation current from channel #3
4X	Analog #1	Excitation voltage from channel #3
5X	Analog #1	Valve current from channel #3
6X	Analog #1	Output from D/A monitor #1 or PGAOUTA
7X	Analog #1	Output from D/A monitor #2 or PGAOUTB
X0	Analog #2	Excitation current from channel #2
X1	Analog #2	Excitation voltage from channel #2
X2	Analog #2	Valve current from channel #2
X3	Analog #2	Excitation current from channel #4
X4	Analog #2	Excitation voltage from channel #4
X5	Analog #2	Valve current from channel #4
X6	Analog #2	Output from D/A monitor #3 or PGAOUTC
X7	Analog #2	Output from D/A monitor #4 or PGAOUTD

2.2 DIGITAL MONITORING PARAMETERS

Base address = Slot + $87

The VDSPSCM can monitor analog signals by digitizing them. The DSP is able to monitor the health of these signals. For example, excitation and valve current can be monitored to determine short or open conditions. A 16 bit A/D converter is fed by the output of two multiplexers. There are two multiplexers, each of them use the 3 lower bits of a 4-bit group. Bit #3 enables multiplexer 1 and Bit #7 enables multiplexer 2.

DATA Bit #0-7	PARAMETER SELECTED
08h	Excitation current from channel #1
09h	Excitation current from channel #2
0Ah	Excitation voltage from channel #1
0Bh	Excitation voltage from channel #2
0Ch	Valve current from channel #1
0Dh	Valve current from channel #2
0Eh	Not Used
0Fh	Not Used
80h	Excitation current from channel #3
90h	Excitation current from channel #4
A0h	Excitation voltage from channel #3
B0h	Excitation voltage from channel #4
C0h	Valve current from channel #3
D0h	Valve current from channel #4
E0h	Not Used
F0h	Not Used

2.3 SIGNAL CONDITIONING MODULES

The VDSP31 is available with two different signal conditioning modules

- LoadCell signal conditioning
- LVDT signal conditioning

2.3.1 DC Signal Conditioning

2.3.1.1 Programmable Instrumentation Amplifier

Incoming low level LoadCell signals are amplified by high precision low noise, low offset, high impedance instrumentation amplifier. The SCM PGA Modules utilize a two stage instrumentation amplifier design that is able to provide any gain between 1 and 5000.

- First stage **G = 1 , 100,125,200,333**
- Second stage **G = 1, 2, 4, 8,16**

A 12-bit multiplying D/A is used to provide attenuation bewteen the two gain stages allowing a fine adjustment of the desired gain. The fixed gain ranges of the SCM PGA Module are as follows:

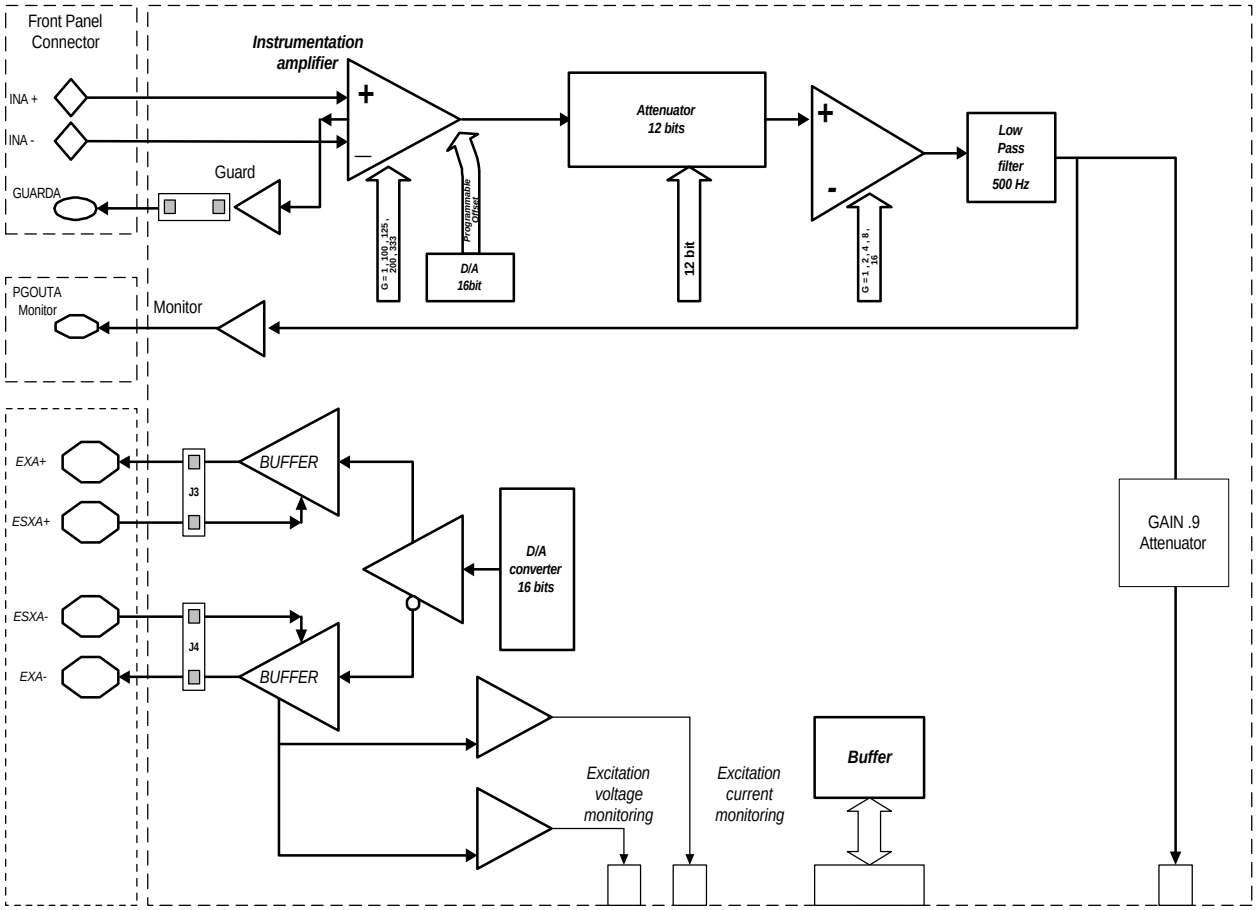
1	**100**	**125**	**200**	**333**
2	200	250	400	666
4	400	500	800	1332
8	800	1000	1600	2664
16	1600	2000	3200	5328

PGA fixed gain ranges

The output offset has a +/- 10v programmable range using a 16 bit D/A converter. The high-level amplified PGA signals go to a high precision Analog to Digital converter. All PGA output signals are converted synchronously. The PGA module outputs can be monitored at the Front Panel level. There is an attenuator with a gain of .9 in front of the A/D convertor. The effective A/D input range is therefore +/- 11 volts. This allows the A/D to detect and properly handle overange transducer inputs. Unity gain buffer amplifiers drive the signals to a SMC connectors located on the front panel.

The Common Mode voltage retrieved at the output of the first stage of the PGA can be driven back to the Input connector forming a driven guard.

The driven guard is enabled by installing jumper J1 on the PGA module.



DC Module Block Diagram

2.3.1.2 PGA ADDRESS REGISTER MAP

Each PGA module occupies 16 address locations. The table below describes the PGA registers :

Address Offset	Name	Description	Bits Used	R/W
$00	PGA_OFFSET	Controls the 16-bit D/A that provides a +/- 10 v output offset on the first stage	16	W
$01	GAIN_SET	First stage amplifier gain bits	8	W
$02	ATTN	Controls a 12-bit Attenuator for fine gain adjustment	12	W
$03	GAIN_AMP_2	Second stage amplifier gain bits	3	W
$04	EXCITATION	Controls the 16-bit D/A that provides +/ 10 v excitation voltage	16	W

PGA Address Map

2.3.1.3 PGA_OFFSET

The output stage return of the first differential amplifier is connected to an operational amplifier driven by a 16 bit D/A converter. A resistive divider routes up to 99 % of the D/As voltage output to the return pin of the Instrumentation amplifier. The D/A format is two's complement:

Writing $8000 to this register generates -9.9 v of offset
Writing $0000 to this register generates 0.0 v of offset
Writing $7FFF to this register generates + 9.9 v of offset

2.3.1.4 GAIN_SET

Each bit in this register enables an open drain VMOS device that drives a relay.
The table below defines register values and associated gains:

GAIN	REG DATA	GAIN	REG DATA	GAIN	REG DATA	GAIN	REG DATA	GAIN	REG DATA
1	0x00	100	0x01	125	0x05	200	0x02	333	0x06
2	0x08	200	0x09	250	0x0D	400	0x0A	666	0x0E
4	0x10	400	0x11	500	0x15	800	0x12	1332	0x16
8	0x18	800	0x19	1000	0x1D	1600	0x1A	2664	0x1E
16	0x38	1600	0x39	2000	0x3D	3200	0x3A	5328	0x3E

PGA Gain Selection

NOTE : FOR IMPROVED SIGNAL TO NOISE RATIO IT IS BETTER TO HAVE THE MAXIMUM GAIN ON THE FIRST STAGE.

2.3.1.5 GAIN_AMP_2

A write to this address latches the current gain value contained in the GAIN_SET register into the second amplifier stage.

2.3.1.6 ATTENUATION

The output of the first amplifier stage is attenuated using a multipying 12-bit D/A converter. The amount of attenuation is:

Vout = -Vin/ D where D = 0 to 4095/4096

Writing a value of 0x0FFF selects minimum attenuation.
Writing a vaue of 0x0000 selects maximum attenuation.

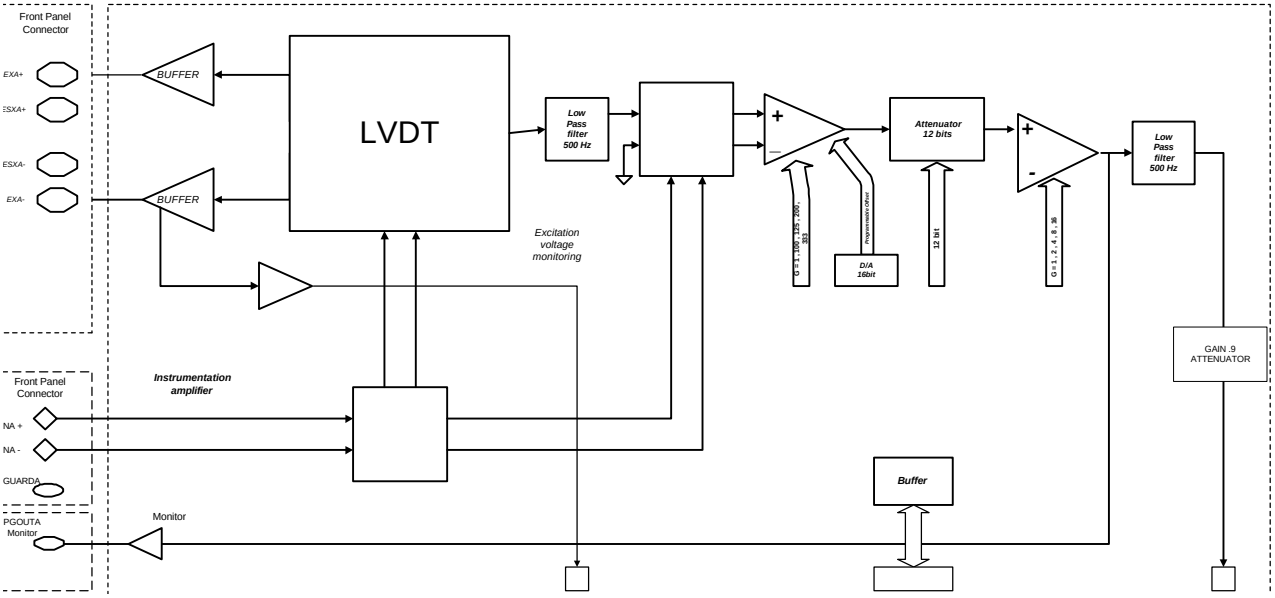
2.3.1.7 DC EXCITATION

The PGA module containes a differential voltage power amplifier that is controlled digitally by a 16-bit D/A. The output voltage is proportional to the D/A output voltage. A +5v D/A output is translated in a 10 V peak-peak excitation voltage. The maximum output is 18v peak to peak into a 100Ω load. Remote sense lines can be incorporated to compensate for voltage drops due to long wire lengths. The return path can be connected at the level of the PGA module (**J3, J4**) or externally at the bridge. The table below documents the Remote Sense jumper configuration:

PGA Channel	Remote Sense Disable J3 , J4	Remote Sense Enable J3 , J4
Excitation A	1-2, 3-4	none
Excitation B	1-2, 3-4	none
Excitation C	1-2, 3-4	none
Excitation D	1-2, 3-4	none

Remote Sense Jumper Settings

2.3.2 AC Signal Conditioning



AC Module Block Diagram

The AC module is designed around the AD698 LVDT signal conditioner from Analog Devices. The excitation frequency can be set between 20 Hz and 20 KHz by changing capacitors. The VDSP431 AC Module is preset to 10 KHz at the factory. The output of the LVDT demodulator is amplified by the same circuitry utilized by the DC Module. Programmable relays allow the LVDT demodulator to be bypassed. This is so the AC Module can be used to support DC high-level inputs such as a DCDT. The AC excitation can be disabled when DC high-level mode is used. Two fourth order filters, with a cut-off frequency of 500 HZ, remove any residual carrier signal from the demodulator output.

2.3.2.1 AC EXCITATION

The LVDT modules excitation is preset at the factory to 7.0 Vpp at 10.0 KHZ.
The demodulator gain is set to output +/- 9 Vdc over full stroke of the LVDT.

2.3.2.2 LVDT ADDRESS REGISTER MAP

Each AC module occupies 16 address locations. The table below describes the LVDT registers :

Address Offset	Name	Description	Bits Used	R/W
$00	LVDT_OFFSET	Controls the 16-bit D/A that provides a +/- 10 v output offset on the first stage	16	W
$01	GAIN_SET	Bits 0-6 First stage amplifier gain bits Bit 7 selects LVDT or DC High-Level Mode Bit 8 disables the LVDT power supply to reduce noise	8	W
$02	ATTN	Controls a 12-bit Attenuator for fine gain adjustment	12	W
$03	GAIN_AMP_2	Second stage amplifier gain bits	3	W
$04	EXCITATION	Controls the 16-bit D/A that provides +/ 10 v excitation voltage	16	W
$05	SEC_LVDT	Prog- amp for secondary LVDT signal	2	W

LVDT Address Map

2.3.2.3 LVDT_OFFSET

The output stage return of the first differential amplifier is connected to an operational amplifier driven by a 16 bit D/A converter. A resistive divider routes up to 99 % of the D/As voltage output to the return pin of the Instrumentation amplifier. The D/A format is two's complement:

Writing $8000 to this register generates -9.9 v of offset
Writing $0000 to this register generates 0.0 v of offset
Writing $7FFF to this register generates + 9.9 v of offset

2.3.2.4 LVDT AMPLIFIER GAIN_SET

Each bit in this register enables an open drain VMOS device that drives a relay.
Bits 0-5 determine the LVDT gain as defined in the table below:

GAIN	REG DATA	GAIN	REG DATA	GAIN	REG DATA	GAIN	REG DATA	GAIN	REG DATA
1	0x00	100	0x01	125	0x05	200	0x02	333	0x06
2	0x08	200	0x09	250	0x0D	400	0x0A	666	0x0E
4	0x10	400	0x11	500	0x15	800	0x12	1332	0x16
8	0x18	800	0x19	1000	0x1D	1600	0x1A	2664	0x1E
16	0x38	1600	0x39	2000	0x3D	3200	0x3A	5328	0x3E

LVDT Gain Selection

NOTE : FOR IMPROVED SIGNAL TO NOISE RATIO IT IS BETTER TO HAVE THE MAXIMUM GAIN ON THE FIRST STAGE.

Bits 6-7 control additional AC module settings:

BIT	"0"	"1"
6	Select AC/LVDT Mode	Select DC High-Level Mode
7	Enable LVDT Excitation	Disable LVDT Excitation

2.3.2.5 GAIN_AMP_2

A write to this address latches the current gain value contained in the GAIN_SET register into the second amplifier stage.

2.3.2.6 ATTENUATION

The output of the first amplifier stage is attenuated using a multipying 12-bit D/A converter. The amount of attenuation is:

Vout = -Vin/ D where D = 0 to 4095/4096

Writing a value of 0x0FFF selects minimum attenuation.
Writing a vaue of 0x0000 selects maximum attenuation.

2.3.3 VALVE DRIVER

The Valve driver module is able to drive up to 100 ma into a 200Ω load. The output of a 16-bit D/A converter drives two power amplifiers that convert the input voltage signal to a current signal. Output of the current is directly proportional to the input signal. The current range is programmable by software using relays.

Four ranges are available :

- 12.5 ma
- 25.0 ma
- 50.0 ma
- 100.0 ma

Current selected is calculated with an input voltage of 5 V.
Overdrive can be up to 100 %.

The actual current delivered to the valve can be monitored by the DSP. A differential amplifier converts the output current to a voltage signal directly proportional to the current flow into the load.

2.3.3.1 VALVE DRIVER ADDRESS REGISTER MAP

Address Register	Name	Description	bits used	R/W
$00	Valve Drive	16-bit D/A that provides a +/- 10 v reference to the current converters.	16	W
$01	Current Range	3 bits are used to select the full scale current range	3	W

Bit activated	Current selected
none	12.5 mA
0	25 mA
1	50 mA
2	100 mA

2.3.3.2 VALVE DRIVER BLOCK DIAGRAM

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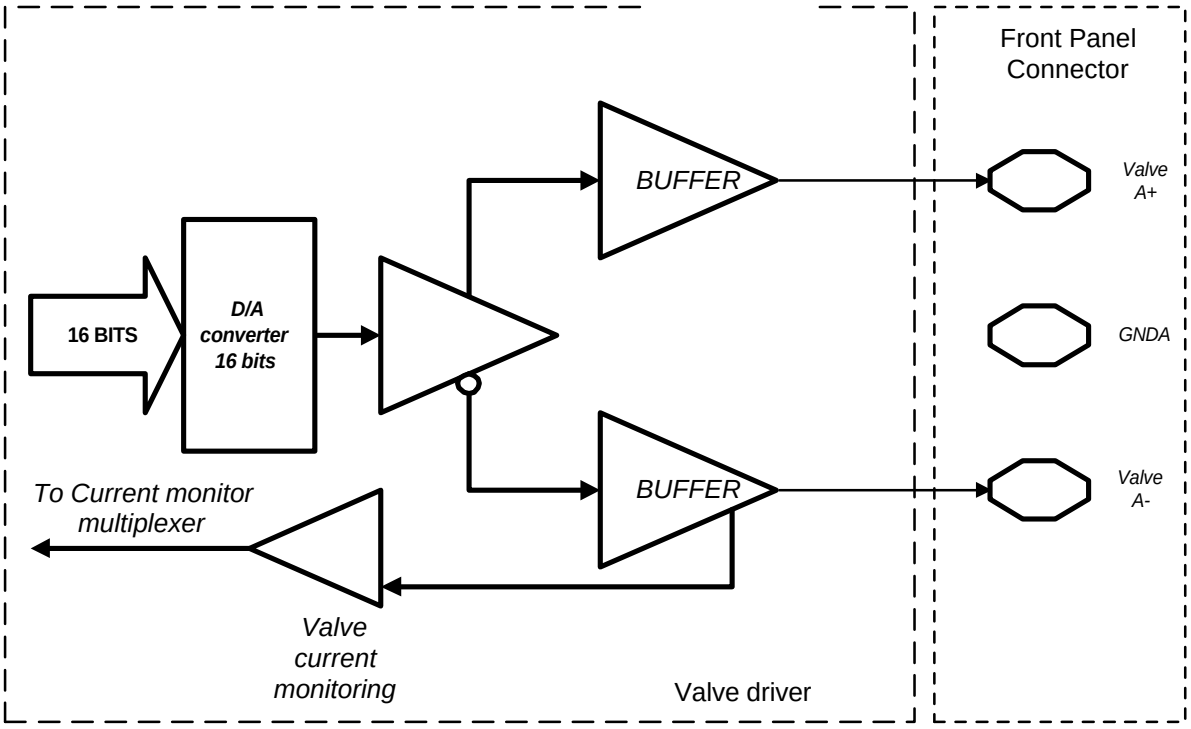

VALVE Module Block Diagram

2.3.4 TYPICAL LOADCELL CONNECTION

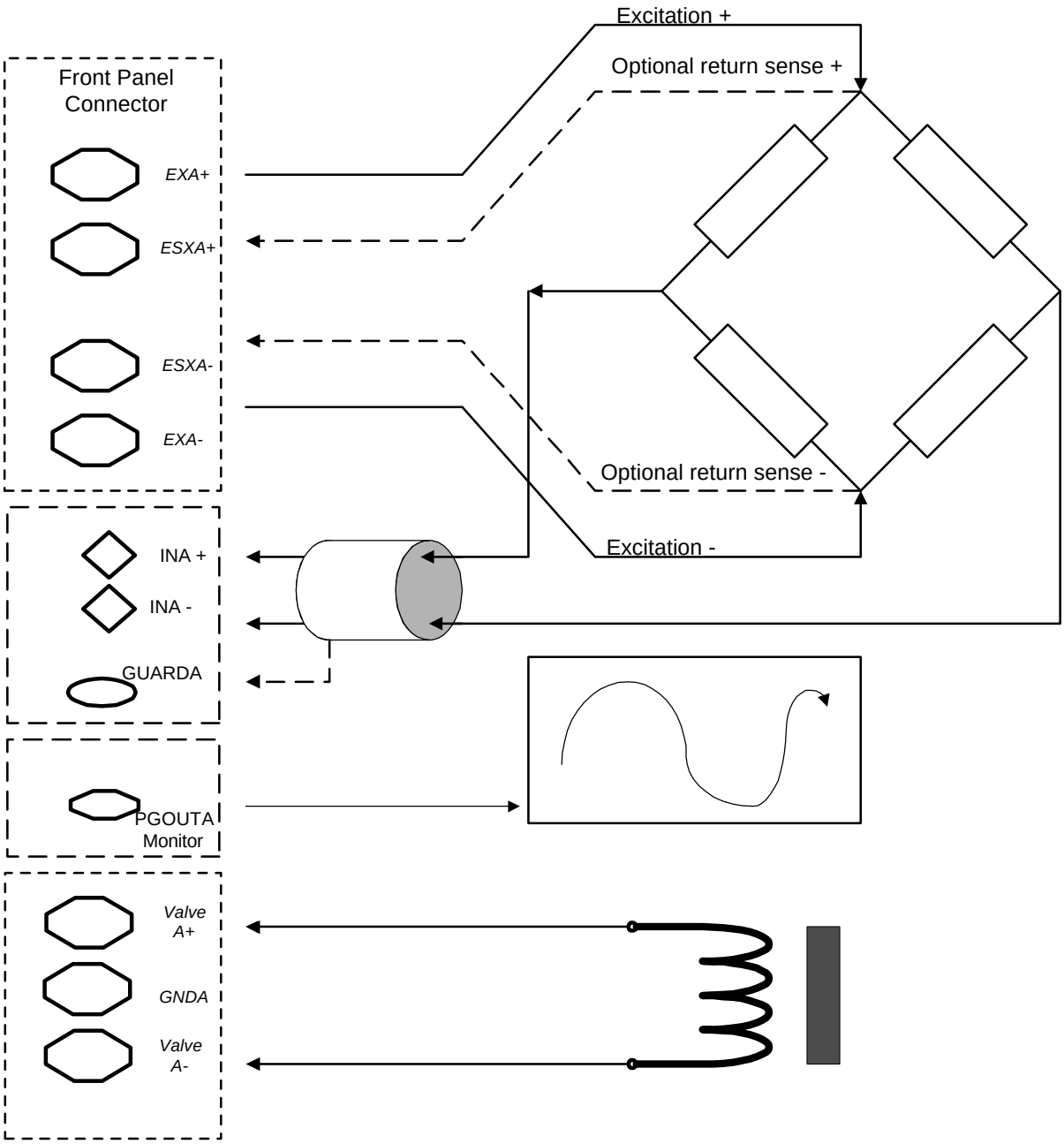

Figure 1 Load cell connection

2.4 Calibration Resistance Register REGCAL

Base address **Slot + $88**

This write only register controls a relay that will connect a internal precision resistor to the line CALAI and CALAO (FOR CHANNEL #1). These two lines, are routed to the front panel connector. This resistance can be connected externally to any of the arm of the loadcell. The resistance is switched “On" with software controlled relay. At reset, all relays are disabled. The calibration resistance value is typically 87.4KΩ +/-1%. Users that want to use another calibration resistance value can short the internal resistance using the internal switch SW1. The new resistance will have to be connected externally. The user is responsible for connecting the two lines to the correct arm of the Bridge.

DATA	LINE	CHANNEL
D00	CALA	CHANNEL #1
D01	CALB	CHANNEL #2
D02	CALC	CHANNEL #3
D03	CALD	CHANNEL #4

Calibration Resistance

SW1	OFF	ON
1-2	CALD = 87.4K	CALD = 0 SHORTED
3-4	CALC = 87.4K	CALC = 0 SHORTED
5-6	CALB = 87.4K	CALB = 0 SHORTED
7-8	CALA = 87.4K	CALA = 0 SHORTED

SW1 Disable Switch

The firmware can detect the presence of the calibration resistance network.

2.5 Status Register

Base address **Slot + $89**

The SCM status register identifies to the VDSP431 the following information:

- SCM module VSB slot location
- Type of signal conditioning module installed

Bit #	Description
0	P2 GA0 slot identification line
1	P2 GA1 slot identification line
2	P2 GA2 slot identification line
3	Calibration resitance module installed if = “0” else “1” if not installed
4	Signal conditionning module # 1 is a PGA if = “0” ,a LVDT if = “1”.
5	Signal conditionning module # 2 is a PGA if = “0” ,a LVDT if = “1”.
6	Signal conditionning module # 3 is a PGA if = “0” ,a LVDT if = “1”.
7	Signal conditionning module # 4 is a PGA if = “0” ,a LVDT if = “1”.