VDSP431

HIGH PERFORMANCE
DIGITAL SERVO CONTROLLER MODULE
4 CHANNEL

REFERENCE MANUAL

Revision 1.4
January 1997

ALPHI TECHNOLOGY CORPORATION
6202 S. Maple Avenue #128
Tempe, AZ 85283 USA
Tel : (602) 838-2428
Fax: (602) 838-4477

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1. GENERAL DESCRIPTION

1.1 INTRODUCTION

The VDSP431 Digital Servo Controller is a set of two different type of module that when connected together provide a complete intelligent system able to control up to 6 channels of double load cell .

Module are :

- VDSP431M

This module is an intelligent DSP base VME module . It can support up to 3 VDSP_SCM module.

-VDSP_SCM

This module is a slave carrier board populated with 2 double load cell signal conditioning.

-Signals conditioning are :

- DC bridge with excitation
- LVDT signal conditioning
- VALVE driver

2. VDSP431M

The primary features of the VDSP431M are as follows:

- VMEbus A16/D16, A24/D16 and A32/D32 Slave Interrupter
- VMEbus Global intercommunication register.
- 128K x 32-bit zero wait state SRAM
- 512K x 32-bit Shared RAM with VMEbus
- One 512K X 8-bit EPROM
- 20 digital I/O lines
- One RS232C interface
- One Serial port interface able to transfer up to 4 Mbit/S.
- Internal trigger driven by 32-bit timer/counter to all channels
- External Front Panel trigger IN
- External Front Panel trigger OUT
- Software Trigger from VMEbus using Programmable Global Register
- Integrated DSP (Digital Signal Processor) running at 32 MHz
- P2 master interface with VDSP_SCM module using P2 backplane.
- Nullpace Input/output signal
- Software watchdog

- Full Instruction block firmware that facilitate communication with the Host Processor
- Possibilities to be stand alone
-

2.1 FUNCTIONAL DESCRIPTION

A functional block diagram of the VDSP431M board is depicted below in Figure 1-1. The VDSP431 is designed around the TMS320C31 that is used to manage the acquisition hardware and to move data to / from the VMEbus. The DSP provides an internal scan clock that paces the acquisition process. The DSP is also used to processes commands from the VMEbus host.

Figure 2-1

2.2 RELATED DOCUMENTS

The following publications listed below may be required for more detailed knowledge of the VDSP431 data acquisition module and its internal components.
VMEbus Specification REV.C1
IEC 821 BUS/IEEE P1014/D1.2

3. THEORY OF OPERATION

3.1 INTERNAL ORGANIZATION

The VDSP431M Board is divided into different sections.
Each section and its relationship to other sections will be discussed. The VDSP431M sections are:

- VMEbus interface
- P2 Master Interface
- Trigger Control
- Data Movement Firmware
- VMEbus Host Interface

3.2 VMEbus INTERFACE

3.2.1 A32/A24 Shared Memory

The local DSP processor shares information with VMEbus masters through a 128K x 32-bit Dual-Access SRAM. The VDSP431 control logic performs the required arbitration to facilitate concurrent access of this SRAM from both the VMEbus and DSP. Normally, this shared memory is only used to pass configuration or setup parameters, but can be used for more general purpose storage. Following a power-on reset, access to this SRAM from the VMEbus is ignored. The VDSP431 has set of MAP registers located in A16 space that allow a VMEbus host to program the starting address of this SRAM to appear in either A32 or A24 address space.

3.2.2 A16 Short I/O Registers

The VMEbus host has access to the VDSP431 I/O registers in A16 space.

3.2.2.1 Fixed Registers

A16 Short I/O BaseAddress + $01

-The **MAP24** register sets the location of the VDSP431 shared memory in A24 space. Following a power-on reset, the VDSP431 shared memory is disabled. The MAP24 register must be written with the requested address for the VDSP431shared memory to respond .

A16 Short I/O BaseAddress + $03

-The **MAP32** register sets the location of the VDSP431 shared memory in A32 space. The MAP32 register must be written to set the VMEbus address of the shared memory.

A16 Short I/O BaseAddress + $05

-The **IVR** (Interrupt Vector Register), is an 8-bit Read/Write register. The value written to this register will be presented to the VMEbus during an interrupt acknowledge (IACK) cycle. The VDSP431 can be programmed to assert an interrupt request to the VMEbus host following command completion or when a block of data has been processed. When the VDSP431 interrupts the VMEbus, the host CPU will run an IACK cycle in order to fetch an interrupt vector.

A16 Short I/O BaseAddress + $07

-The **MAP_TRIG** registersis a write only register that can used as a software trigger. When a host CPU access the A16 address location (only the 8 Upper bit are used) defined by the MAP_TRIG register an internal interrupt is generated to the local DSP. The register still need to be enable by setting bit #1 from the VMERST register to a "1".

A16 Short I/O BaseAddress + $09

-The **MBOX** (mailbox) register is a write only register that is used to interrupt the VDSP431. This register is 16 bit wide that will allows the VDSP431 to faster identifies the Host Command. Also upon reception of this interrupt, the VDSP431 will check shared memory for a new command from the VMEbus host.

A16 Short I/O BaseAddress + $0F

-The **VMERST** register controls the VDSP431 reset, the dual-ported sram and the behavior of the module when its global intercommunication register is accessed.
Bit #0 is used to reset the VDSP431. This register can hold the VDSP431 hardware in a reset state that is independent of the VMEbus SYSRESET.

3.2.2.2 Programmable Register

Global Trigger Register.

The Base Address of this register is defined by the 8 Bit of the **MAP_TRIG** register.
When accessed by a VME Host in a write mode an interrupt is sent to the local DSP processor.
The VME host need to receive an Acknoledge to terminate the cycle.
As more than one Global Register is set at the same address, one of the VDSP431 need to be defined as master and send a DTACK to the VME.
Bit #2 of the Reset Register is used for this function.
The Global Trigger Register is enable by setting the bit #1 of the Reset Register.

3.3 P2 INTERFACE

The VDSP431 communicate with the VDSP_SCM module through the P2 external row connector. The VDSP431 acts as a P2 Master device. The P2 bus at the exception of two signals is compatible with the P2 specifications.
The VDSP_SCM module needs a Scan_Clock signal to initiate a conversion of the A/D converter. This signal is routed through the BUSY* line.
At the End of conversion the VDSP_SCM release the ERR* signal from the bus.
Initialization to access the P2 bus include :

- Reset the P2 window at address $F00002
- Program the Address Space bit # 2 and #3 at the Address $F00006.

A value of $1C at this Address will define :

- P2 space as “System address space “
- Scanclk been generated by the C31 writting at the address $ F0000C

3.4 TRIGGER CONTROL

The VDSP431 supports three different trigger modes. The trigger hardware is depicted below in **Figure 2-1**. The trigger modes are selected through software programming and are also discussed in Section 4 Programming. Trigger isgnal is reouted at the level of :

- P2 for stand alone mode
- P1 for Master Trigger mode

Jumper W5 at the level of the VDSP431 and W2 at the level of the VDSP_SCM must be configured as describe below.

3.4.1 SOFTWARE TRIGGER

Upon writing to the MAP_TRIG register, a task operation is initiated. This task can be a Start of Conversion for the A/D converter.

3.4.2 FRONT PANEL TRIGGER

A SMC connector can be the source of the trigger. This trigger is daisy chain to an output SMC connector for DAISY chained purpose.

3.4.3 INTERNAL TRIGGER

In Internal Trigger mode, all A/D converters are triggered internally via the DSP timer/counter or software writes to the A2DCONV register. The selection of DSP timer/counter or software trigger is made by TCLKCONV. The selected trigger is then routed to all A/D Start Conversion lines. The “Clock Out” front panel connector is driven with internal trigger. The “Clock Out” signal can be connected to the “Clock In” signal of additional VDSP431 boards.

3.4.4 Stand alone trigger mode

In this mode each VDSP431 is responsible to drive the VDSP_SCM SCANCLK for data acquisition. Correct jumper setting must be made at the level of the VDSP431 and the VDSP_SCM. Except for the SOFTWARE trigger each group of A/D associated with one VDSP431 is independent.

3.4.5 Master trigger mode

It is possible for a VDSP431 located in a multiple configuration mode (up to 3 VDSP431 in a chassis) to control the SCANCLK of all the VDSP_SCM inside the chassis. Daisy -chain to other chassis can be made using the Front Panel output of the” Master”
VDSP431.

VDSP431 W5	Description
3-4	Single independent trigger mode using P2 line
1-2	Master trigger mode using P1 line to transfer the SCANCLK to other VDSP_SCM located into the same rack

Table 3-1 VDSP431 trigger mode

VDSPSCM W2	Description
3-4	Single independent trigger mode using P2 line
1-2	Master trigger mode using P1 line to receive the SCANCLK to other VDSP_SCM located into the same Rack

Table 3-2 VDSPSCM trigger mode

3.5 VME A16 SHORT I/O ADDRESS

The VDSP431 supports Short I/O A16/D16, A24/D16 and A32/D32 VMEbus access. Following a power-on reset, only the A16 registers are accessible to the VMEbus. The VMEbus address of the A16 registers is determined by a set of jumpers. Once the A16 address has been set, software can program the starting address of the VDSP431 shared memory. The VDSP431 responds to both supervisory and non-privileged access. Each VDSP431 module occupies 256 Bytes in Short I/O space. Jumper **W8** sets the A16 address as shown below in **Table 3-1**:

VMEbus Address Line	Jumper W8	Off	On
A15	1-2	1	0
A14	3-4	1	0
A13	5-6	1	0
A12	7-8	1	0
A11	9-10	1	0
A10	11-12	1	0
A09	13-14	1	0
A08	15-16	1	0

Table 3-3 A16 Address Jumper W8

NOTE: When a jumper is not present the corresponding address line comparator is pulled-up to a logical “1”.

3.6 VME A24/A32 SHARED MEMORY ADDRESS

The VDSP431 shared memory occupies 2 Mbytes of VMEbus address space. The base address of the shared memory on the VDSP431 is programmed via software. Please refer to Section 4 Programming for additional information.

3.7 VME INTERRUPT SELECTION

The VDSP431 is able to generate an interrupt request to the VMEbus. The interrupt request level IRQ1-IRQ7 is determined by jumpers **W1** and **W2**. Using Table 3-2 below, select the desired interrupt request level and set jumpers W1 and W2 accordingly.

Interrupt Level	W2 Jumper at location	W1 Jumper at location
IRQ 1	13-14	3-4, 5-6
IRQ 2	11-12	1-2, 5-6
IRQ 3	9-10	5-6
IRQ 4	7-8	1-2, 3-4
IRQ 5	5-6	3-4
IRQ 6	3-4	1-2
IRQ 7	1-2	none

Table 3-4 Interrupt Request Level Selection

3.8 FACTORY JUMPERS

All others jumpers located on VDSP431 module are set at the factory and should not be changed. The factory set jumpers are depicted in **Table 3-3** below:

JUMPER	SETTING	PURPOSE
W6	none	Probe input used to program the Mach 445
W5	none	Enable Mach 445 U45 to be programmed
W4	none	Enable Mach 445 U6 to be programmed
W3	none	Enable Mach 445 U19 to be programmed
P5	none	Probe for the TMS320C31 emulator
W10	none	Select EPROM size
P6	none	RS232C SERIAL port
P4	none	TMS320C31 serial port
W9	none	MCMP jumper selection

Table 3-5

3.9 VDSP431 JUMPER LOCATION ILLUSTRATION

Figure 3-1

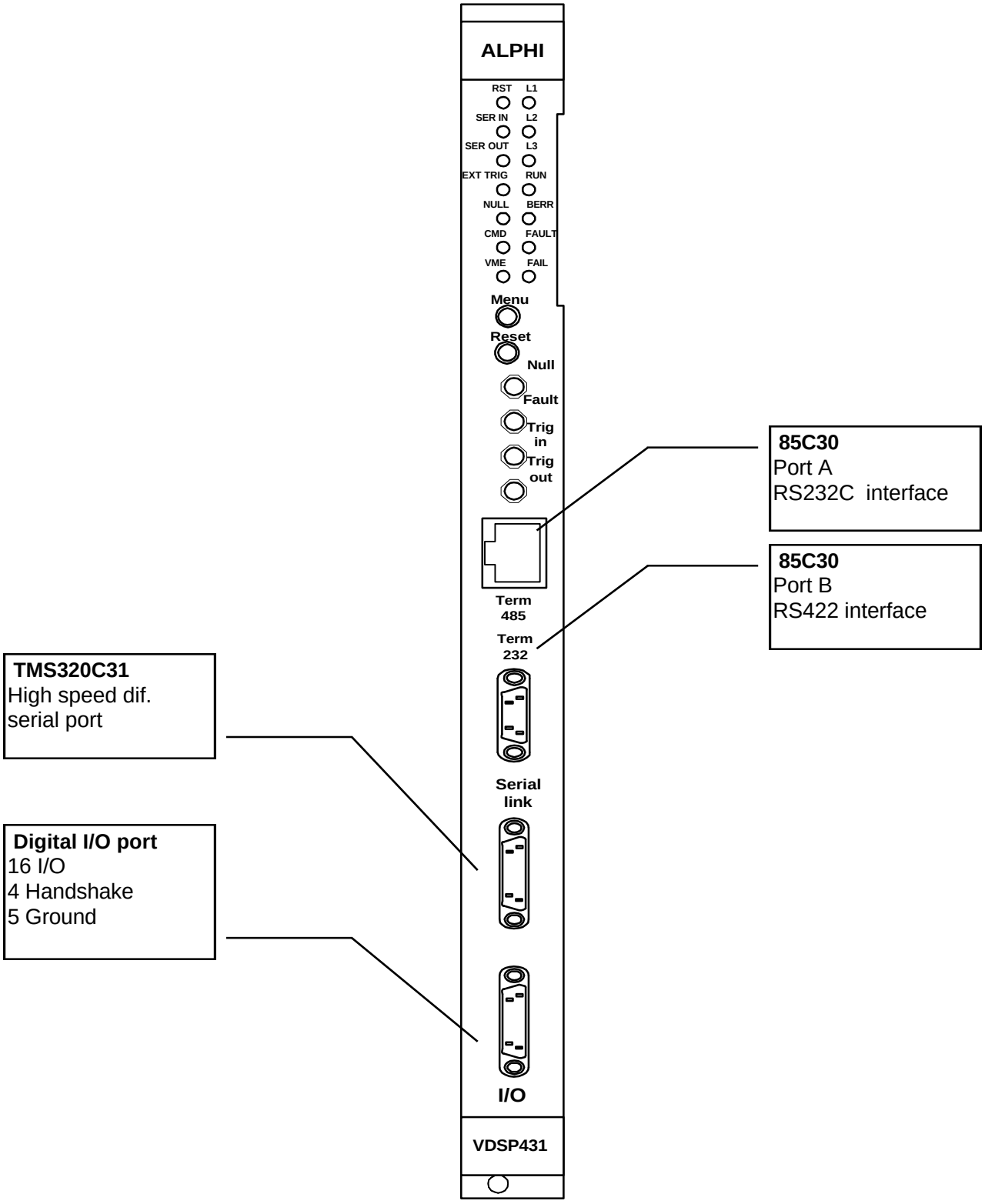


Figure 3-2

4. PROGRAMMING

Two separate group of registers are accessible by the Host VME in the short I/O space.

-***Standard A16 Short I/O*** register witch base address is jumper selectable and are unique by system.

-***Global Register*** witch base address is software programmable through the Standard A16 Short I / O Base address register using the MAP_TRIG register address.

When the Host Processor write at this location a 16 bit word , an interrupt is send to the local DSP. This interrupt can be use to Pace any command. Also the Interrupt is lacthed and can be read by the DSP at the level of the Status Register. One of the VDSP431M module will have to be programmed as Master to send an acknowledge to the Host Processor that may not be designed with Global Register possibilities.

The register still need to be enable by setting bit #1 from the VMERST register to a "1".

One of the VDSP431M module will have to be designed as Master to send an acknowledge to the Host Processor that may not be designed with Global Register possibilities(Auto generation of local DTACK).

Bit #2 of the VMERST register when set to a "1" enable the corresponding VDSP431 to generate a DTACK to the VMEbus.

4.1 A16 SHORT I/O REGISTERS

The VDSP431 A16 Register are shown below in Table 4-1:

A16 Short I/O Address	Register Name	Description	Read/Write
BASE ADDRESS + $01	MAP24	A24 Address Map Bits	W
BASE ADDRESS + $03	MAP32	A32 Address Map Bits	W
BASE ADDRESS + $05	IVR	Interrupt Vector Register	R/W
BASE ADDRESS + $07	MAP_TRIG	Software location trigger address	W
BASE ADDRESS + $09	MBOX	Mail Box Register	W
BASE ADDRESS + $0F	RESET	VDSP431 Hardware Reset	W

Table 4-1

4.1.1 MAP24 REGISTER

BASE ADDRESS + $01

The MAP24 register sets the location of the VDSP431 shared memory in A24 space. Following a power-on reset, the VDSP431 shared memory is disabled. The MAP24 register must be written to set the VMEbus address of the shared memory. This register is write only and cannot be read back. Software must maintain a shadow copy of the register contents. The MAP24 register is defined below:

BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 00
A23	A22	A21	not used	not used	not used	not used	ENABLE

4.1.2 MAP32 REGISTER

NOTE: When a bit is set to a "1", the comparator is active if the corresponding address line is equal to a "1".
Bit 0 of this register must be set to a "1" to enable to shared memory decoder.

BASE ADDRESS + $03

The MAP32 register sets the location of the VDSP431 shared memory in A32 space. Following a power-on reset, the VDSP431 shared memory is disabled. The MAP32 register must be written to set the VMEbus address of the shared memory. This register is write only and cannot be read back. Software must maintain a shadow copy of the register contents. The MAP32 register is defined below:

BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 00
A31	A30	A29	A28	A27	A26	A25	A24

NOTE: When a bit is set to a "1", the comparator is active if the corresponding address line is equal to a "1". Bit 0 of the MAP24 register must be set to a "1" to enable to shared memory decoder.

Example : Host A32 master access on VME is $01000000.
Write $01 at address Base Address + $02 to enable Dual ported Sram
Write $01 at address Base Address + $03 to match the VME host Address.

4.1.3 INTERRUPT VECTOR REGISTER (IVR)

BASE ADDRESS + $05

The Interrupt Vector Register is an 8-bit Read/Write register. The value written to this register will be presented to the VMEbus during an interrupt acknowledge (IACK) cycle. The VDSP431 can be programmed to assert an interrupt request to the VMEbus host following command completion or when a block of data has been processed. When the VDSP431 interrupts the VMEbus, the host CPU will run an IACK cycle in order to fetch an interrupt vector. The IVR register is defined below:

BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 00
IV07	IV06	IV05	IV04	IV03	IV02	IV01	IV00

4.1.4 MAP_TRIG REGISTER

BASE ADDRESS + $07

The MAP_TRIG register sets the location of the VDSP431 Software trigger. Following a power-on reset, the VDSP431 shared memory is disabled. The MAP32 register must be written to set the VMEbus address of the shared memory. This register is write only and cannot be read back. Software must maintain a shadow copy of the register contents. The MAP_TRIG register is defined below.
Enable of the decoding is made using bit # 1of the VMERST register
Master VDSP431M in charge of sending an acknowledgeto VMEbus is programmable by setting bit#2 of VMERST register.

BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 00
A15	A14	A13	A12	A11	A10	A09	A08

Note : By using different address in a Multi VDSP431 system, it is possible to select witch VDSP431 have to responds to one Address.

4.1.5 MAILBOX REGISTER (MBOX)

BASE ADDRESS + $09

The Mailbox register is a write only register that is used to interrupt the VDSP431. Upon reception of this interrupt, the VDSP431 will check shared memory for a new command from the VMEbus host.

BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 00
-	-	-	-	-	-	-	-

4.1.6 RESET REGISTER

BASE ADDRESS + $0F

The Reset register is used to :

- Reset the VDSP431. This register can hold the VDSP431 hardware in a reset state that is independent of the VMEbus SYSRESET. This register is write only and cannot be read back. Software must maintain a shadow copy of the register contents.
- Enable the Global Address Register
- Enable the Master mode for the VDSP431 to generate a VMEbus DTACK.

BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 00
-	-	-	-	-	MASTER	GLOBAL ENABLE	RST

RST

When RST = 1, the VDSP431 is held in RESET. When RST = 0, the VDSP431 is released from RESET.

GLOBAL ENABLE

When set to a”1” the VDSP431 will generate a local interrupt if the Host computer access the Global register address.

MASTER

If set to a “1”, the VDSP431 module generate a DTACK acknowledge to a Global register access from the Host.

4.2 VDSP431 INTERNAL ADDRESS MAP

This section will describe the local memory map of the VDSP431 as seen by the DSP. This information is being provided for those customers who wish to write their own firmware. ALPHI Technology can provide you with a toolkit containing the necessary header files to build your own applications. Contact the factory for more information.

4.2.1 MEMORY MAP

The local memory spaces accessible by the DSP are illustrated below in Table 4-2:

MEMORY RANGE	MEMORY DESCRIPTION
0x00000000 - 0x0001FFFF	128K x 32 High-Speed Static RAM
0x00400000 - 0x0043FFFF	256K x 8 Boot EPROM
0x00480000 - 0x0049FFFF	128K x 8 Flash
0X004C0000 - 0X004FFFF	DPR Mezzanine module
0x00500000 - 0x0051FFFF	512K x 32 VMEbus Shared Memory
0x00F80000 - 0x00F83FFF	16K x 32 P2 Access Window

Table 4-2

4.2.2 I/O REGISTERS

The local memory mapped I/O registers are summarized below in Table 4-3:

REGISTER ADDRESS	REGISTER NAME
0x00F00000	CTRL0
0x00F00001	CTRL1
0x00F00002	P2 WINDOW UPPER ADDRESS
0X00F00003	CS_BUG
0X00F00005	CS_ITSTAT
0x00F00006	CS_C31CTRL
0x00F00007	WATCHSET
0x00F00008	SLOT
0x00F00009	VMEIRQ
0x00F0000A	GLOBAL REGISTER
0x00F0000B	CS_LED'S
0x00F0000C	A2DCONV
0X00F000010-13	Serial port 85C30
0X00F000014-17	I/O port 85C36
0X00F8000-FBFFF	P2WINDOW ACCESS

Table 4-3

4.2.3 CTRL0 REGISTER

ADDRESS $00F00000

The CTRL0 register :

The function of each bit in defined below:

BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 00
-	-	-	-	Not Used 3	WATCHDOG	Not Used1	Not Used0

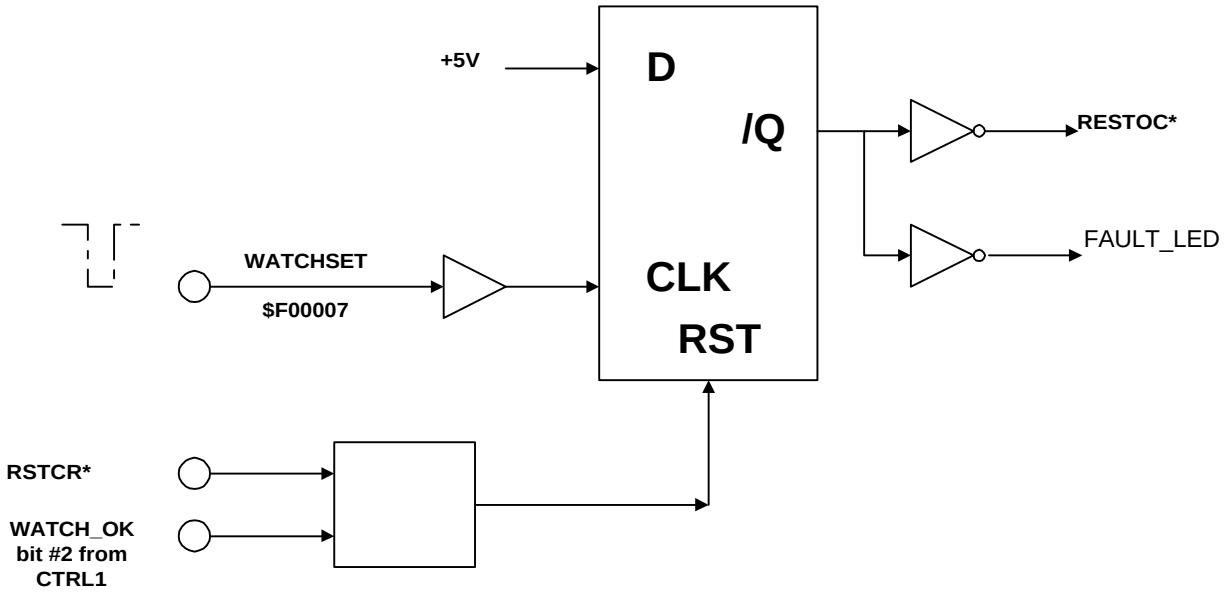
Not used Bit 0 Not Used0
This bit is reserved for future application.

Not used Bit 1 Not Used0
This bit is reserved for future application.

Watchdog timer bit WATCHDOG

Upon reset a latch is set to a Fault position(Low Open drain output) until the local processor remove the latch from it's reset position (setting ***bit #2 from CTRL1*** at address ***$F00001*** to " 1") and making a write access at address $ ***F00007*** to a " No Fault" position (High open).
If the Software watchdog timer is enable (WATCHSOFT = "1") the local processor has to "TOGGLE" bit #2 WATCHDOG from the CTRL0 register in a timely manner(no more than 250ms) to avoid the DS1232 Watchdog chip to reset. Fail to refresh the DS1232 ,a local reset will occurs and the **Fault** led will be activated.
A low "Fault position " is set and stay until the local firmware is "healthy " again to reset the Latch.

Not used Bit 3 Not Used3
This bit is reserved for future application.



4.2.4 CTRL1 REGISTER

ADDRESS $00F00001

The function of each bit in defined below:

BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 00
-	-	-	-	WATCHSOFT	WATCH_OK	RST_C31Z	ZCTRL

ZCTRL MEZZANINE CTRL Signal

This bit controls behavior of the DSP mezzanine module.

RST_C31Z RST_C31Z reset

This bit controls the RESET of the Mezzanine module.

WATCH_OK Watchdog reset

Upon Power_on reset the WATCHDOG latch is maintained in a reset mode until the WATCH_OK bit is set to a “1” by the healthy local DSP. Now, upon finishing its internal self test the DSP write at the address $F00007 to remove the Fault position.

WATCHSOFT Watchdog clock selection

When = “0” (after a Power reset) this signal direct the clock used to maintained the DS1232 watchdog disable to H1 CLOCK from the DSP processor. When set to a “1” by software, the clock will be the bit #2 of the CTRL0 register.

4.2.5 P2 WINDOW ADDR REGISTER

4.2.5.1 ADDRESS $00F00002

This register is used to drive the P2 address lines :

Access are made only in a 32 bit mode to the P2 bus.

VSIZE1	VSIZE0	TRANSFER SIZE
0	0	32-bit four bytes

CPU Window Mode - A 16K X 32 bit window to the P2 address space is available to the DSP. This windows starts at the address $00F80000 and ends at $00F83FFF. Bit 16 of this register corresponds to address line A16 on the P2.
The function of each bit in defined below:

CPU Window Mode

BITS 31 - 16	BITS 15 - 00
P2 Address Lines A31 - A16	-

The VDSP_SCM module checks only the 16 lower address. The upper address must be set to “0”.

4.2.5.2 P2 ADDRESS MAP

ADDRESS $F80000

The VDSP431 is able to control up to three (3) VDSP_SCM module.
Each module occupies 1024 Bytes. Access is allowed in 32 bits mode only.
Each VDSP_SCM detect an access by comparing the upper address XLA08 to XLA10 (VSAD10 to VSAD12) with the Physical slot location defined by GA0 ,GA1, GA2.
Location "0" is reserved for the P2 controller, VDSP431.
First VDSP_SCM is located at address $F80100.
No jumper setting is needed for the VDSP_SCM . Each memory address from the TMS320C31 use 4 Bytes. Only the lower two bytes are used (VSD00-VSD15).

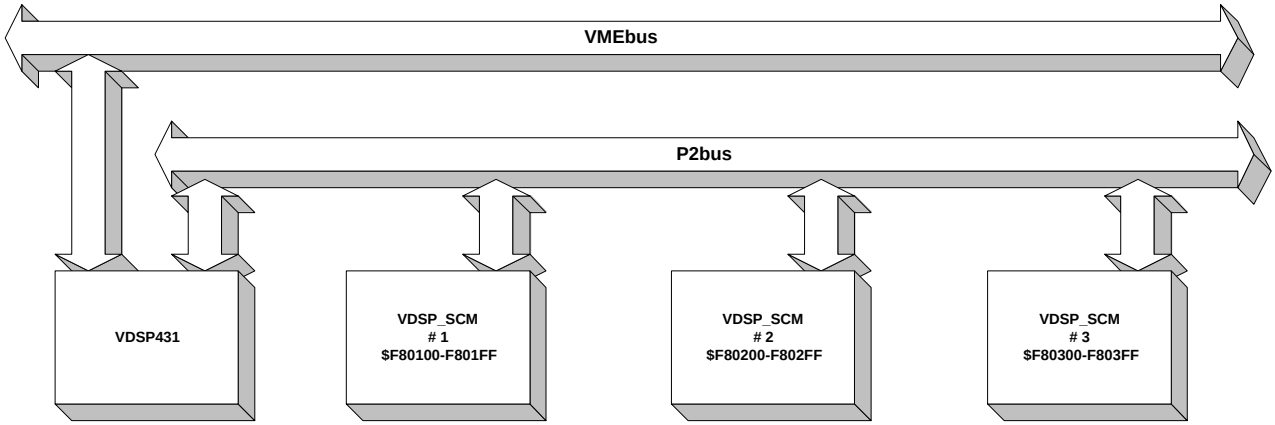


Figure 3 VDSP431 VPDS_SCM Interconnection

4.2.6 BERR or BUG detector

ADDRESS $00F00003

The TMS320C31 does not have an internal watchog that can prevent the module to "crash" in the event of the Firmware accessing a register or VDSP_SCM module that does not responds. A delay timer is implemented in such a way that after a long delay the timer send an acknoledge to the DSP to terminate the cycle, send an interrupt to imform the DSP of a "Problem", latch the address, R/W , and interrupt that the DSP was tryng to access. The DSP can then read the status of the address BUG and recovers , ping-point the failure.

BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 00
MA07	MA06	MA05	MA04	MA03	MA02	MA01	MA00

Table 4-4

BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 09	BIT 08
MA15	MA14	MA13	MA12	MA11	MA10	MA09	MA08

Table 4-5

BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16

MA23	MA22	MA21	MA20	MA19	MA18	MA17	MA16

Table 4-6

BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24
Not Used	Not Used	MCMP	INT3	INT2	INT1	INT0	XLIORW

Table 4-7

4.2.7 INTERRUPT STATUS REGISTER

ADDRESS $00F00005

4.2.7.1 INTERRUPT SOURCE

The TMS320C31 has only for interrupt lines available. More than one source of interrupt share the same interrupt. The interrupt status register allow the DSP to identifies the interrupt source. Each interrupt is latched and toggling the correspondant bit at the C31_CTRL register lear the latch.

INTERRUPT SOURCE	NAME	C31 Interrupt and bit #	ITStaT Reg bit #	RESET_IT VME/P2 Reg
End of A/D conversion	V_ERRB	INT0		none
BOOT	BOOT	INT1		RESET
GLOBAL REG access	Global _IT	INT1	GLOBAL #7	#7 toggle
VME_CTRL access	VME_CT RL_IT	INT1	VMEIRQ #6	#6 toggle
IACK_IT access	CLINT_IT	INT1	IVRIACK #5	#1 toggle
BUG	IT_BUG*	INT2	BERR #4	#0 toggle
SCC8530	IT85	INT2	IT85 #3	8530 access
local 8536	IPIA	INT2	IPIA #2	8536 access
MEZZANINE	MEZ_IT	INT2	MEZ_IT #1	access Mezzanine
SCM 8536	V_IRQB*	INT2	SCM8536 #0	SCM access
FP_IT	FP_IT	INT3		

The interrupt BOOT signal is used to load the program stored in EPROM by generating an interrupt INT1* on RESET. The signal MCMP* must be high (no jumper on J5).

4.2.7.2 ITSTAT REGISTER

ADDRESS $00F00005

BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 00
GLOBAL	VMEIRQ	IVRIACK	BERR	IT85	IPIA	MEZ_IT	SCM8536

GLOBAL GLOBAL = 1 when the VME host has access the Global Register address of the module.

VMEIRQ VMEIRQ = 1 when the VMEbus writes to the MBOX Short I/O register

IVRACK IVRACK = 1 when the DSP interrupts the VMEbus. IVRACK = 0 when the VMEbus runs an IACK cycle reading the IVR Short I/O register

BERR BERR =1 .The DSP has made an access to a location that doesn't return an Acknowledge. After 32 cycle the local logic generate a ACK to prevent the DSP to Stay lock. An interrupt is issue and the Address ,XLIORW, IRQ0-3 are latched. The DSP can detect the origin of the failure.

IT85 IT85 =0 The local Serial controller 85C30 has been programmed to generate an interrupt.

ITPIA ITPIA =0 The local parallel I/O PORT controller has been programmed to generate an interrupt.

MEZ_IT MEZ_IT = 0 The second DSP module has generate an interrupt to the Main DSP processor.

SCM8536 SCM8536 = 0 Each SCM module has a Parallel I/O Port 8536 able to generate an interrupt on certain programmable condition. The SCM interrupt are Ored to an open Drain buffer output line. When detecting an interrupt the DSP controller need to check every SCM8536 to find the origin of the interrupt.

4.2.8 C31_CTRL VME/P2 CTRL REGISTER

ADDRESS $00F00006

The VME/P2 CTRL register has multiple function :

- controls the behavior of the P2 bus .
- Define source of the SCANCLK for the A/D converters.
- Reset interrupt latches by toggling to a "1" the correspondant bit

The function of each bit in defined below:

BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 00
GLBL_RST_IT	VME_RST_IT	MODE1	MODE0	VSPACE1	VSPACE0	IACK_RST_IT	SCM_RST_IT

SCM_RST_IT When toggle to a "1" the bit reset the latch that memorize an interrupt generated by one of the SCM 8536 Digital I/O controller.

IACK_RST_IT When toggle to a "1" the bit reset the latch that memorize an "Interrupt acknowledge phase " made by the VME host due to an interrupt generated by the VDSP431

VSPACE0 Refer to Table 4-6
VSPACE1 Refer to Table 4-6

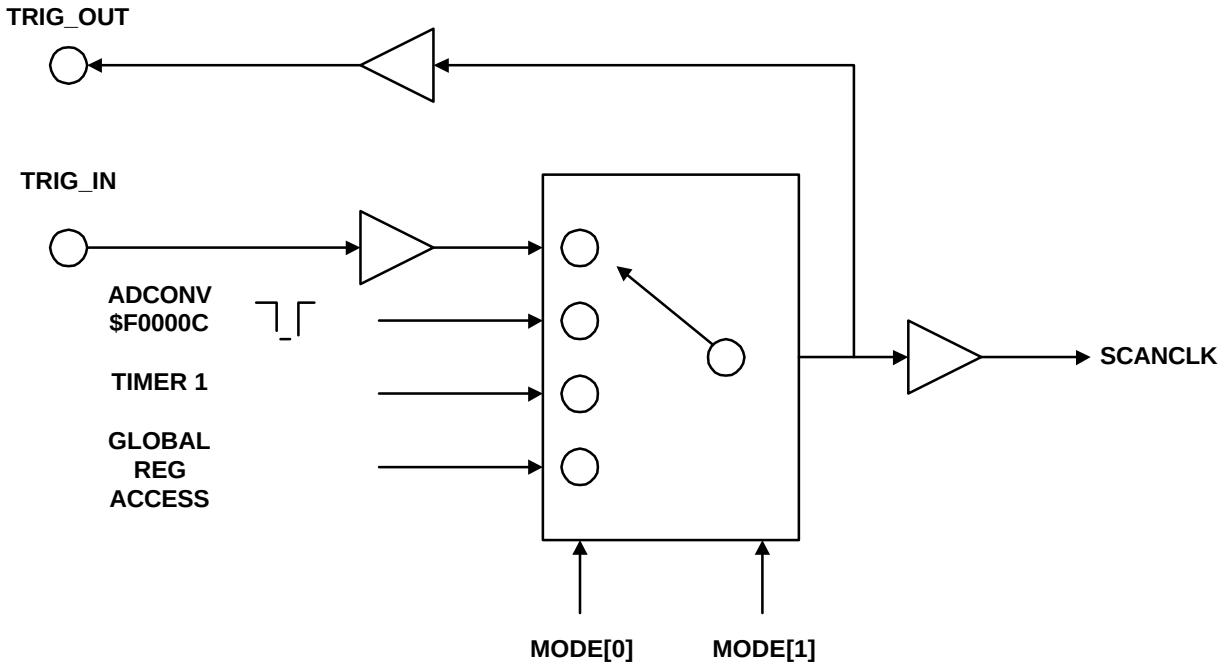
VSPACE1	VSPACE0	P2 ADDRESS SPACE
0	1	ALTERNATE ADDRESS SPACE
1	0	I/O ADDRESS SPACE
1	1	SYSTEM ADDRESS SPACE

Table 4-8 P2 Address Space Selection

MODE0 ,MODE1 See Tables Below

MODE1	MODE0	TRIGGER SOURCE
0	0	Internal DSP timer1
0	1	Local Address access ADCONV
1	0	Front Panel input
1	1	Global Register access

Table 4-9 Trigger source Selection



IACK_RST_IT When toggle to a "1" the bit reset the latch that memorize an "Interrupt acknowledge phase " made by the VME host due to an interrupt generated by the VDSP431.

GLBL_RST_IT When toggle to a "1" the bit reset the latch that memorize an "Global register access " made by the VME host .

4.2.9 VME/P2SLOT REGISTER

ADDRESS $00F00008

The P2SLOT register provides information about P2 or VMEbus activity
The function of each bit in defined below:

BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 00
Not used	LIMIT	NOPACE	MEZ_ON	MASTER	GA2	GA1	GA0

GA2-GA0 These bits define the location of the VDSP431 on the P2 bus "0" should be the correct position for Slot "0" location.

MASTER The present VDSP431M module is in charge of sending the VME TACK to an Host access to the Global register location.

MEZ_ON The Mezzanine module is installed if the bit is = to a “0”.

NOPACE Reflect the Output Collector signal NULLPACE at the level of the Front Panel.

LIMIT Read back of the Front Panel LIMIT output

NOT USED = “1”

4.2.10 VME_IRQ REGISTER

ADDRESS $00F00009

The VME_IRQ register is used to assert and send an interrupt to the VMEbus. The interrupt level (IRQ1 - IRQ7) is determined by VDSP431 hardware jumper settings. Any write access to this register will assert an interrupt to the VMEbus. The function of each bit in defined below:

BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 00
X	X	X	X	X	X	X	X

X = Don’t care
Interrupt level is defined by setting the jumpers described on paragraph 3.7.

4.2.11 GLOBAL INTER-COMMUNICATION REGISTER

ADDRESS $ F0000A

This register is written by at he HOST processor at the address define by the MAP_TRIG register. A 16 bit word read at the address $F0000A by the DSP can be used for Command control of the VDSP431.

4.2.12 CS LED'S

ADDRESS $F0000B

The Front Panel is populated with LED'S that provide some USER information about the Behavior of the VDSP431 module. From the Fourteen (14)LED'S , six (6) are controlled by software and the other are a direct image of signals located inside the VDSP431 module.

BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 00
Not Used	LIMIT	NULL-PACE	Not Used	LED2	LED1	FAIL	BERR

Table 4-10

4.2.13 A2DCONV REGISTER

ADDRESS $00F0000C

The A2DCONV register is used to issue a software trigger to the A/D converters. When the DSP make a write access to this register , it sends a trigger to all A/Ds. The function of each bit in defined below:

BIT 07	BIT 06	BIT 05	BIT 04	BIT 03	BIT 02	BIT 01	BIT 00
X	X	X	X	X	X	X	X

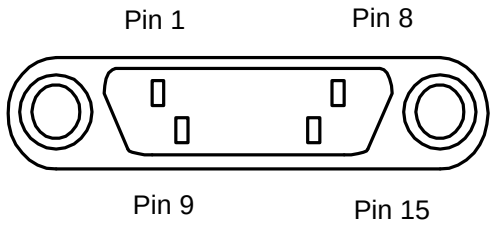
X = Don't care

4.3 Communication ports

4.3.1 TMS320C31 Serial port (Option)

The VDSP31 module has a serial communications ports available to the Front Panel interface module .

The Synchronous port (optional) provide up to 8 Mbits transfer. Each signal is buffered by a RS422 buffer interface. Signals are available at the front panel using a 15 Pin connector.



	PIN		PIN
Pin 1	FSX0+	Pin 9	FSX0-
Pin 2	GND	Pin 10	DX0+
Pin 3	DX0-	Pin 11	GND
Pin 4	CLKXO+	Pin 12	CLKX0-
Pin 5	DR0+	Pin 13	DR0-
Pin 6	GND	Pin 14	FSRO+
Pin 7	FSR0-	Pin 15	CLKR0+
Pin 8	CLKR0-		

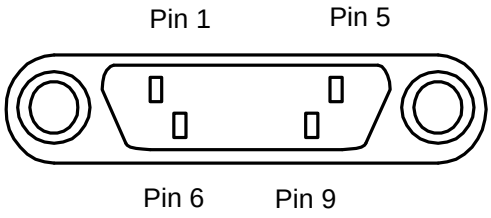
PIN	SIGNAL NAME	DESCRIPTION
8	CLKRO-	Serial port 0 receive clock. This pin serves as the serial shift clock for the serial port 0 receiver.
15	CLKRO+	Serial port 0 receive clock. This pin serves as the serial shift clock for the serial port 0 receiver.
12	CLKXO-	Serial port 0 transmit clock. This pin serves as the serial shift clock for the serial port transmitter
4	CLKXO+	Serial port 0 transmit clock. This pin serves as the serial shift clock for the serial port transmitter
13	DRO-	Data receive. Serial port 0 receives serial data via the DRO pin
5	DRO+	Data receive. Serial port 0 receives serial data via the DRO pin

3	DXO-	Data transmit output. Serial port 0 transmits serial data on this pin.
10	DXO+	Data transmit output. Serial port 0 transmits serial data on this pin.
7	FSRO-	Frame synchronization pulse for receive. The FSRO pulse initiates the received data process over DRO.
14	FSRO+	Frame synchronization pulse for receive. The FSRO pulse initiates the received data process over DRO.
9	FSXO-	Frame synchronization pulse for transmit. The FSXO pulse initiates the transmit data process over DXO.
1	FSXO+	Frame synchronization pulse for transmit. The FSXO pulse initiates the transmit data process over DXO.
2	GND	
11	GND	
6	GND	

4.3.2 Serial communication controller 85C30

BASE ADDRESS $F00010 - $F00013

A SCC85C30 serial communication controller provide two communication port :
- Port A an RS232C asynchronous serial communication port .Clock for the 85C30 is 4.9 MHZ.
The serial connector is available to the front panel using a subminiature 9 pin connector.
The Terminal port use a 9 Pin Subminiature female connector as RS-232C interface



	Terminal	port
Pin 1		
Pin 2	RS232_TX	Output
Pin 3	RS232_RX	Input
Pin 4	RS232_CTS	Input
Pin 5	GND	
Pin 6	RS232_RTS	Output
Pin 7	GND	
Pin 8		
Pin 9		

- Port B an RS422/485 communication port available to front panel using a RG45 connector.

4.3.2.1 OPTION 1

PINOUT WITH W14JUMPER BETWEEN 2-3 AND W13 JUMPER BETWEEN 2-3 AND W12 NO JUMPER

	Terminal	port
Pin 1	RS422A_TX+	Output
Pin 2	RS422A_TX-	Output
Pin 3	RS422A_RX+	Input
Pin 4	RS422A_RTS+	Output
Pin 5	RS422A_RTS-	Output
Pin 6	RS422A_RX+	Input
Pin 7	RS422A_CTS+	Input
Pin 8	RS422A_CTS-	Input

Table 4-11 OPTION 1

4.3.2.2 OPTION 2

The TX buffer can be enable by the ligne RTS using jumper W12 (jumper between pin 1-2) to emulate RS485 interface.

W12 jumper	Interface
none	RS422A
1-2	RS485

Table 4-12 option 2

4.3.2.3 OPTION 3

The RTS buffer can also Transmit the Transmit CLOCK and the CTS buffer can receive a Reiceved clock.

PINOUT WITH W14JUMPER BETWEEN 1-2 AND W13 JUMPER BETWEEN 1-2 AND W12 NO JUMPER

	Terminal	port
Pin 1	RS422A_TX+	Output
Pin 2	RS422A_TX-	Output
Pin 3	RS422A_RX+	Input
Pin 4	RS422A_TXCLK+	Output
Pin 5	RS422A_TXCLK-	Output
Pin 6	RS422A_RX+	Input
Pin 7	RS422A_RXCLK+	Input
Pin 8	RS422A_RXCLK-	Input

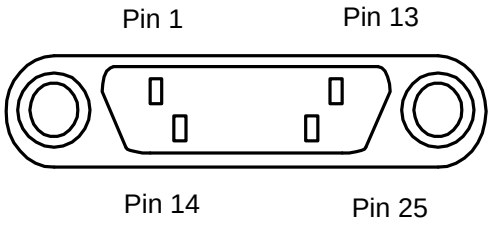
Table 4-13 OPTION 3

5. DIGITAL Inputs / Outputs

BASE ADDRESS $F00014 - $F00017

A 8536 is used to provide up to 20 digital TTL Inputs / Outputs available on a subminiature 25 Pin connector.
Two group of 8 channels can be selected as input or output by jumper.
They corresponds to the PortA and Port B of the 8536.
Four (4) other channels (Port C) can be selected separately as input or output by set of jumpers.
For more information about programation of the 8536 refers to the data sheet manufacturer.

The I/O DIGITAL port use a 25 Pin Subminiature female connector



	PIN		PIN		PIN
Pin 1	PA07	Pin 10	PB00	Pin 19	PB07
Pin 2	PA05	Pin 11	FAULT	Pin 20	PB05
Pin 3	PA03	Pin 12	FP_PC2	Pin 21	PB03
Pin 4	PA01	Pin 13	FP_PC0	Pin 22	PB01
Pin 5	GND	Pin 14	PA06	Pin 23	GND
Pin 6	GND	Pin 15	PA04	Pin 24	FP_PC3
Pin 7	PB06	Pin 16	PA02	Pin 25	FP_PC1
Pin 8	PB04	Pin 17	PA00		
Pin 9	PB02	Pin 18	LIMIT		

6. Front Panel

6.1 LED's

Base address :$F0000B

The Front Panel displays two type of LED's. Some are directly reflecting the Image or status of a signal.
Some can be programmed by software and be used for diagnostic purpose. Six bit from a register located at the Address **$F00002 drive** the LED'S.

LED's name	Driving Signal	Description	Software bit location
RUN	DSP strobe	Active low	
VME	VME_ACCES	The Host VME has made an access to the A16 Register	
CMD	VME_CTRL2	The Host VME has made an access to the A16 Global Register	
RESET	DSP Reset	Active low	
FAULT	RSTMEM	The VDSP431 module Watchdog has been activated due to DSP failure by H1 clock failure or DSP not able to refresh the Watchdog in time....	
EXT TRIGGER	F.Panel trigger	A Front Panel Trigger has been detected .	
SERIAL IN	DR0	Serial port input data active	
SERIAL OUT	DX0	Serial port output data active	
NULL PACE	Under DSP control	The DSP has detected that a command has not been executed "properly "	Bit #5 CS_LED Reg
BERR	BUG_IT	Hardware watchdog (32cycle) has been activated	Bit #0 CS_LED
FAIL			Bit #1 CS_LED
LED1			Bit #2 CS_LED
LED2			Bit #3 CS_LED
LED3			Bit #4 CS_LED

A Flat cable can be connected on the back of the Front Panel to remotely displays and provide all the signals from the Front Panel.

6.2 NULL PACE

The NULL PACE output signal is controlled by software to inform through an open drain output at the level of the front panel that the task assigned to the local processor is not executed within the "normal time allocated and that something is wrong with the "model" under test .
The local processor write a "1" to the ***bit # 5*** of the ***CS_LED*** Register (***$F00002***).
An open drain is active low allowing Oring of the **Null Pace *** signal with other modules.
The read-back of the status of the output is available at the level of the ***P2/VME Status*** register at address ***$ F00008 bit # 5.***

6.3 SWITCHES

Two Push Buttons on the Front Panel provide the following function :

-Reset When push Reset the Local D.S.P.

-Menu When push an interrupt is generated to the D.S.P. that will Initiate a Menu Program using the RS232 port.

6.4 Connectors

