VDSP431

HIGH PERFORMANCE
DIGITAL SERVO CONTROLLER MODULE

INSTALLATION MANUAL

Revision 1.0
March 1997

ALPHI TECHNOLOGY CORPORATION
6202 S. Maple Avenue #128
Tempe, AZ 85283 USA
Tel : (602) 838-2428
Fax: (602) 838-4477

NOTICE

The information in this document has been carefully checked and is believed to be entirely reliable. While all reasonable efforts to ensure accuracy have been taken in the preparation of this manual, ALPHI TECHNOLOGY assumes no responsibility resulting from omissions or errors in this manual, or from the use of information contain herein.

ALPHI TECHNOLOGY reserves the right to make any changes, without notice, to this or any of ALPHI Technology's products to improve reliability, performance, function or design.

ALPHI TECHNOLOGY does not assume any liability arising out of the application or use of any product or circuit described herein; nor does ALPHI TECHNOLOGY convey any license under its patent rights or the rights of others.

1. HARDWARE PREPARATION

To ensure proper operation of the VDSP431 module, certain procedures must be followed to guarantee proper operation. The following cooling requirements, jumper configurations, I/O connectors and cable assemblies, and switches must be properly prepared and installed.

1.1 COOLING REQUIREMENTS

The **VDSP431** control system is designed to operate reliably with an incoming air temperature range from 0° C to +50° C **with forced air cooling**. The following conditions should be met to match manufacturing testing procedures with in-the-field operation:

- The temperature cooling requirements must be performed in a standard VME chassis.
- The airflow from three axial fans should be greater than 75 CFM per fan.
- The incoming air temperature should be measured between the forced air fan
- cooling assembly and the VME card cage.
- Test software should be run while the system is operational. The test software should exercise the entire system. If a failure due to heat occurs, the test procedure should indicate that an abnormal stop has occurred.

1.2 FACTORY CONFIGURATION

The VDSP431 module does not require jumper changes unless the standard configuration needs to be changed.

2. INTRODUCTION

The VDSP431 is a VME based Digital Servo Controller System.

The Minimum configuration includes :

- VME 6U chassis (21 slots) with VSB overlay (up to 3)
- Independent VMEbus Host Controller
- VDSP431 Digital Servo Controller
- VDSPSCM Signal Conditioning Module
- VDSP431 I/O Interface rack

3. VME 6U CHASSIS

The VME 6U chassis provides 21 VME slots with up to 3 VSB overlays (6 slots). Each VDSP431 controller can support up to 3 SCM modules as shown below. The chassis has been selected to provide a high air flow circulation. Slot # 1 is reserved for the Host VMEbus Controller. Slots #2, #9 and #16 are for the VDSP431 controller. The SCM modules can be relocated without any jumper modification.

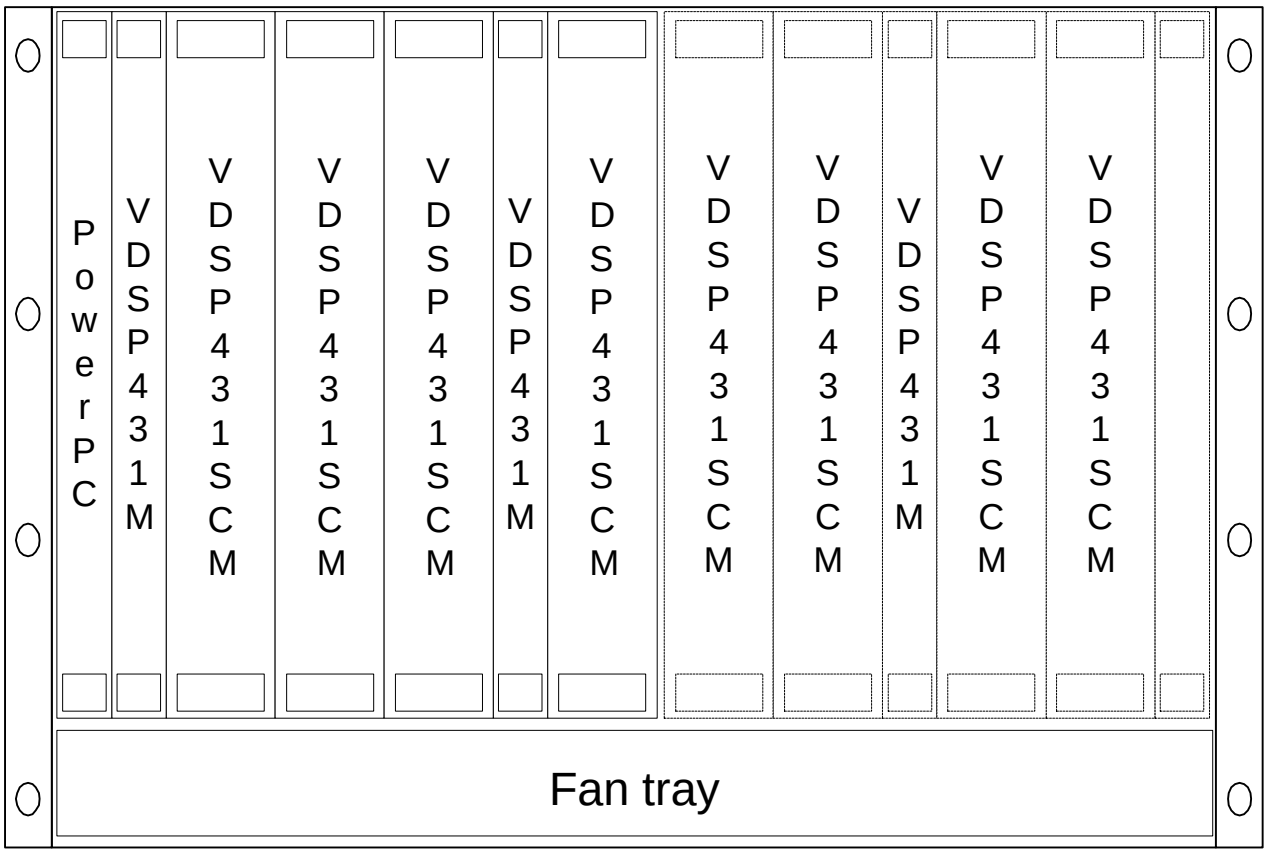


Figure 3-1

Slot	Module	A16 Offset	W2 Jumper Settings	Note
1	Host VME controller	N/A	N/A	Customer defined
2	VDSP431 # 1	$0100	1-2,3-4,5-6,7-8,9-10,11-12,13-14	No Jumper between 15-16
3	VDSPSCM			Channel # 1 -2
5	VDSPSCM			Channel # 3 -4
7	VDSPSCM			Channel # 5 -6
9	VDSP431 # 2	$0200	1-2,3-4,5-6,7-8,9-10,11-12, 15-16	No Jumper between 13-14
10	VDSPSCM			Channel # 1 -2
12	VDSPSCM			Channel # 3 -4
14	VDSPSCM			Channel # 5 -6
16	VDSP431 # 2	$0300	1-2,3-4,5-6,7-8,9-10,11-12	No Jumper between 13-14, 15-16
17	VDSPSCM			Channel # 1 -2
19	VDSPSCM			Channel # 3 -4
21	SPARE			User Slot

Table 3-1 VME Slot Assignments

4. HOST VMEbus ACCESS

Each VDSP431 module communicates with the VMEbus through a dual-access RAM and small number of registers located in A16 space. The dual-access RAM memory can be located in either A24 or A32 space. This memory is disabled at power-up and only the A16 registers are accessible by the VMEbus host processor. Each VDSP431 requires a different A16 address.

5. VDSP431 SHORT I/O ADDRESS

The VDSP431 supports Short I/O A16/D16, A24/D16 and A32/D32 VMEbus accesses. Following a power-on reset, only the A16 registers are accessible to the VMEbus. The VMEbus address of the A16 registers is determined by a set of jumpers. Once the A16 address has been set, software can program the starting address of the VDSP431 shared memory. The VDSP431 responds to both supervisory and non-privileged access. Each VDSP431 module occupies 256 Bytes in Short I/O space. Jumper **W2** sets the A16 address as shown below in **Table 5-1**:

VMEbus Address Line	Jumper W2	Off	On
A15	1-2	1	0
A14	3-4	1	0
A13	5-6	1	0
A12	7-8	1	0
A11	9-10	1	0
A10	11-12	1	0
A09	13-14	1	0
A08	15-16	1	0

Table 5-1 A16 Address Jumper W2

NOTE: When a jumper is not present the corresponding address line comparator is pulled-up to a logical “1”.

5.1 VDSP431 #1

VMEbus Address Line	Jumper W2
A15	1-2
A14	3-4
A13	5-6
A12	7-8
A11	9-10
A10	11-12
A09	13-14
A08	none

Table 5-2 A16 Address Jumper for VDSP431 #1

5.2 VDSP431 #2

VMEbus Address Line	Jumper W2
A15	1-2
A14	3-4
A13	5-6
A12	7-8
A11	9-10
A10	11-12
A09	**none**
A08	15-16

Table 5-3 A16 Address Jumper for VDSP431 #2

5.3 VDSP431 #3

VMEbus Address Line	Jumper W2
A15	1-2
A14	3-4
A13	5-6
A12	7-8
A11	9-10
A10	11-12
A09	**none**
A08	**none**

Table 5-4 A16 Address Jumper for VDSP431 #3

5.4 VME INTERRUPT SELECTION

The VDSP431 is able to generate an interrupt request to the VMEbus. The interrupt request level IRQ1-IRQ7 is determined by jumpers **W1** and **W3**. Using **Table 5-5** below, select the desired interrupt request level and set jumpers **W1** and **W3** accordingly.
IRQ 4 is the factory address setting.

Interrupt Level	W1 Jumper at location	W3 Jumper at location
IRQ 1	13-14	3-4, 5-6
IRQ 2	11-12	1-2, 5-6
IRQ 3	9-10	5-6
IRQ 4	**7-8**	**1-2, 3-4**
IRQ 5	5-6	3-4
IRQ 6	3-4	1-2
IRQ 7	1-2	none

Table 5-5 Interrupt Request Level Selection

5.5 FACTORY JUMPERS

All others jumpers located on VDSP431 module are set at the factory and should not be changed. The factory set jumpers are depicted in **Table 5-6** below:

JUMPER	SETTING	PURPOSE
W1,W3		See Above
W2		See Above
W5	3-4	SCANCLK use P2 VBUSY line
W6,W7, W8	none	Enable Mach 445 U48,U51,U65 to be programmed
W9	none	MCMP jumper selection
W10	none	85C36 port is selected as INPUT port
W11	2-3	Select EPROM size (27C0101A)
W12	none	RS422 Transmit port always enable
W13	2-3	RS422 port transmit RTS
W14	2-3	RS422 port receive CTS
W15	none	Jumper selection for 85C36 PortC to be input or output
P3	none	Probe input used to program the Mach 445
P4	none	Probe for the TMS320C31 emulator
P5	none	Remote Front Panel signals

Table 5-6

5.6 VDSP431 JUMPER LOCATION ILLUSTRATION

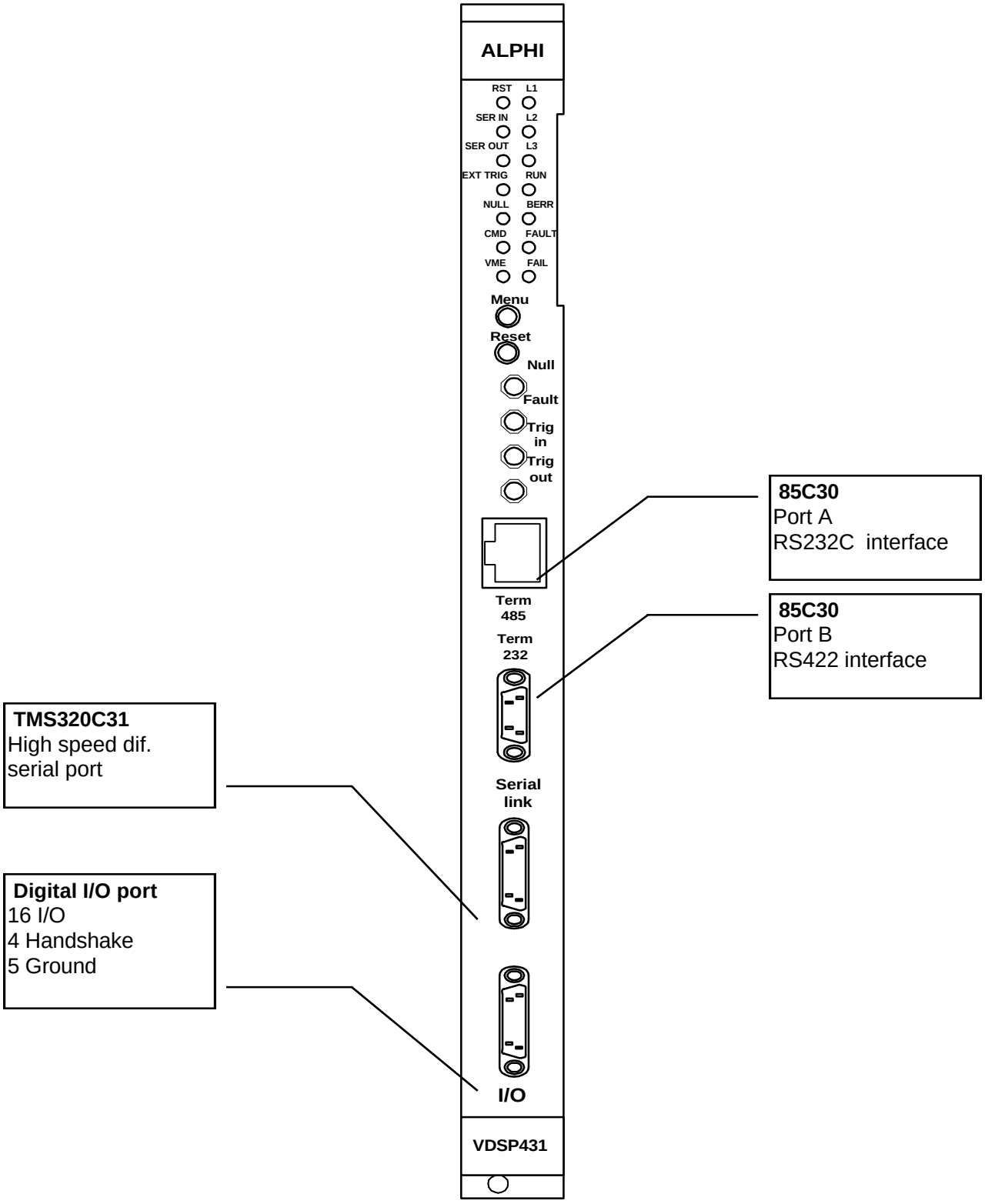


Figure 5-1

6. VDSPSCM

6.1 VDSPSCM Features

The VDSPSCM module is a slave carrier that is populated with :

- Two channel LVDT
- Two channel DC for strain gage
- Two VALVE driver channel
- Four A/D converter to digitize DC and AC parameters
- Up to 20 Digital I/O
- Four channel D/A monitor
- Two channel A/D used to monitor parameters as valve current....
- Calibration resistance
- DC/DC converter for analog circuit.

6.2 VDSPSCM BASE ADDRESS

A fully loaded VDSP431 system can support up to three (3) SCM modules connected together using a VSB backplane. Each VSB is identified using a set of three jumpers located on the back of each VSB SLOT. Slot “0” is normally reserved for the VSB controller , in this case the VDSP431 module. Using this identification every, SCM module recognizes its own location and will respond to the address placed on the P2 connector. Address decoding by the SCM modules is made by comparing the SLOT location identified with GA0-GA3 with the P2 address VSAD10 to VSAD12 which correspond to address LA08 to LA10 for the TMS320C31.

No jumpers need to be changed in order for the VDSP431 to be able to access the SCM modules.

6.3 OTHERS JUMPERS

Others Jumpers are factory installed and should not be changed.

Jumpers	Setting	Description
W1	1-2	Input voltage source for the DC/DC converter Input +5v
W2	3-4	SCANCLK use P2 line VBUSY* as clock
W3	none	VSB System Space
W4		Enable programming of the MACH 445
W5	none	85C36 Ports are selected as inputs
W6	none	Jumper selection for 85C36 Port C to be input or output
W7	none	Test Point
W8	2-3	OutMon #4 is routed to Mux A channel #8
W9	2-3	OutMon #3 is routed to Mux A channel #7
W10	2-3	OutMon #2 is routed to Mux A channel #8
W11	2-3	OutMon #1 is routed to Mux A channel #7
W12	none	Test point for OutMon #1
W13	none	Test point for OutMon #2
P3		Pod for MACH445 programming

6.4 FRONT PANEL LED's

Six Front Panels LED's provide information about the SCM modules status and health:

LED's	Description
L1	+5 V Power supply
L2	+ 12V Power supply
L3	- 12V Power supply
L4	+ 15V DC/DC converter
L5	- 15V DC/DC converter
L6	VDSP_SCAN module is accessed
L7	SCANCLK Active

Table 6-1 LED'S description

6.5 CALIBRATION RESISTANCE

This resistance is connected externally to EXCV- AND SIG- arms of the load cell. The resistance is switched 'On' by a relay activated via software. At reset, all of the relays are disabled. Calibration resistance values are typically 87.4KΩ +/- 1% and located on a socket. Users that want to use another calibration resistance value can short the internal resistance using the internal switch SW1. The new resistance will have to be connected externally.

SW1	OFF	ON
1-2	CALD = 87.4K	CALD = 0 SHORTED
3-4	CALC = 87.4K	CALC = 0 SHORTED
5-6	CALB = 87.4K	CALB = 0 SHORTED
7-8	CALA = 87.4K	CALA = 0 SHORTED

Table 6-2 SW1 disable switch

The firmware can detect the presence of the calibration resistance network.

7. DIGITAL INPUTS

An 8536 is used to provide up to 20 digital TTL Inputs / Outputs. These Digital I/O signals are made available on a Subminiature 25 Pin connector. Two groups of 8 channels can be selected as input or output by jumper. They correspond to Ports A and B of the 8536.

W5	NONE	INSTALLED
1-2	PA00- PA07 OUTPUT	PA00- PA07 INPUT
3-4	PB00-PB07 OUTPUT	PB00-PB07 INPUT

Table 7-1 I/O PINS

Four (4) other channels (Port C) can be selected separately as input or output by setting the jumpers:

W6	PC0	W6	PC0
1-3 2-4	INPUT	1-2 3-4	OUTPUT

Table 7-2

W6	PC1	W6	PC1
5-7 6-8	INPUT	5-6 7-8	OUTPUT

Table 7-3

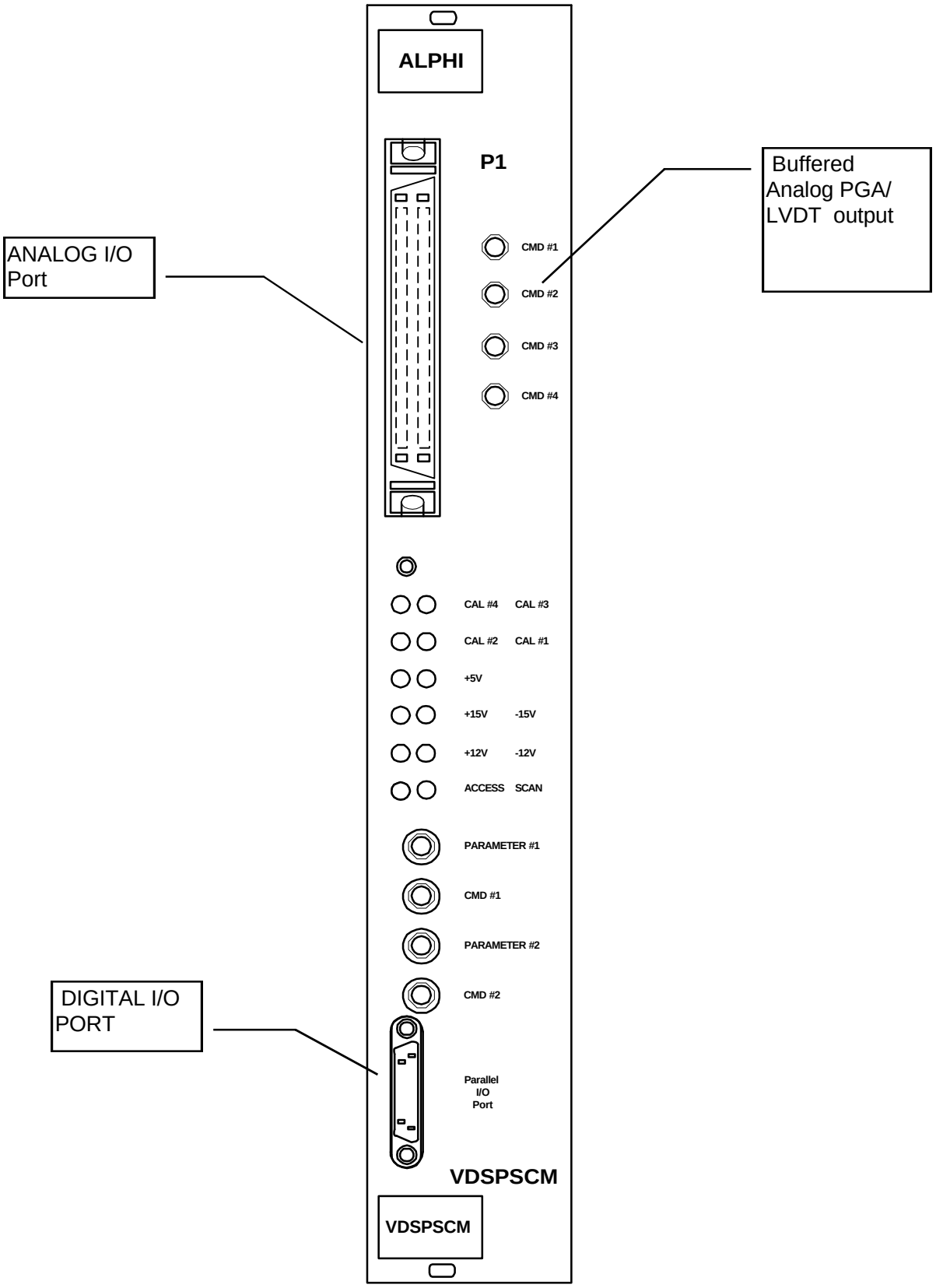
W6	PC2	W6	PC2
9-11 10-12	INPUT	9-10 11-12	OUTPUT

Table 7-4

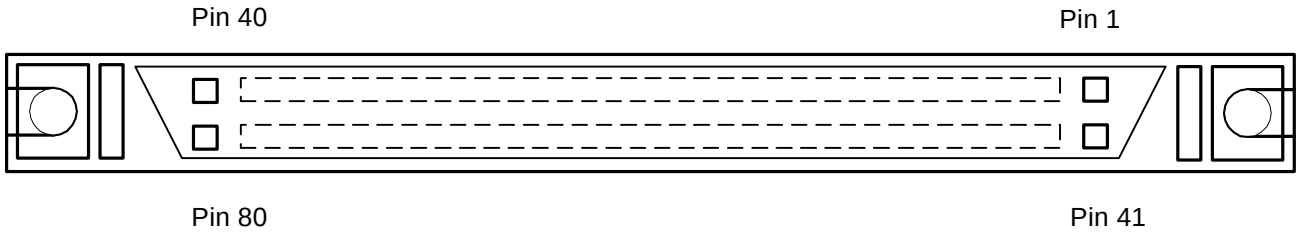
W6	PC3	W6	PC3
13-15 14-16	INPUT	13-14 15-16	OUTPUT

Table 7-5

8. SCM FRONT PANEL



8.1 PORT P1 CONNECTOR ORIENTATION



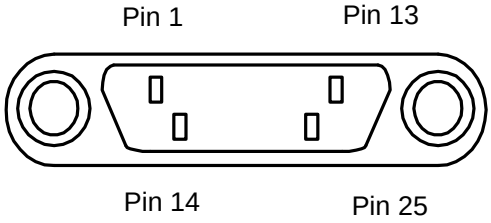
8.2 P1 CONNECTOR SIGNAL PINOUT

		P1		
Pin 1	I/O PC2		Pin 41	I/O PC3
Pin 2	I/O PC0		Pin 42	I/O PC1
Pin 3	GND		Pin 43	GND
Pin 4	Not Used		Pin 44	Not Used
Pin 5	CALA_I		Pin 45	CALA_O
Pin 6	EXSA+		Pin 46	EXSA-
Pin 7	EXA+		Pin 47	EXA-
Pin 8	GNDA		Pin 48	
Pin 9	CALB_I		Pin 49	CALB_O
Pin 10	EXSB+		Pin 50	EXSB-
Pin 11	EXB+		Pin 51	EXB-
Pin 12	GNDA		Pin 52	
Pin 13	CALC_I		Pin 53	CALC_O
Pin 14	EXSC+		Pin 54	EXSC-
Pin 15	EXC+		Pin 55	EXC-
Pin 16	GNDA		Pin 56	
Pin 17	CALD_I		Pin 57	CALD_O
Pin 18	EXSD+		Pin 58	EXSD-
Pin 19	EXD+		Pin 59	EXD-
Pin 20	GNDA		Pin 60	
Pin 21	GNDA		Pin 61	GNDA
Pin 22	OUTMON#2		Pin 62	OUTMON#4
Pin 23	OUTMON#1		Pin 63	OUTMON#3
Pin 24	GNDA		Pin 64	GNDA
Pin 25	PGOUTSC		Pin 65	PGOUTSD
Pin 26	PGOUTSA		Pin 66	PGOUTSB
Pin 27	VALVED+		Pin 67	VALVED-
Pin 28	GND_VDC		Pin 68	GND_VDD
Pin 29	VALVEC+		Pin 69	VALVEC-
Pin 30	VALVEB+		Pin 70	VALVEB-
Pin 31	GND_VDA		Pin 71	GND_VDB
Pin 32	VALVEA+		Pin 72	VALVEA-
Pin 33	GUARDD		Pin 73	GNDA
Pin 34	IND-		Pin 74	IND+
Pin 35	GUARDC		Pin 75	GNDA
Pin 36	INC-		Pin 76	INC+
Pin 37	GUARDB		Pin 77	GNDA
Pin 38	INB-		Pin 78	INB+
Pin 39	GUARDA		Pin 79	GNDA
Pin 40	INA-		Pin 80	INA+

Table 8-6 Pinout connector

8.3 I/O DIGITAL PORT

The I/O DIGITAL port uses a 25 Pin Subminiature female connector



	PIN		PIN		PIN
Pin 1	PA07	Pin 10	PB00	Pin 19	PB07
Pin 2	PA05	Pin 11	Not used	Pin 20	PB05
Pin 3	PA03	Pin 12	FP_PC2	Pin 21	PB03
Pin 4	PA01	Pin 13	FP_PC0	Pin 22	PB01
Pin 5	GND	Pin 14	PA06	Pin 23	GND
Pin 6	GND	Pin 15	PA04	Pin 24	FP_PC3
Pin 7	PB06	Pin 16	PA02	Pin 25	FP_PC1
Pin 8	PB04	Pin 17	PA00		
Pin 9	PB02	Pin 18	Not used		

Table 8-7 I/O Port

9. VDSP431 I/O INTERFACE RACK

The VDSP431 I/O Interface rack is use to connect each SCM signal to and from the “outside world”. For each SCM, a transition module is use to route the signals from the 80 Pin connector to a screw terminal interface. From there, Bendix round connectors are pre-wired to match the interface between the signal source and the transition module. Each VDSP431 I/O Interface is custom designed to match customer requirements.

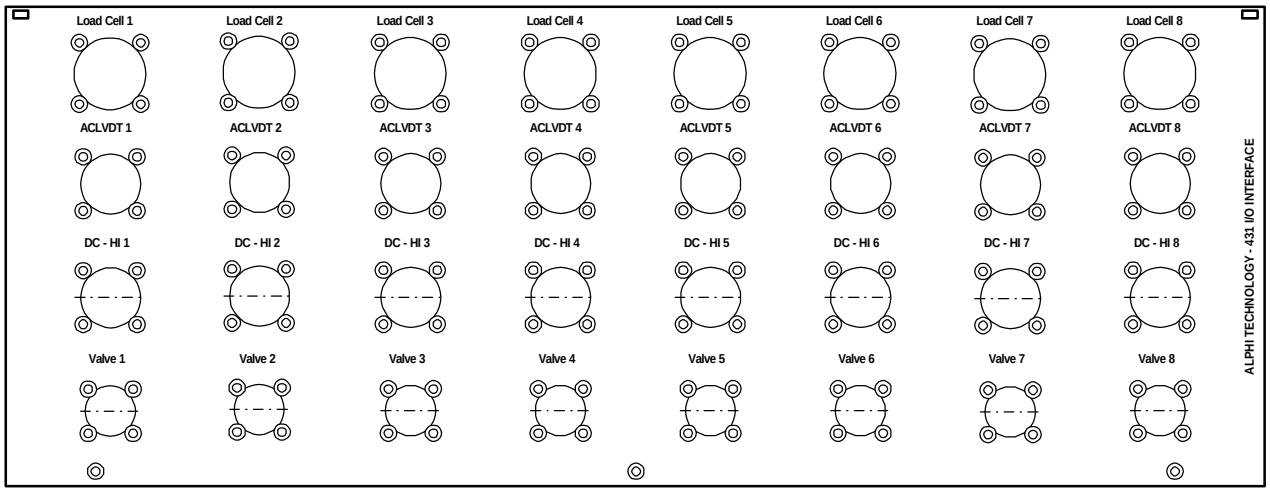


Figure 9-1 I/O RACK