IP
FPGA- 4020

IP MODULE
FPGA

HARDWARE REFERENCE MANUAL

Revision 1.5
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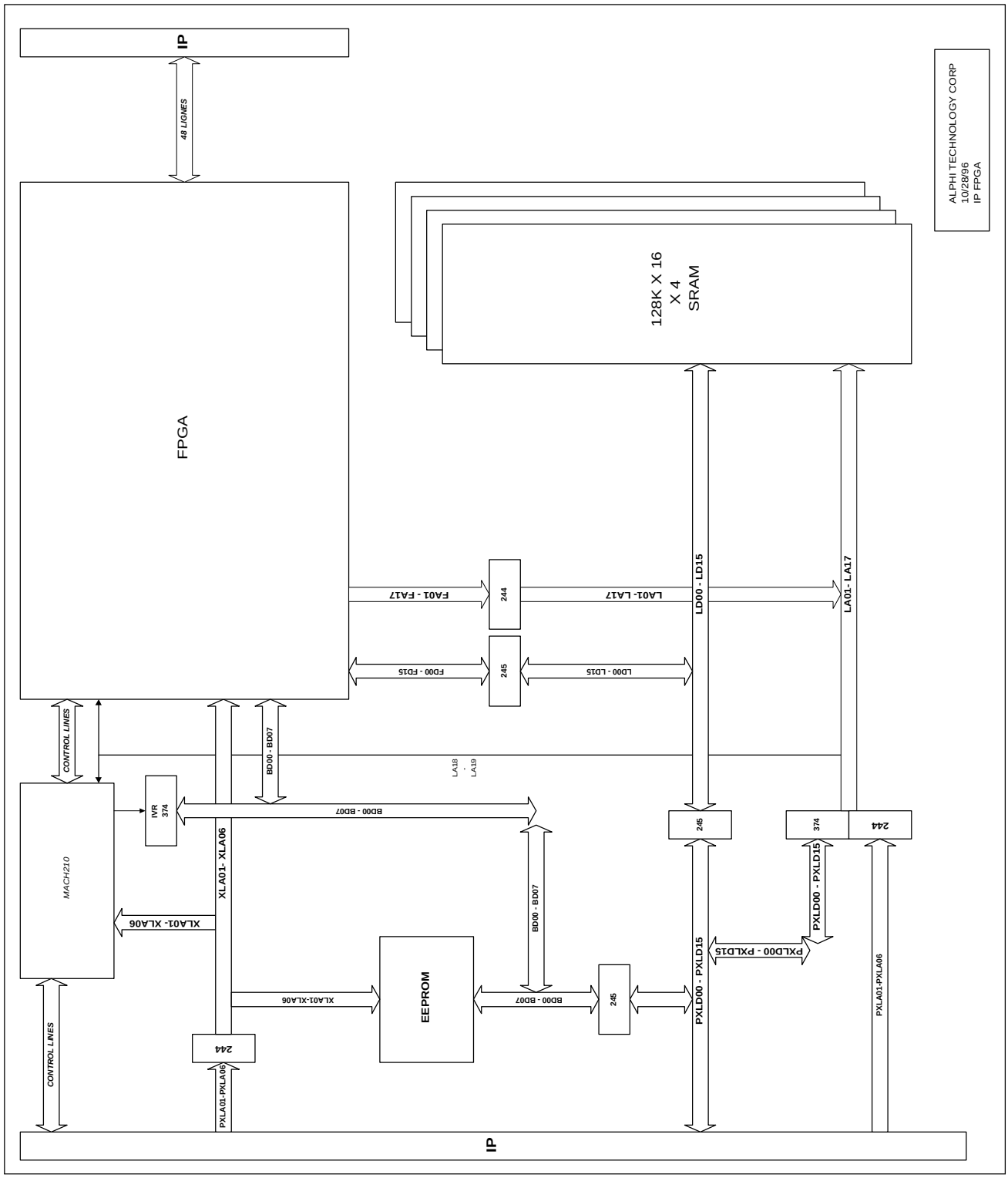
1. Introduction

1.1 Functional description

The IP_FPGA module board is designed around the FPGA XC4020 from XILINX. Key Features are:

- Up to 42 I/O Pin available
- UP TO 2Mbytes of SRAM
- Power supply pin with fuse protection available

1.2 Block diagram



2. MAP ADDRESS

The IP_FPGA module use the three available space defined in the Industries Pack specifications.

2.1 IDSPACE

A EEPROM that occupies 64 address space provide information about the module to the User. The lower address contains data related to the type of module, revision, etc. ..
The Upper space can be used to store some information. Only ODD address are valid.
Each IP to conform to the IP Bus Specification has 32 byte of EEPROM that can be read by the local Host to identifies the IP module Manufacturer, type , revision,etc.
Base Address is located in the IP IDENTification Base address. The IP-Summit has in reality 128 Bytes that are not protected.

ID space address	Description	Value
$01	Ascii “I”	$49
$03	Ascii “P”	$50
$05	Ascii “A”	$41
$07	Ascii “C”	$43
$09	Manufacturer identification	$99
$0B	Module type	
$0D	Revision module	
$0F	Reserved	$00
$11	Driver ID,low byte	
$13	Driver ID,high byte	
$15	Number of bytes used	$0C
$17	CRC	
$19-$3F	User space	

Table 2-1 EEPROM byte content

Address $01-$07 identifies “IPAC” .Also this identifies the EEprom beginning.
The EEprom is not protected against write.

2.2 IOSPACE

IP_FPGA use the IOSPACE for the following :

2.2.1 Control Register

Base address IOSPACE + $00 word access *Write only* BD00-BD01

BD00 is cleared on reset . It controls the Input line PROGRAM from the XILINX. It is used to initiate the Programation of the XILINX chip.

BD01 can be used to initiate a READ_Back of the contents of the XILINX memory and node .

2.2.2 Status Register

Base address IOSPACE + $02 Word access *Read only* BD00-BD07

The data read are the image inverted of the signals described below.
A "1" read means the signal input is Low.
A "0" read means the signal input is High.

Bit	NAME	Description
BD00	RDY/BUSY	Status of the FPGA when using the Asynchronous peripheral Mode
BD01	RDBK_P	I/O line from FPGA programs to inform the read is in progress
BD02	Disable	Status of the FPGA output line use to tri-state the Lattice ispLSI 1016 signals.
BD03	XCM1	Status of Jumper use to select Programation Mode
BD04	XCM0-2	Status of Jumper use to select Programation Mode
BD05	FPGA_INT	When low the FPGA has an Interrupt pending
BD06	INIT	Status of FPGA when in program mode
BD07	DONE	When high Programation is complete and successful

Table 2-2 Status Register

2.2.3 IVR Interrupt Vector Register

This eight bit register located at address IOSPACE + $04 Word access can be read and write by the Carrier module. The vector is automatically furnished when the INTSPACE is accessed by the Carrier. The FPGA controls the opening of the IVR if it is the source of an interrupt.

2.2.4 FPGA

The FPGA can be programmed in asynchronous mode by writing at the address IOSPACE + $06 word access BD00-BD07 are used. The programation is made in byte to an internal parallel to serial register that will convert the byte in a serial stream.

2.3 INTSPACE

When the FPGA has an interrupt pending the Carrier module can read the IVR register that has been program early by the carrier.

2.4 SRAM

Four (4) banks of 128k x 16 bit (1 Mbytes) SRAM is available to the User.
The SRAM can be accessed through the IP interface using the Memory space or by the FPGA.
Programation of the FPGA must be made using I/O lines.
Dual access can be made but the arbitration will have to be made by the FPGA.
The line Disable can be use to control the Lattice chip.

2.5 SRAM INTERCONNECTION WITH FPGA

SRAM ADDRESS	FPGA PIN		SRAM DATA	FPGA PIN
LA01	89		LD00	118
LA02	88		LD01	120
LA03	87		LD02	121
LA04	86		LD03	124
LA05	85		LD04	125
LA06	84		LD05	126
LA07	83		LD06	127
LA08	82		LD07	129

LA09	81		LD08	134
LA10	80		LD09	135
LA11	76		LD10	136
LA12	75		LD11	137
LA13	74		LD12	139
LA14	73		LD13	140
LA15	72		LD14	141
LA16	71		LD15	143
LA17	70			

Table 2-3 SRAM to FPGA connection

2.6 SRAM CONTROL LINES FROM FPGA

These signals can be active only if the Lattice pal is disable .

SRAM LINE	FPGA PIN	NOTE
MCS0*	145	Enable First bank 128k X 16 SRAM
MCS1*	144	Enable Secund bank 128k X 16 SRAM
MWR0*	163	Write signal to the SRAM
MCS2*	150	Enable Third bank 128k X 16 SRAM
MCS3*	146	Enable Fourth bank 128k X 16 SRAM
MRD*	149	Read for SRAM
LA18	167	Address LA18
LA19	164	Address LA19
FAEN*	97	When low enable data and address buffer between SRAM and FPGA

Table 2-4 Sram Control lines

2.7 FPGA TO IP BUS CONNECTION

IP BUS LINE	FPGA PIN	NOTE
ACKAH	7	This signal can be active as output high only if the lattice is disable
MEMSEL0*	10	Memory space selection
IOSELA*	11	Iospace selection
BDS1*	12	Upper byte
BDS0*	13	Lower byte
RESET*	111	Ip reset
DMAENDH	193	Connection to IP bus through open drain Output
PDMAEND*	187	Input DMAend from IPbus
DMAREQ*	188	This Output Signal Is Buffered
DMACK*	192	DMA acknowledge from IP carrier
IPRW*	112	Read Write signal from IPbus
INTSELA*	166	IP carrier respond to an Interrupt
INTREQ0*	174	IP FPGA generates an Interrupt
INTRD*	115	When low enable IVR (Interrupt Vector Register) read
INTWR*	116	Write to the IVR
BEN*	172	Low enable address and data bus for IPbus to access SRAM
LACHAD	178	A raising edge during MEMSELO active (low) latch the address

Table 2-5 FPGA to IP connector

3. Jumpers

JUMPER	FACTORY SETTING	DESCRIPTION
W1	none	Select the FPGA programation mode
W3	none	Select the Master or Slave programation mode
W2	1-2	Select the use of the pin 151 from FPGA as DIN serial input when using the pod for programmation or BD00 when using Asynchronous mode

Table 3-1 Jumper factory setting

3.1 JUMPERS

3.1.1 W1

This jumper selects the Programation mode of the XILINX. Three input pins define the mode at the level of the XILINX. Two of these pins XCM0 and XCM2 are connected together. When there is a jumper the signal is grounded.

XCM1	XCM0-2	Mode
none	none	***Slave serial mode.*** The external Pod connected to J2 is used for programmation. Jumper W2 must be set between 1-2. Jumper W3 have no jumper.
1-2	3-4	***Master serial mode.*** This mode allows on power_up to have the XILINX reading the Data automatically from the Serial EEPROM. Jumper W2 must be set between 1-2. The signal done automatically disconnects the Program signal. Jumper W3 must be set between 1-2.
1-2	none	***Asynchronous peripheral mode.*** The FPGA is programmed through the IP bus at the address IOSPACE +$06. Jumper W3 must be set between 1-2 Jumper W2 must be set between 2-3
		OTHERS MODE ARE NOT ALLOWED

Table 3-2 W1 Programmation mode selection

3.1.2 W3

This jumper is used to control the behavior of the PROG line of the FPGA.
The line Prog is the image of the signal Done clocked by CCLK clock.

MODE	Jumper	Description
Slave serial	none	The XILINX pod provide the signal
Master serial	1-2	Upon reset the signal is low, the FPGA generate the CCLK to read the Serial EEPROM. When the programation is finished the signal Done from the FPGA de_asserts the signal Prog.
Asynchronous peripheral	1-2	Upon reset the signal is controlled by the IP carrier. the bit #0 of the Control register is used to assert the signal Prog.

Table 3-3 W3 Programmation mode selection

3.1.3 W2

The jumper is used to connect the I/O pin “D0, Din” of the FPGA to BD00 ,the local bus signal or DIN the Serial input data.

MODE	Jumper	Description
Slave serial	1-2	The XILINX pod provide the Din signal
Master serial	1-2	Upon reset the signal is low, the FPGA generate the CCLK to read the Serial EEPROM. The data from the EEPROM are sent to the FPGA through the DIN pin.
Asynchronous peripheral	2-3	The Carrier programs the FPGA in byte. The Bus line BD00 must be connected to the input “D0, DIN” of the FPGA.

Table 3-4 W2 Programmation mode selection

4. Connectors

4.1 I/O Port

		P4		
Pin 1	I/O 00		Pin 26	I/O 01
Pin 2	I/O 02		Pin 27	I/O 03
Pin 3	I/O 04		Pin 28	I/O 05
Pin 4	I/O 06		Pin 29	I/O 07
Pin 5	I/O 08		Pin 30	I/O 09
Pin 6	I/O 10		Pin 31	I/O 11
Pin 7	I/O 12		Pin 32	I/O 13
Pin 8	I/O 14		Pin 33	I/O 15
Pin 9	I/O 16		Pin 34	I/O 17
Pin 10	I/O 18		Pin 35	I/O 19
Pin 11	I/O 20		Pin 36	I/O 21
Pin 12	I/O 22		Pin 37	I/O 23
Pin 13	I/O 24		Pin 38	I/O 25
Pin 14	I/O 26		Pin 39	I/O 27
Pin 15	I/O 28		Pin 40	I/O 29
Pin 16	I/O 30		Pin 41	I/O 31
Pin 17	IPC50-32		Pin 42	IPC50-33
Pin 18	IPC50-34		Pin 43	IPC50-35
Pin 19	IPC50-36		Pin 44	IPC50-37
Pin 20	IPC50-38		Pin 45	IPC50-39
Pin 21	IPC50-40		Pin 46	IPC50-41
Pin 22	IPCLK		Pin 47	IPRESET
Pin 23	+12V		Pin 48	-12V
Pin 24	+5		Pin 49	+5
Pin 25	GND		Pin 50	GND

Table 4-1 IP connector I/O

4.2 FPGA

4.2.1 Boundary Scan

The FPGA has Boundary Scan capabilities. Connector J1 provide the interface with the XILINX chip.

J1 Pin	Signal
Pin 1	TDI
Pin2	TDO
Pin3	TCK
Pin4	TMS
Pin5	GND
Pin6	N.C.
Pin7	N.C.
Pin8	DOUT

Table 4-2 Boundary scan probe

4.2.2 Programation Pod

Slave Serial programmation use connector J2 for programmation. Jumper W3 should have no Jumper.

J2 Pin	Signal
Pin 1	+5
Pin2	GND
Pin3	N.C.
Pin4	CCLK
Pin5	DONE
Pin6	DIN
Pin7	INIT
Pin8	PROG

Table 4-3 Serial mode probe

4.3 Lattice pod

This pod is use to program the Lattice ISPL1016 at factory. It is not available to the user.

5. TIMING

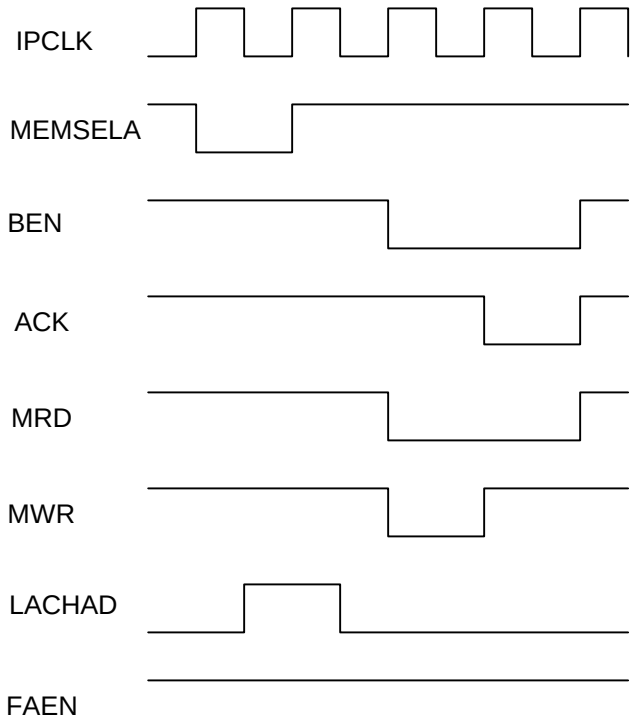


Figure 1 Timing

6. SERIAL EPROM

XLINX XC4020E need a 17256DP8C and a 17128DP8C serial eprom.

