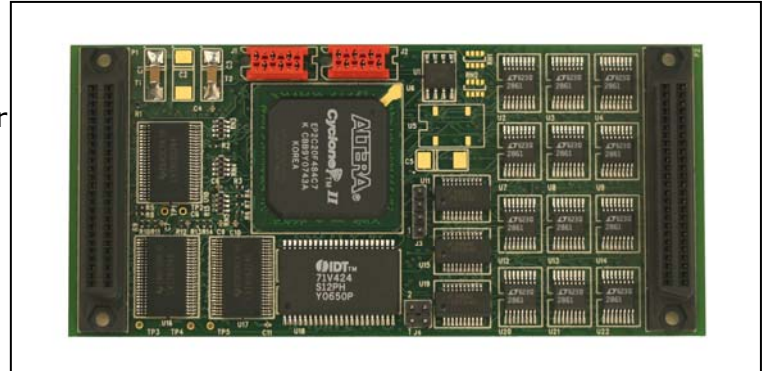


IP Cyclone FPGA with RS485/RS422/TTL Parallel I/O

Features

- Single wide industry pack board format
- Altera FPGA EP2C20 or EP2C50
- Up to 24xRS485 or RS422 driver/receiver (LTC2861) or TTL input/output lines
- Each line can be separately selected as input or output
- Programmable in groups of 4 I/O
- 100Ω terminating resistor or no resistor for RS485/RS422 I/O, resistor software selectable using LTC2861 switch
- Up to 512K x 8 x 2 dual ported SRAM
- MAX 3128 timing device for IP bus, DPR bus, and FLEX device access
- 8 or 32 MHz clock
- Optional user clock on board running at different speed than IP bus
- 2 interrupts and 2 slave DMA IP bus lines
- FPGA programmable through JTAG header, onboard serial EPROM, or through IP bus
- VITA 4 compliant



Block Diagram Overview

The IP-CYCLONEII-PIO module is an IP mezzanine card that is populated with an Altera Cyclone II embedded programmable FPGA. Two different sized FPGA's can be selected. A dual ported SRAM can be accessed by either some form of CPU/DSP on the IP bus side and/or the ALTERA Cyclone FPGA. The I/O can be either RS485/RS422 or TTL in groups of 4 I/O.

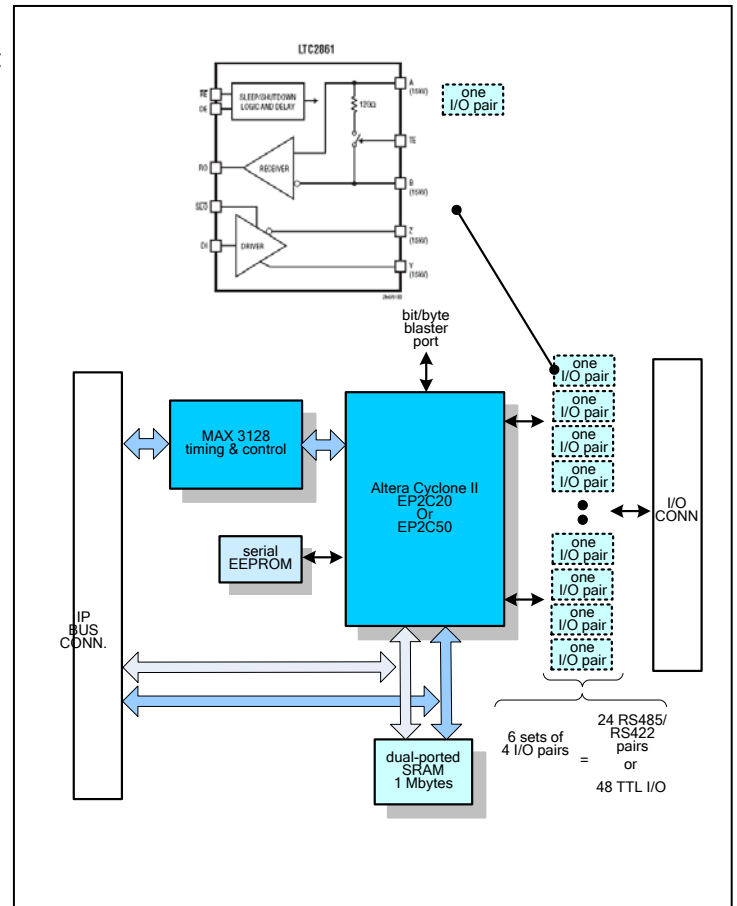
Available Software Drivers:

The customer must have an Altera development tool to implement their own FPGA design.

The IP module can be used as a stand-alone module.

The FPGA's program can be downloaded in one of three ways:

- JTAG header connector connected directly to the FPGA, or
- Local serial EPROM, or
- Through the IP bus.



Applications:

The IP-CYCLONE II-PIO can be used as a RS485/RS422 bus I/O interface for parallel and/or serial communications between carrier systems or simply used as a TTL I/O subsystem for monitoring and/or controlling digitally oriented functions.

The FPGA can be programmed through the Blaster interface for quick design turnaround. The local serial EPROM can be used for local programming. The FPGA can also be programmed by downloading the entire program into the FPGA from the IP bus for those applications that require complete security.

LTC2861 - 20Mbps RS485 Transceivers with Integrated Switchable Termination1

- 20 Mbps Max Data Rate
- No Damage or Latchup to ESD: ±15kV HBM
- High Input Impedance Supports 256 Nodes
- 250kbps Low-EMI Mode Full duplex
- Guaranteed Failsafe Receiver Operation Over the Entire Common Mode Range
- Current Limited Drivers and Thermal Shutdown
- Delayed Micropower Shutdown (5µA Max)
- Low Operating Current (900µA Max in Receive Mode)

I/O Features (TTL mode):

- 24 pair RS-422/485 or 48 TTL or combination
- High Input Impedance-Supports 256 nodes
- Software selectable Half-Full Duplex
- Enhanced ESD protection allows to withstand ±15 KV
- Logic-Selectable 120Ω Termination Resistor

Industry Pack Specifications:

- Meets ANSI/VITA 4-1995
- 8/32 MHz synchronous operation
- Supports ID, 128 byte I/O, interrupt. & 8 Mbyte memory spaces
- 2 Interrupts per module
- Two passive DMA channels are possible.
- Hardware self timed per IP module
- Triggered via system reset and software control
- Jumper or software time-out function
- 5, +/-12 volt reset-able fuse per IP

Mechanical: Environmental:

- Size – VITA 4 compliant
1.8" x 3.9" or 46 mm x 99 mm
- Power – 1.0 watt
- Vibration – 0.5G, 20-2000 Hz rand
- Shock – 20G, 11 msec, ½ sine
- Weight – 3 ounces
- MTBF – >250,000 hours

Operating Environment:

- Operating temperature
Commercial: 0 to +70 °C
Optional: -25 °C to +80 °C
- Non-operating: -40 °C to +85 °C
- Airflow requirement – 5 CFM
- Humidity – 5 to 90% (non-cond)
- Altitude – 0 to 10,000 feet



Ordering Information:

Part Number : IP-Cyclone II-C20 - PIO RS-485/422 ALTERA EP2C20Industry Pack module
 IP-Cyclone II-C50 - PIO RS-485/422 ALTERA EP2520Industry Pack module

Optional Accessories

Part Number : TB-50-HDR 50 pin terminal block and 1meter flat ribbon cable
 Part Number : CBL-50-HDR 50 pin,1meter flat ribbon cable, IDC header connector