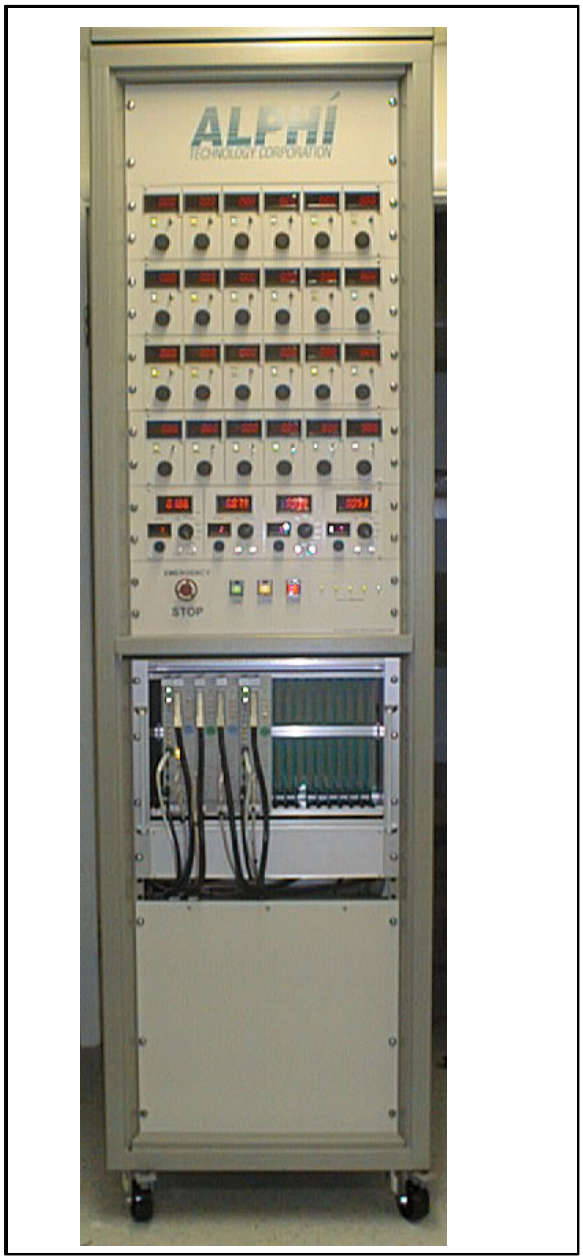
ADM-96S AND ADM-48D HIGH PERFORMANCE DATA ACQUISITION SYSTEMS



ADM-96S DATA ACQUISITION SYSTEM

KEY FEATURES

- Up to 96 Single Ended Input (ADM-96S)
- Up to 48 Differential Input (ADM-48D)
- 16 bit Resolution
- 100 KSPS per channel
- 200 KSPS per channel: interleave mode
- Simultaneous Sampling on all channels
- +/-10 Volt input voltage
- Over-voltage protection up to +/-25V
- Up to 9.6 Msamples/S throughput
- 8 programmable scanning timers
- External and internal scan trigger
- External and internal gate signal
- Full VME master/slave capabilities
- VMEbus Rev C compatible
- 68EC030 processor
- VIC068/VAC068 VME interface chipset will support both master and slave DMA transfers
- Up to 6 Mbytes of dual-ported SRAM for analog to digital converted data
- Up to 128 Kbytes of dual-ported SRAM for communication between a VME host and the local **ADM31** processor
- 512 Kbytes of EPROM
- 64 Kbytes of EEPROM for non-volatile system configuration information and calibration
- One external RS-232C serial port interface and one external 25-pin parallel port PC compatible interface available from the front panel.
- ADM-96S occupies 2 or 3 VME slots

6202 South Maple Ave., Suite 120 Tempe, Arizona 85283
PHONE (602) 838-2428 FAX (602) 838-4477 email: info@alphitech.com

500-1-0-4100 REV.A

GENERAL DESCRIPTION

The VME-based **ADM96S** and **ADM48D** data acquisition systems supports up to 96 single-ended analog inputs or up to 48 differential analog inputs.

ADM31 OPERATION

The **ADM31** control card is an intelligent A/D subsystem master or slave device that controls the analog A/D cards. Up to two A/D cards can be configured with the control card to complete the A/D system. See **Figure 1** below for the various card combinations available for a data acquisition system.

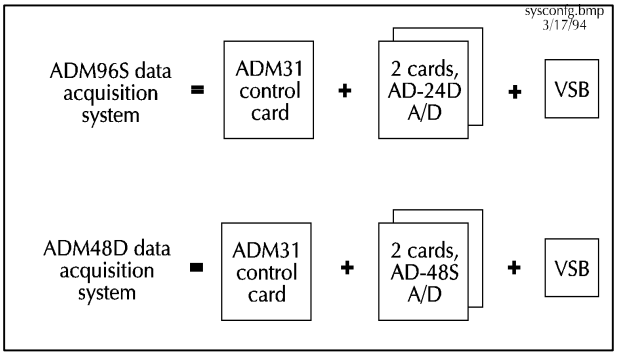


Figure 1. Data Acquisition System Configurations.

The **ADM31** control card can be configured to:

- Operate as a master system controller or slave in a VME card cage, and
- Be controlled by an external PC in terminal mode through the front panel serial port with PC-based data display information available through the parallel I/O port also on the front panel.

ADM31 Control Local Resources

The block diagram for the ADM31 control card is found in **Figure 2**. The **ADM31** control card's resources include:

- MC68EC030 microprocessor,
- VIC and VAC VME interface chips,
- EEPROM,
- EPROM,
- SRAM for data acquisition storage,
- SRAM memory communication,
- SRAM for channel data list,
- Timers for data acquisition control,
- Scan-clock Trigger
- An RS232C serial port, and
- A LPT1 compatible parallel port.

Processor

The **ADM31** base board module use a high performance MC68EC030 32-bit processor that handles communication with the VME host and initiates data transfers on the VME bus. The 68EC030 in conjunction with the VIC068 and VAC068 support chips, facilitate stand-alone operation as a VME bus master or as an intelligent slave device.

VIC/VAC VMEbus Interface

The **ADM31** module uses the VIC068 and VAC068 to provide an interface between the VMEbus and local busses. These two industry standard products provide maximum performance for a VMEbus master/slave module.

EEPROM

The 64 Kbytes of EEPROM are used to store system parameters in non-volatile memory.

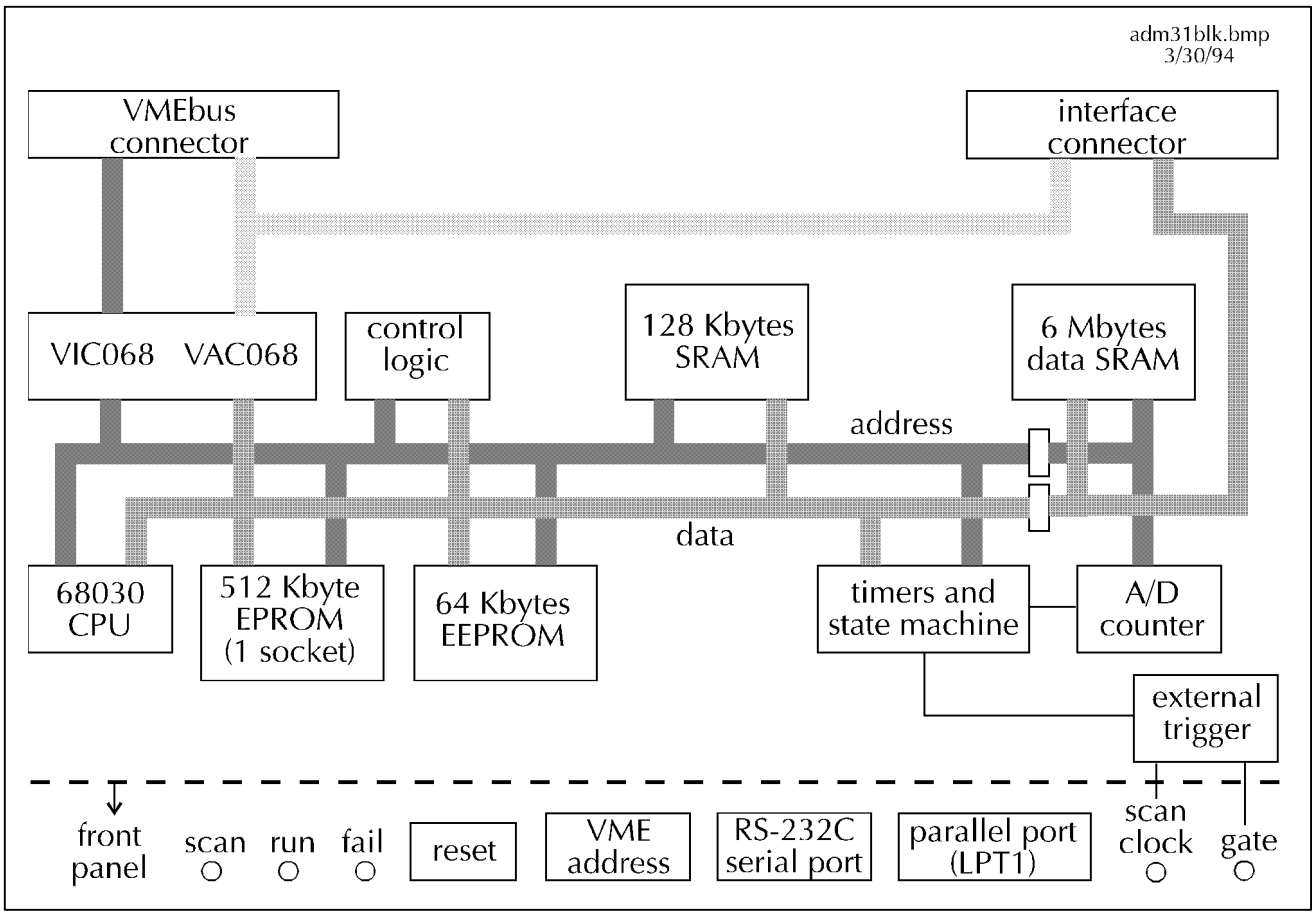


Figure 2. ADM31 Control Card Block Diagram.

ADM31 CONTROL CARD

EPROM

Up to 512 Kbytes of EPROM are used for the control card's independent operation. A part of the EPROM memory space is used to store the scanning and system data acquisition software

Data SRAM

Up to 6 Mbytes of SRAM is used as a buffer for digitally converted sample data from the A/D subsystem. The converted data is temporarily stored in data SRAM for local VME master interrogation or external PC display.

Host Communication SRAM

The **ADM31** module contains a 128 Kbytes dual ported SRAM which is shared by the VMEbus and the local 68EC030 processor. This memory is mapped to a user defined space on the VMEbus. The 68EC030 uses this memory for program storage and to process information downloaded from the VME host

Channel SRAM

2 Kbytes of SRAM is used for temporary storage of channel identification. The hardware-based state machine after activation by a trigger source uses the channel pointers for data acquisition and control of the A/D subsystem.

TIMERS

Eight 16 bits timers allow the user to select up to eight different sample clock rates in 65536 steps. Each channel can be connected to one of the eight timers.

Scan Clock

An external clock reference, routed from the front panel, provides external trigger support. The external trigger is TTL differential with programmable active edge. Internal or external trigger operation is defined by software.

Gate Signal

The GATE signal provides a Start/Stop for the external Scanclock. This external GATE signal is TTL differential. Internal or external GATE operation is defined by software.

Serial Port

A 6-pin RJ-11 RS232C serial port is available for external PC-based control and monitoring.

Parallel Port

A 25-pin parallel port is available for external PC-based data acquisition. This parallel port is LPT1 compatible.

AD-48S AND AD-24D OPERATION

The analog input signals are synchronously sampled and held upon reception of the SCANCLK signal. The conversion is also made concurrently upon reception of a trigger single provided by the **ADM31**. After conversion is finished, the ADM31 scans
the activated list and stores the activated channel data into the data RAM. **See Figure 3** for a block diagram of the **AD-24D** card and **Figure 4** for a block diagram of AD-48s card.

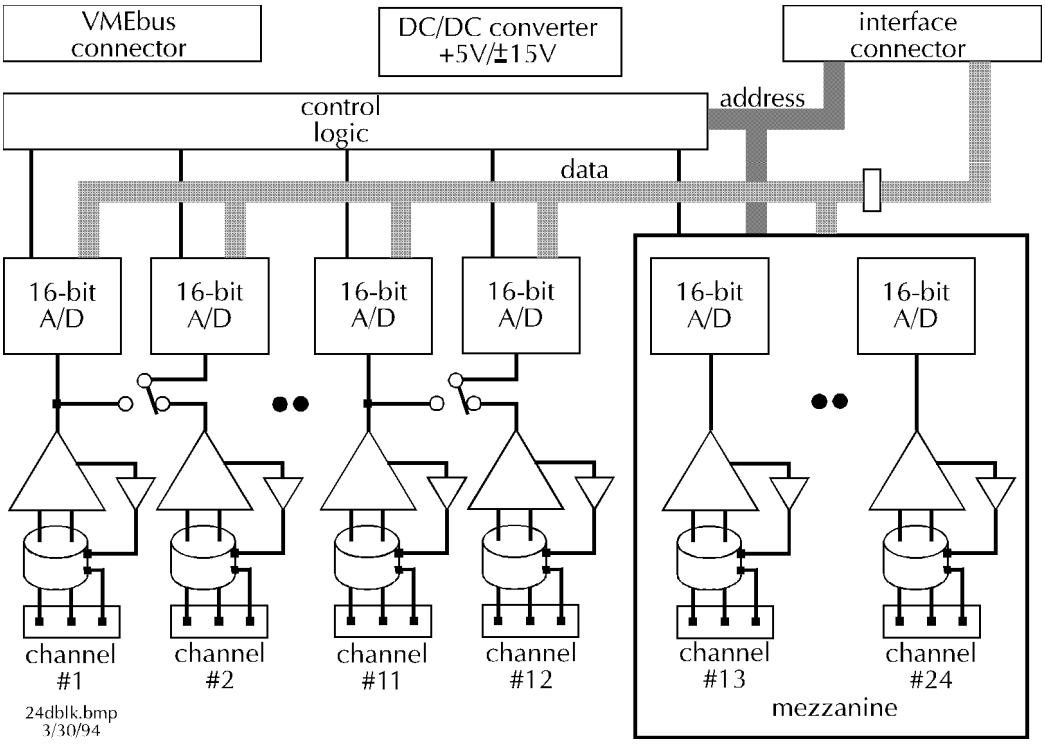


Figure 3. **AD-24D** Block Diagram.

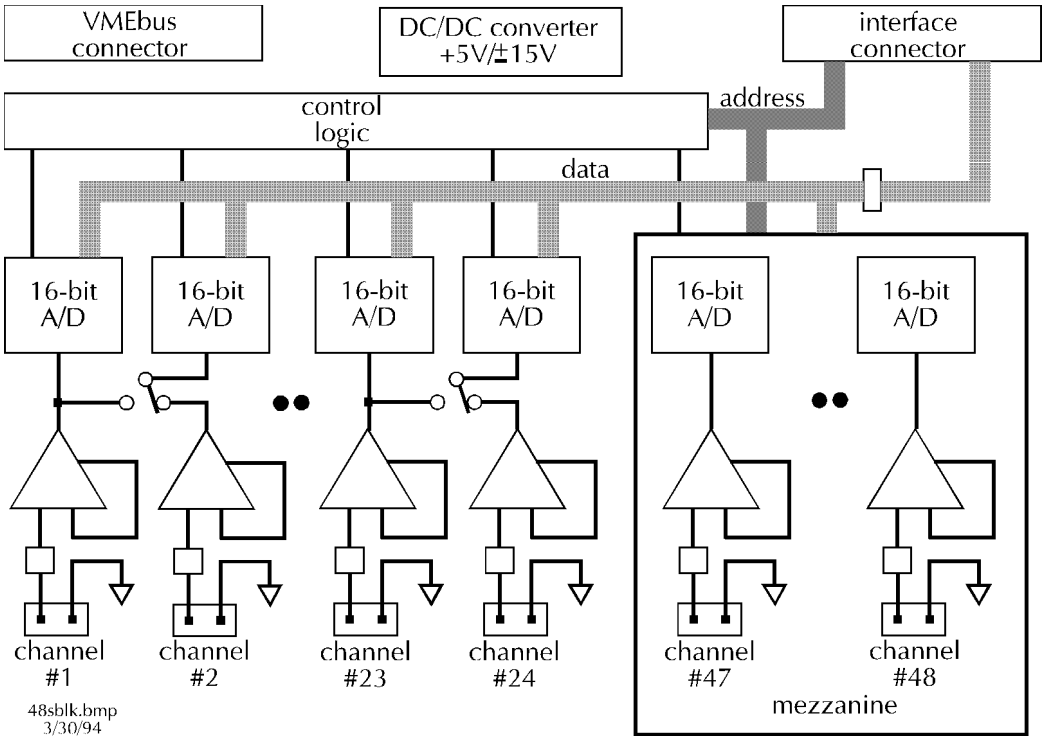


Figure 4. **AD-48S** Block Diagram.

MODULE SYSTEM SPECIFICATIONS

Specifications for the data acquisition system are broken into two parts - **Table 1** includes the **ADM31** CPU control card, **Table 2** includes the **AD-24D** differential A/D card and the **AD-48S** single-ended A/D card.

Characteristics	Specifications
microprocessor	68EC030, up to 32 MHz
system memory (master or slave) extended access	A32/D08 (OE) A32/D16 A32/D32, A32/D32 BLT, A32 /D32 UAT
standard access	A24/D08 (OE) A24/D16 A24/D32, A24/D32 BLT, A24/D32 UAT
memory size capability EPROM data SRAM channel SRAM EEPROM host/control SRAM	 up to 512 Kbytes up to 6 Mbytes 2K bytes up to 64 Kbytes up to 128 Kbytes
indicators	scan run fail
operators	ABT (abort) RST (reset)
operating temperature	0° C to +50° C
storage temperature	-20° C to +80° C
operating humidity	90% non-condensing
power requirements	+5 VDC, 1.9 A
physical characteristics board dimensions front panel	double height VME board with front panel 9.32 inches (233 mm) 6.4 inches (160 mm) 10.48 inches (262 mm) 0.8 inches (20 mm)

Table 1. **ADM31** Control Card Specifications.

Characteristics	AD-24D Specifications	AD-48S Specifications
number of A/D channels	24 channels with 24 A/D's	48 channels with 48 A/D's
type of A/D channel	true differential	single-ended
acquisition time	10 microseconds	10 microseconds
sampling rate	200 Ksamples/sec interleaved	200 Ksamples/sec interleaved
input capacitance	< 70 pF	< 70 pF
resolution	16 bits	16 bits
quantization error	± .5 LSB	± .5 LSB
integral non linearity	± 0.005% FSR maximum	± 0.005% FSR maximum
overvoltage protection	± 25 V	± 25 V
type of code output	no missing codes, binary 2's complement	no missing codes, binary 2's complement
channel-to-channel crosstalk	>96 dB at ± 10 V	-
slew rate	13 V/microsecond min.	-
common mode rejection	>80 dB typical	-
common mode voltage	± 10 V minimum	-
low bias current	± 2 pA typical, ± 20 pA maximum at 25 °C	< 20 pA
input impedance	> 10 GΩ (limited to 10 MΩ by resistor)	> 10 GΩ (limited to 10 MΩ by resistor)
temperature range	0° C to +50° C	0° C to +50° C
storage temperature	-20° C to +80° C	-20° C to +80° C
operating humidity	90% non-condensing	90% non-condensing
power requirements	+5 VDC, 4.8 A	+5 VDC, 4.8 A
physical characteristics	double height VME board	double height VME board
board dimensions	9.32 inches (233 mm) 6.4 inches (160 mm)	9.32 inches (233 mm) 6.4 inches (160 mm)
front panel	10.48 inches (262 mm) 0.8 inches (20 mm)	10.48 inches (262 mm) 0.8 inches (20 mm)

Table 2. **AD-24D** / **AD-48S** A/D Card Specifications.

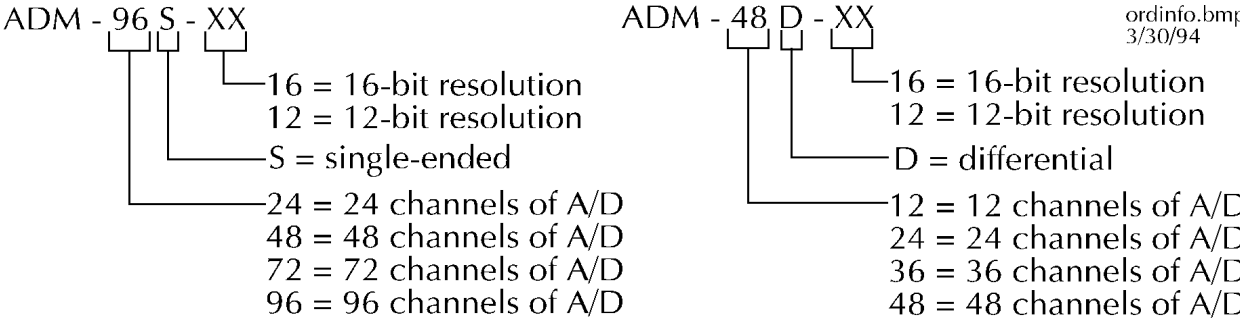
FIMWARE

On board Firmware allows under VME Host or PC control:

- Data download in a slave or master mode with local DMA
- Software Programmable:
  - Channel list
  - Timers sampling frequency
  - Sampling clock frequency
  - Trigger mode
  - DMA operations

- Built in test program
- VME configuration
- Data monitoring
- Custom firmware can be down-loaded using the VMEbus
- "C" Source Code available
- Lab Windows / CVI

ORDERING INFORMATION



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